74ABT125

Quad buffer; 3-state

Rev. 10.1 — 18 January 2024 Product data sheet

1. General description

The 74ABT125 is a quad buffer/line driver with 3-state outputs controlled by the output enable inputs ($n\overline{OE}$). A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state. This device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

- Supply voltage range from 4.5 V to 5.5 V
- BiCMOS high speed and output drive
- Direct interface with TTL levels
- Power-up 3-state
- Inputs are disabled during 3-state mode
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up protection exceeds 500 mA per JESD78B class II level A
- Quad bus interface
- 3-state buffers
- Live insertion and extraction permitted
- Output capability: HIGH -32 mA; LOW +64 mA
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ABT125D	-40 °C to +85 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74ABT125PW	-40 °C to +85 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74ABT125BQ	-40 °C to +85 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

4. Functional diagram

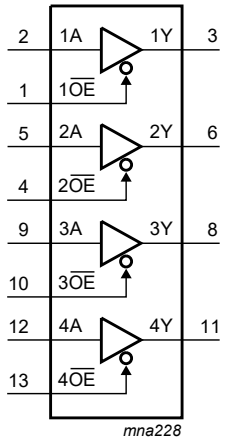


Fig. 1. Logic symbol

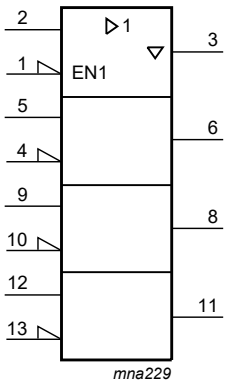


Fig. 2. IEC logic symbol

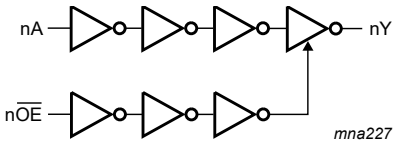
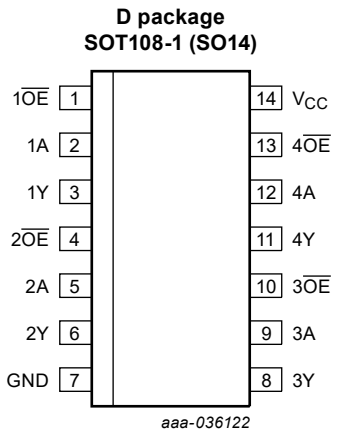
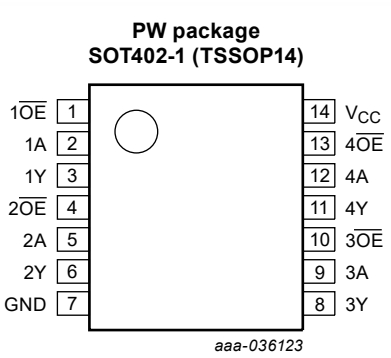


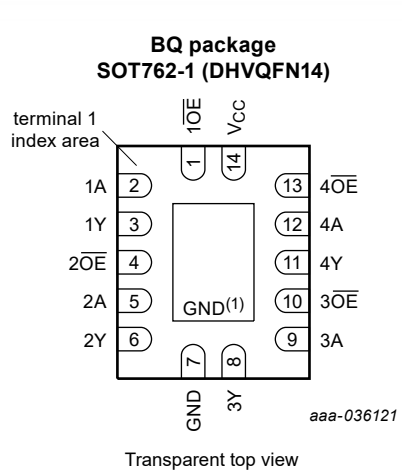
Fig. 3. Logic diagram (one buffer)

5. Pinning information

5.1. Pinning







(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$	1, 4, 10, 13	output enable input (active LOW)
1A, 2A, 3A, 4A	2, 5, 9, 12	data input
1Y, 2Y, 3Y, 4Y	3, 6, 8, 11	data output
GND	7	ground (0 V)
V_{CC}	14	supply voltage

6. Functional description

Table 3. Function selection

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Inputs		Output
$n\overline{OE}$	nA	nY
L	L	L
L	H	H
H	X	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+7.0	V
V_I	input voltage		[1]	-1.2	+7.0	V
V_O	output voltage	output in OFF-state or HIGH-state	[1]	-0.5	+5.5	V
I_{IK}	input clamping current	$V_I < 0$ V		-18	-	mA
I_{OK}	output clamping current	$V_O < 0$ V		-50	-	mA
I_O	output current	output in LOW-state		-	128	mA
T_j	junction temperature		[2]	-	150	°C
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +85 °C	[3]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

[3] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.
For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.
For SOT762-1 (DHVQFN14) package: P_{tot} derates linearly with 9.6 mW/K above 98 °C.

8. Recommended operating conditions

Table 5. Operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		4.5	5.5	V
V_I	input voltage		0	V_{CC}	V
V_{IH}	HIGH-level input voltage		2.0	-	V
V_{IL}	LOW-level Input voltage		-	0.8	V
I_{OH}	HIGH-level output current		-32	-	mA
I_{OL}	LOW-level output current		-	64	mA
$\Delta t/\Delta V$	input transition rise and fall rate		-	10	ns/V
T_{amb}	ambient temperature	in free air	-40	+85	°C

9. Static characteristics

Table 6. Static characteristics

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
V_{IK}	input clamping voltage	V_{CC} = 4.5 V; I_{IK} = -18 mA	-	-0.9	-1.2	-	-1.2	V
V_{OH}	HIGH-level output voltage	V_I = V_{IL} or V_{IH}						
		V_{CC} = 4.5 V; I_{OH} = -3 mA	2.5	2.9	-	2.5	-	V
		V_{CC} = 5.0 V; I_{OH} = -3 mA	3.0	3.4	-	3.0	-	V
		V_{CC} = 4.5 V; I_{OH} = -32 mA	2.0	2.4	-	2.0	-	V
V_{OL}	LOW-level output voltage	V_{CC} = 4.5 V; I_{OL} = 64 mA; V_I = V_{IL} or V_{IH}	-	0.35	0.55	-	0.55	V
I_I	input leakage current	V_{CC} = 5.5 V; V_I = GND or 5.5 V	-	±0.01	±1.0	-	±1.0	µA
I_{OFF}	power-off leakage current	V_{CC} = 0.0 V; V_I or V_O ≤ 4.5 V	-	±5.0	±100	-	±100	µA
$I_{O(pu/pd)}$	power-up/power-down output current	V_{CC} = 2.1 V; V_O = 0.5 V; V_I = GND or V_{CC}; $\overline{OE}$ = don't care [1]	-	±5.0	±50	-	±50	µA
I_{OZ}	OFF-state output current	V_{CC} = 5.5 V; V_I = V_{IL} or V_{IH}						
		V_O = 2.7 V	-	1.0	50	-	50	µA
		V_O = 0.5 V	-	-1.0	-50	-	-50	µA
I_{CEX}	output high leakage current	HIGH-state; V_O = 5.5 V; V_{CC} = 5.5 V; V_I = GND or V_{CC}	-	5.0	50	-	50	µA
I_O	output current	V_{CC} = 5.5 V; V_O = 2.5 V [2]	-50	-100	-180	-50	-180	mA
I_{CC}	supply current	V_{CC} = 5.5 V; V_I = GND or V_{CC}						
		outputs HIGH-state	-	65	250	-	250	µA
		outputs LOW-state	-	12	15	-	30	mA
		outputs disabled	-	65	250	-	250	µA
ΔI_{CC}	additional supply current	per control pin; V_{CC} = 5.5 V; one control input at 3.4 V, other inputs at V_{CC} or GND [3]						
		outputs enabled	-	0.5	1.5	-	1.5	mA
		outputs disabled	-	50	250	-	250	mA
		one enable input at 3.4 V and other inputs at V_{CC} or GND; outputs disabled	-	0.5	1.5	-	1.5	mA
C_I	input capacitance	V_I = 0 V or V_{CC}	-	4	-	-	-	pF
C_O	output capacitance	outputs disabled; V_O = 0 V or V_{CC}	-	7	-	-	-	pF

[1] This parameter is valid for any V_{CC} between 0 V and 2.1 V, with a transition time of up to 10 ms. From V_{CC} = 2.1 V to V_{CC} = 5 V ± 10 %, a transition time of up to 100 µs is permitted.

[2] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[3] This is the increase in supply current for each input at 3.4 V.

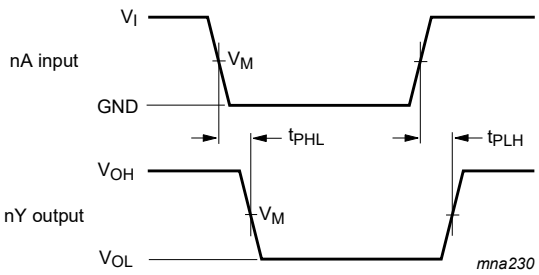
10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V. Test circuit is shown in Fig. 6.

Symbol	Parameter	Conditions	25 °C; V_{CC} = 5.0 V			-40 °C to +85 °C; V_{CC} = 5.0 V ± 0.5 V		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}	LOW to HIGH propagation delay	nA to nY, see Fig. 4	1.0	2.8	4.1	1.0	4.6	ns
t_{PHL}	HIGH to LOW propagation delay	nA to nY; see Fig. 4	1.0	3.1	4.6	1.0	4.9	ns
t_{PZH}	OFF-state to HIGH propagation delay	$n\overline{OE}$ to nY; see Fig. 5	1.0	3.2	5.0	1.0	5.9	ns
t_{PZL}	OFF-state to LOW propagation delay	$n\overline{OE}$ to nY; see Fig. 5	1.0	4.2	6.2	1.0	6.8	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$n\overline{OE}$ to nY; see Fig. 5	1.0	4.1	5.4	1.0	6.2	ns
t_{PLZ}	LOW to OFF-state propagation delay	$n\overline{OE}$ to nY; see Fig. 5	1.5	2.8	5.0	1.5	5.5	ns

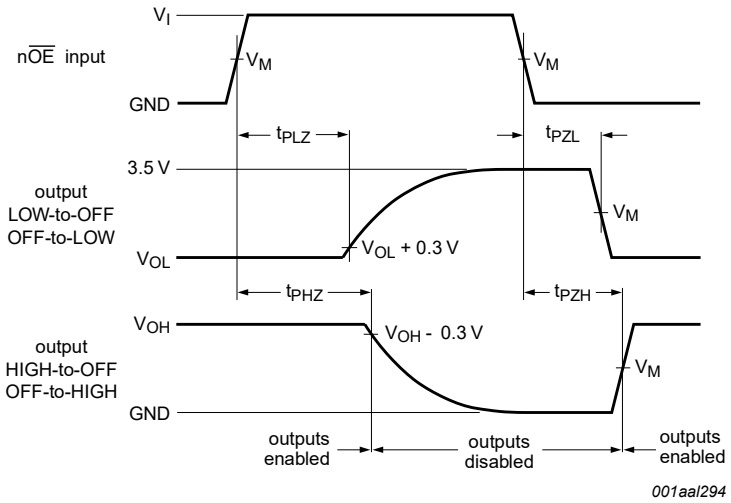
10.1. Waveforms and test circuit



V_M = 1.5 V

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

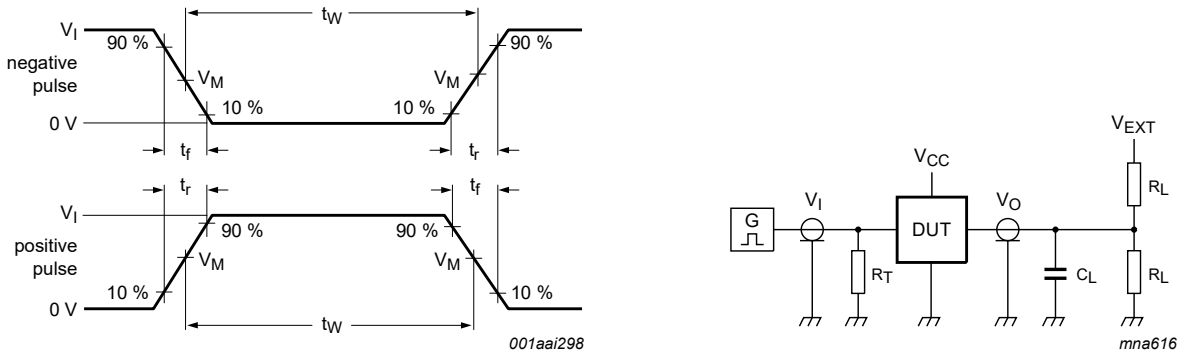
Fig. 4. Propagation delay input (nA) to output (nY)



V_M = 1.5 V

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 5. Enable and disable times



a. Input pulse definition

b. Test circuit

Test data is given in Table 8.

Test circuit definitions:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = Test voltage for switching times.

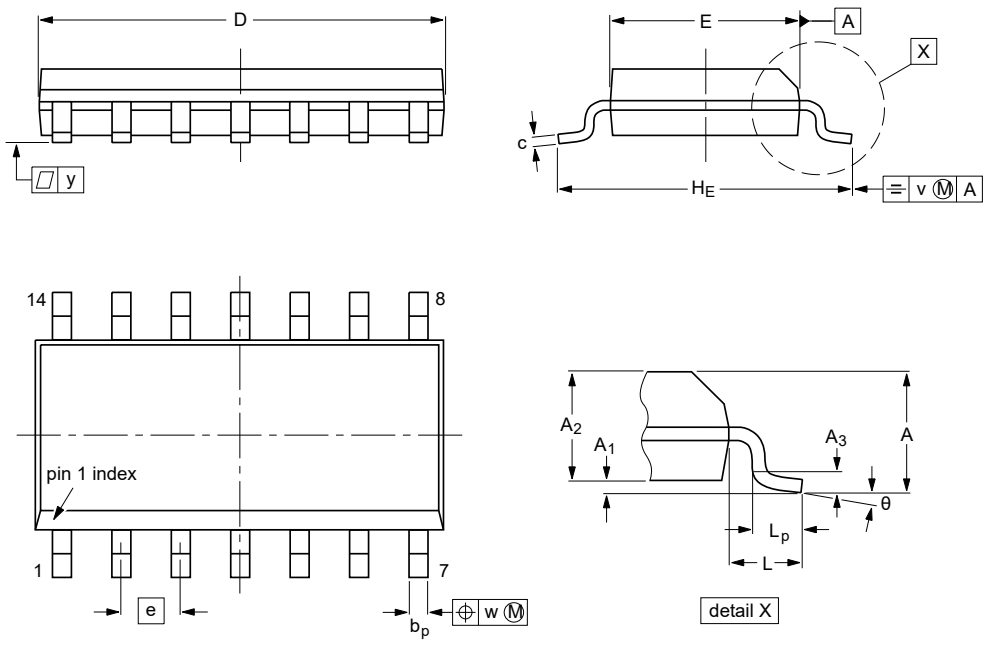
Fig. 6. Test circuit for measuring switching times

Table 8. Test data

Input				Load		V_{EXT}		
V_I	f_I	t_W	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
3.0 V	1 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	open	open	7.0 V

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



Dimensions (inch dimensions are derived from the original mm dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.75	0.25			0.51	0.25	8.75	4.0		6.2		1.27				8°
	nom				0.25					1.27		1.05		0.2	0.25	0.1	
	min		0.10	1.25		0.31	0.10	8.55	3.8		5.8		0.4				0°
inches	max	0.069	0.010			0.020	0.010	0.344	0.16		0.244		0.05				8°
	nom				0.01					0.05		0.041		0.008	0.01	0.004	
	min		0.004	0.049		0.012	0.004	0.337	0.15		0.228		0.016				0°

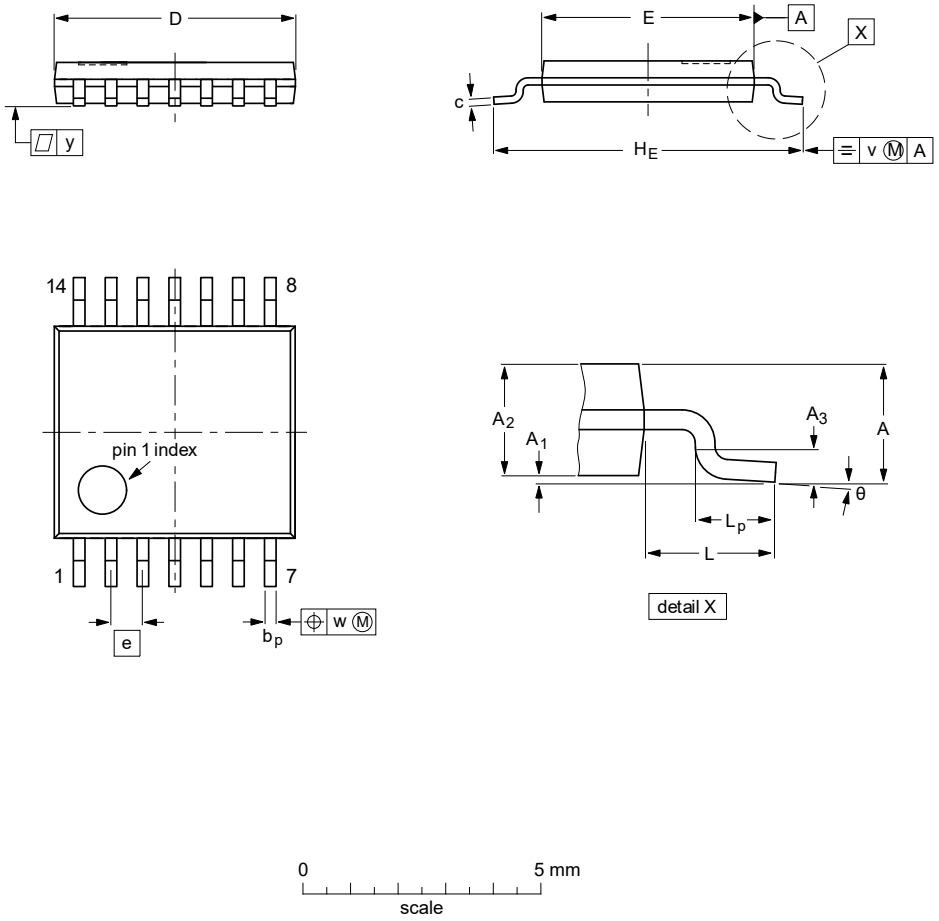
Note
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

sot108-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT108-1		MS-012				~~03-02-19~~ 23-10-27

Fig. 7. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.20	0.15	1.05		0.30	0.2	5.1	4.5		6.6		0.75				8°
	nom				0.25					0.65		1		0.2	0.1	0.1	
	min		0.05	0.80		0.19	0.09	4.9	4.3		6.2		0.45				0°

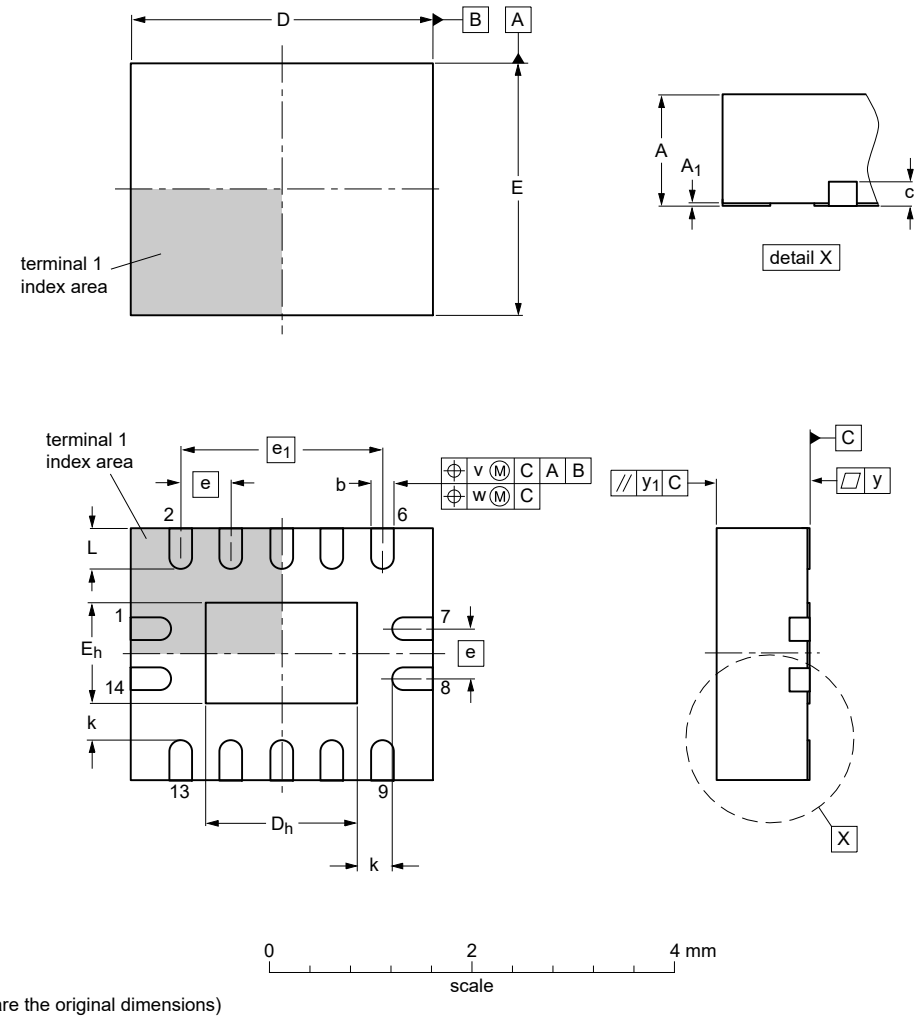
Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot402-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~03-02-18~~ 23-10-27

Fig. 8. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



Dimensions (mm are the original dimensions)

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	k	L	v	w	y	y_1
	max	1	0.05	0.30		3.1	1.65	2.6	1.15				0.5				
mm	nom		0.02	0.25	0.2	3.0	1.50	2.5	1.00	0.5	2		0.4	0.1	0.05	0.05	0.1
	min		0.00	0.18		2.9	1.35	2.4	0.85			0.2	0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot762-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT762-1		MO-241				~~15-04-10~~ 15-05-05

Fig. 9. Package outline SOT762-1 (DHVQFN14)

12. Abbreviations

Table 9. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ABT125 v.10.1	20240118	Product data sheet	-	74ABT125 v.9
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard. • Fig. 7, Fig. 8: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153.			
74ABT125 v.9	20230313	Product data sheet	-	74ABT125 v.8
Modifications:	• Table 6: $I_{CC(max)}$ value at +85 °C (outputs disabled) corrected. (errata).			
74ABT125 v.8	20210630	Product data sheet	-	74ABT125 v.7
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type number 74ABT125DB (SOT337-1/SSOP14) removed. • Section 1 and Section 2 updated. • Section 7: Derating values for P_{tot} total power dissipation updated.			
74ABT125 v.7	20151125	Product data sheet	-	74ABT125 v.6
Modifications:	• Type number 74ABT125N (SOT27-1) removed.			
74ABT125 v.6	20111103	Product data sheet	-	74ABT125 v.5
Modifications:	• Legal pages updated			
74ABT125 v.5	20101124	Product data sheet	-	74ABT125 v.4
74ABT125 v.4	20100427	Product data sheet	-	74ABT125 v.3
74ABT125 v.3	20080429	Product data sheet	-	74ABT125 v.2
74ABT125 v.2	19980116	Product specification	-	74ABT125 v.1
74ABT125 v.1	19960305	-	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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