# FOD8480, FOD8482

# Optically Isolated Intelligent Power Module (IPM) Driver in Stretched Body SOP 6-Pin

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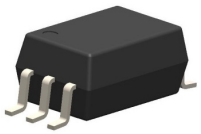
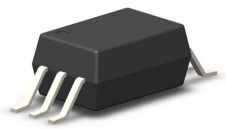


**SOIC6**
**SUFFIX**
**CASE 751EL**



**SOIC6 W**
**SUFFIX**
**CASE 751EM**

### Description

The FOD8480 and FOD8482 are low power optocouplers, which support isolated interface to Intelligent Power Module (IPM) communicating digital control signals from the controller to the IPM, without conducting ground loops or hazardous voltages.

The FOD848x Series, packaged in a stretched body 6−pin small outline plastic package, consists of an aluminum gallium arsenide (AlGaAs) light emitting diode and an integrated high gain photo detector. The detector has a detector threshold with hysteresis. The hysteresis provides differential mode noise immunity and eliminates the potential for output signal chatter. Its non−inverting output is designed as totem pole, which does not require any pull−up resistor.

The FOD8482 has a lower threshold input current, $I_{FLH}$, at 3.0 mA maximum. For the complete FOD848x Series, the Electrical and Switching Characteristics are guaranteed over the extended industrial temperature range of −40°C to 100°C and a $V_{DD}$ range of 4.5 V to 30 V. Low $I_F$ and wide $V_{DD}$ range allow compatibility with TTL, LSTTL, and CMOS logic and result in lower power consumption compared to other high speed optocouplers.

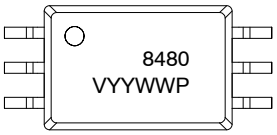
### Features

- Maximum Threshold Input Current, $I_{FLH}$,
  - FOD8480 – 5.5 mA
  - FOD8482 – 3.0 mA
- FOD8480T and FOD8482T – 8 mm Creepage and Clearance Distance, and 0.4 mm Insulation Distance to Achieve Reliable and High Voltage Insulation
- High Noise Immunity Characterized by Common Mode Transient Immunity (CMTI)
- 20 kV/μs Minimum CMTI
- Wide Operating Voltage Range, 4.5 V to 30 V
- Specifications Guaranteed Over Extended Industrial Temperature Range, −40 to 100°C
- Safety and Regulatory Approvals
  - UL1577, 5,000 $VAC_{RMS}$ for 1 Min.
  - DIN−EN/IEC60747−5−5, 1,140 V Peak Working Insulation Voltage

### Typical Applications

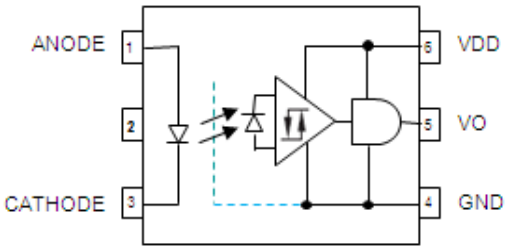
- Isolating Intelligent Power Module
- Isolating Industrial Communication Interface

### MARKING DIAGRAM




8480 or 8482 = Specific Device Number
V = DIN EN/IEC60747−5−5 Option
YY = Two Digit Year Code
WW = Two Digit Work Week
P = Assembly Package Code

### PIN CONNECTIONS




### TRUTH TABLE

| LED | Vo |
|---|---|
| Off | Low |
| On | High |

### ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 10 of this data sheet.

**Table 1. SAFETY AND INSULATION RATINGS for Stretched Body SOP 6−Pin**
As per DIN_EN/IEC60747−5−5. This optocoupler is suitable for “safe electrical insulation” only within the safety limit data. Compliance with the safety ratings shall be ensured by means of protective circuits.

| Parameter | Symbol | FOD8480<br>FOD8482 | FOD8480T<br>FOD8482T | Unit |
|---|---|---|---|---|
| Installation Classifications per DIN VDE 0110/1.89 Table 1, for rated main voltage <150 Vrms | | I−IV | I−IV | |
| for rated main voltage <300 Vrms | | I−IV | I−IV | |
| for rated main voltage <450 Vrms | | I−III | I−IV | |
| for rated main voltage <600 Vrms | | I−III | I−III | |
| Climatic Classification | | 40/100/21 | 40/100/21 | |
| Pollution Degree (DIN VDE 0110/1.89) | | 2 | 2 | |
| Comparative Tracking Index | CTI | 175 | 175 | |
| Input to Output Test Voltage, Method b, VIORM*1.875=$V_{PR}$, 100% Production Test with $t_m$=1 sec,Partial Discharge <5 pC | $V_{PR}$ | 1,671 | 2,137 | $V_{peak}$ |
| Input to Output Test Voltage, Method a, VIORM*1.6 = $V_{PR}$, Type and Sample Test with $t_m$ = 10 sec, Partial Discharge <5 pC | $V_{PR}$ | 1,426 | 1,824 | $V_{peak}$ |
| Max Working Insulation Voltage | $V_{IORM}$ | 891 | 1,140 | $V_{peak}$ |
| Highest Allowable Over Voltage | $V_{IOTM}$ | 6,000 | 8,000 | $V_{peak}$ |
| External Clearance | | 7.0 | 8.0 | mm |
| External Creepage | | 8.0 | 8.0 | mm |
| Insulation thickness | | 0.4 | 0.4 | mm |
| Insulation Resistance at $T_S$,$V_{IO}$ = 500 V | $R_{IO}$ | $10^9$ | $10^9$ | Ω |
| Safety Limit Values− Maximum Values allowed in the event of a failure, | | | | |
| Case Temperature | $T_S$ | 150 | 150 | °C |
| Input Current | $I_{S,INPUT}$ | 200 | 200 | mA |
| Output Power | $P_{S,OUTPUT}$ | 600 | 600 | mW |

**Table 2. ABSOLUTE MAXIMUM RATINGS** ($T_A$ = 25°C unless otherwise specified)

| Symbol | Parameter | Value | Units |
|---|---|---|---|
| $T_{STG}$ | Storage Temperature | −40 to +125 | °C |
| $T_{OPR}$ | Operating Temperature | −40 to +100 | °C |
| $T_J$ | Junction Temperature | −40 to +125 | °C |
| $T_{SOL}$ | Lead Solder Temperature (Refer to Reflow Temperature Profile) | 260 for 10 sec | °C |
| **INPUT CHARACTERISTICS** | | | |
| $I_F$ | Average Forward Input Current | 20 | mA |
| $V_R$ | Reverse Input Voltage | 5.0 | V |
| $PD_I$ | Input Power Dissipation (Notes 1, 3) | 35 | mW |
| **OUTPUT CHARACTERISTICS** | | | |
| $V_{DD}$ | Supply Voltage | 0 to 35 | V |
| $V_O$ | Output Voltage | −0.5 to $V_{DD}$ | V |
| $I_O$ | Average Output Current | 25 | mA |
| $PD_O$ | Output Power Dissipation (Notes 2, 3) | 300 | mW |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**Table 3. RECOMMENDED OPERATING CONDITIONS**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $T_A$ | Ambient Operating Temperature | −40 | +100 | °C |
| $V_{DD}$ | Supply Voltages (Note 4) | 4.5 | 30 | V |
| $V_{F(OFF)}$ | Forward Input Voltage (OFF) | 0 | 0.8 | V |
| $I_{F(ON)}$ | Forward Input Current (ON) (Note 5) | 6.6 | 10 | mA |
| | | 3.6 | 7.5 | mA |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. No derating required across operating temperature range.
2. Derate linearly from 25°C at a rate of 2.87 mW/°C.
3. Functional operation under these conditions is not implied. Permanent damage may occur if the device is subjected to conditions outside these ratings.
4. 0.1 μF bypass capacitor must be connected between Pin 4 and 6.
5. For FOD8480, the initial switching threshold is 5.5 mA or less. It is recommended that 6.6 mA be used to permit at least a 20% CTR degradation guard band. For FOD8482, the initial switching threshold is 3.0 mA or less. It is recommended that 3.6 mA be used to permit at least a 20% CTR degradation guard band.

**Table 4. ISOLATION CHARACTERISTICS** (Apply over all recommended conditions, typical value is measured at $T_A$ = 25°C)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{ISO}$ | Input−Output Isolation Voltage | $T_A$ = 25°C, R.H. < 50%, t = 1.0 min, $I_{I-O} \leq$ 2 μA (Notes 6, 7) | 5,000 | | | $VAC_{RMS}$ |
| $R_{ISO}$ | Isolation Resistance | $V_{I-O}$ = 500 V (Note 6) | | $10^{11}$ | | Ω |
| $C_{ISO}$ | Isolation Capacitance | $V_{I-O}$ = 0 V, freq = 1.0 MHz (Note 6) | | 1.0 | | pF |

6. Device is considered a two terminal device: Pins 1, 2 and 3 are shorted together and Pins 4, 5, and 6 are shorted together.
7. 5,000 $VAC_{RMS}$ for 1 minute duration is equivalent to 6,000 $VAC_{RMS}$ for 1 second duration.

**Table 5. ELECTRICAL CHARACTERISTICS** (Apply over all recommended conditions, $T_A$ = −40°C to +100°C, 4.5 V ≤ $V_{DD}$ ≤ 30 V, FOD8480: $I_{F(ON)}$ = 6 mA to 10 mA, FOD8482: $I_{F(ON)}$ = 4 mA to 7 mA, $V_{F(OFF)}$ = 0 to 0.8 V, unless otherwise specified. Typical value is measured at $T_A$ = 25°C and $V_{DD}$ = 5 V.)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **INPUT CHARACTERISTICS** | | | | | | |
| $V_F$ | Forward Voltage | $I_F$ = 6 mA | | 1.4 | 1.75 | V |
| $BV_R$ | Reverse Breakdown Voltage | $I_R$ = 10 μA | 5.0 | | | V |
| $C_{IN}$ | Input Capacitance | $V_F$ = 0, f = 1 MHz | | 60 | | pF |
| $\Delta V_F/\Delta T_A$ | Input Diode Temperature Coefficient | $I_F$ = 6 mA | | −1.4 | | mV/°C |
| $I_{FLH}$ | Threshold Input Current Low to High | FOD8480 | | 2.2 | 5.5 | mA |
| | | FOD8482 | | 1.45 | 3.0 | mA |
| $I_{HYS}$ | Input Current Hysteresis | $V_{DD}$ = 5 V | | 0.3 | | mA |
| **OUTPUT CHARACTERISTICS** | | | | | | |
| $I_{DDH}$ | Logic High Output Supply Current | $V_{DD}$ = 5 V, $I_F$ = 10 mA | | 1.6 | 2.5 | mA |
| | | $V_{DD}$ = 30 V, $I_F$ = 10 mA | | 1.8 | 2.5 | mA |
| $I_{DDL}$ | Logic Low Output Supply Current | $V_{DD}$ = 5 V, $I_F$ = 0 mA | | 1.6 | 2.5 | mA |
| | | $V_{DD}$ = 30 V, $I_F$ = 0 mA | | 1.8 | 2.5 | mA |
| $I_{OSH}$ | Logic High Short Circuit Output Current | $V_{DD}$ = 5.5 V, $I_F$ = 10 mA, $V_O$ = GND | | | −80 | mA |
| | | $V_{DD}$ = 30 V, $I_F$ = 10 mA, $V_O$ = GND | | | −80 | mA |
| $I_{OSL}$ | Logic Low Short Circuit Output Current | $V_{DD}$ = $V_O$ = 5.5 V, $V_F$ = 0 V | 80 | | | mA |
| | | $V_{DD}$ = $V_O$ = 30 V, $V_F$ = 0 V | 80 | | | mA |
| $V_{OH}$ | Logic High Output Voltage | $I_{OH}$ = −2.6 mA | $V_{DD}$ − 0.1 | $V_{DD}$ − 0.04 | | V |
| | | $I_{OH}$ = −0.4 mA | $V_{DD}$ − 0.1 | $V_{DD}$ − 0.01 | | V |
| $V_{OL}$ | Logic Low Output Voltage | $I_{OL}$ = 6.4 mA, $V_F$ = 0 V | | | 0.5 | V |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

**Table 6. SWITCHING CHARACTERISTICS** (Apply over all recommended conditions, $T_A$ = −40°C to +100°C, 4.5V ≤ $V_{DD}$ ≤ 30 V, FOD8480: $I_{F(ON)}$ = 6 mA to 10 mA, FOD8482: $I_{F(ON)}$ = 4 mA to 7 mA, $V_{F(OFF)}$ = 0 to 0.8 V, unless otherwise specified. Typical value is measured at $T_A$ = 25°C and $V_{DD}$ = 5 V.)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Date Rate | | | | | 1 | Mbit/s |
| $t_{PHL}$ | Propagation Delay Time to Logic Low Output | With peaking capacitor, $C_L$ = 15 pF | | 130 | 300 | ns |
| $t_{PLH}$ | Propagation Delay Time to Logic High Output | With peaking capacitor, $C_L$ = 15 pF | | 100 | 300 | ns |
| PWD | Pulse Width Distortion, $\lvert t_{PHL} - t_{PLH} \rvert$ | With peaking capacitor, $C_L$ = 15 pF | | | 250 | ns |
| $t_{PSK}$ | Propagation Delay Skew (Note 8) | With peaking capacitor, $C_L$ = 15 pF | | | 150 | ns |
| $t_R$ | Output Rise Time (10% − 90%) | | | 15 | | ns |
| $t_F$ | Output Fall Time (90% − 10%) | | | 10 | | ns |
| $\lvert CM_H \rvert$ | Common Mode Transient Immunity at Output High | $I_F$ = $I_{F(ON)}$, $V_O$ > 2.0 V, $V_{CM}$ = 1000 V, $T_A$ = 25°C (Note 9) | 20 | 40 | | kV/μs |
| $\lvert CM_L \rvert$ | Common Mode Transient Immunity at Output Low | $I_F$ = 0 mA, $V_O$ < 0.8 V, $V_{CM}$ = 1000 V, $T_A$ = 25°C (Note 9) | 20 | 40 | | kV/μs |

8. $t_{PSK}$ is equal to the magnitude of the worst case difference in $t_{PHL}$ and/or $t_{PLH}$ that will be seen between any two units from the same manufacturing date code that are operated at same case temperature (±5°C), at same operating conditions, with equal loads (CL = 15 pF), and with an input rise time less than 5 ns.
9. Common mode transient immunity at output high is the maximum tolerable negative dVcm/dt on the trailing edge of the common mode impulse signal, Vcm, to assure that the output will remain high. Common mode transient immunity at output low is the maximum tolerable positive dVcm/dt on the leading edge of the common pulse signal, Vcm, to assure that the output will remain low.

## TYPICAL CHARACTERISTICS

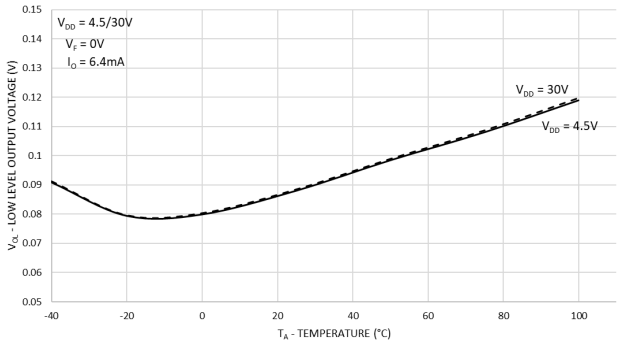



**Figure 1. Typical Logic Low Output Voltage vs. Temperature**

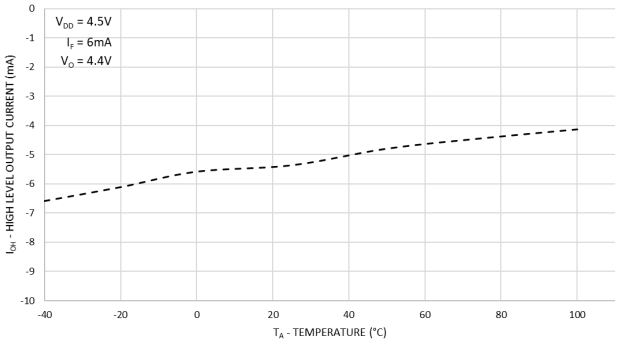



**Figure 2. Typical Logic High Output Current vs. Temperature**

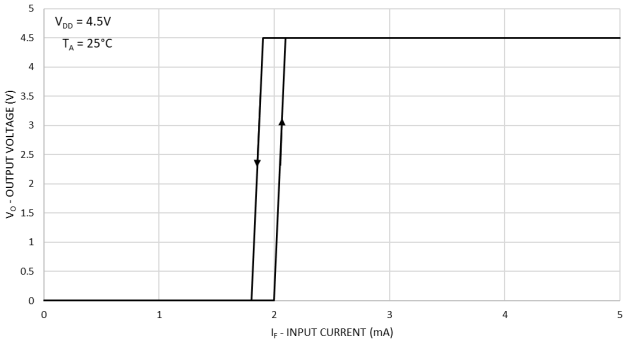



**Figure 3. Typical Output Voltage vs. Forward Input Current (FOD8480)**

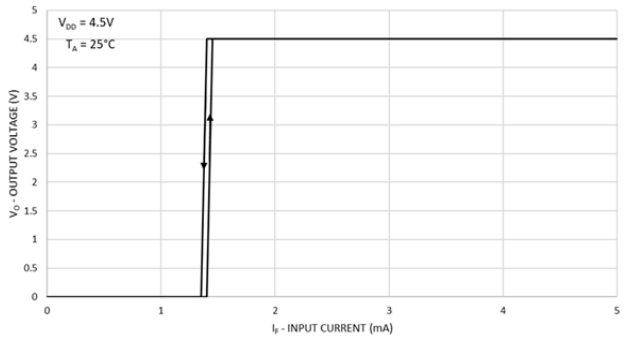



**Figure 4. Typical Output Voltage vs. Forward Input Current (FOD8482)**

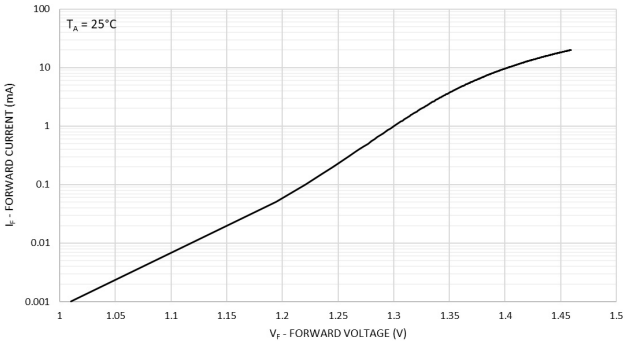



**Figure 5. Typical Input Diode Forward Characteristic**

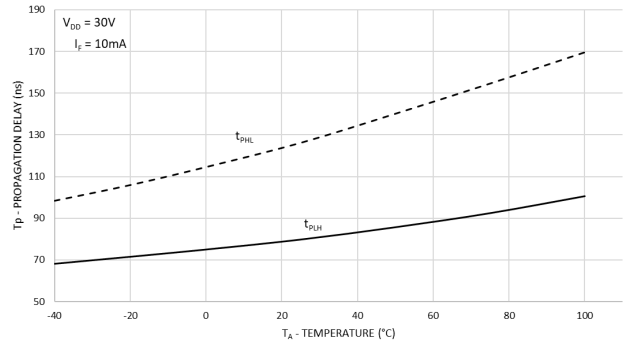



**Figure 6. Typical Propagation Delay vs. Temperature**

## TYPICAL CHARACTERISTICS

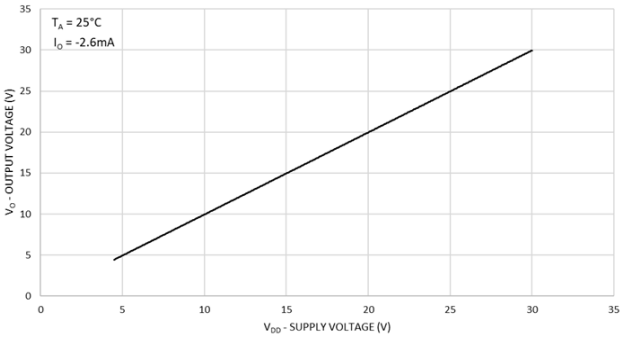



**Figure 7. Typical Logic High Output Voltage vs. Supply Voltage**

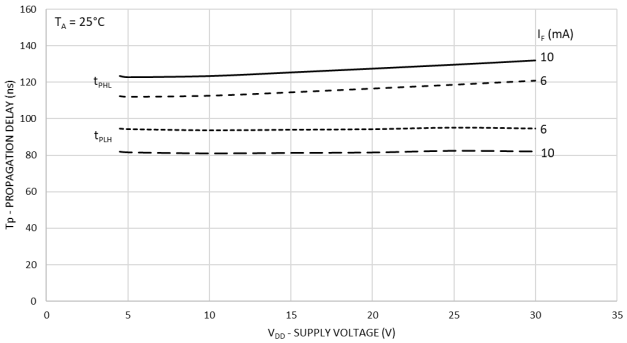



**Figure 8. Typical Propagation Delay vs. Supply Voltage**

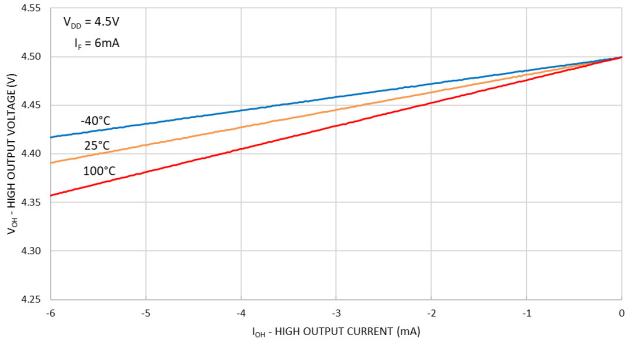



**Figure 9. $V_{OH}$ vs. $I_{OH}$ Across Temperatures**

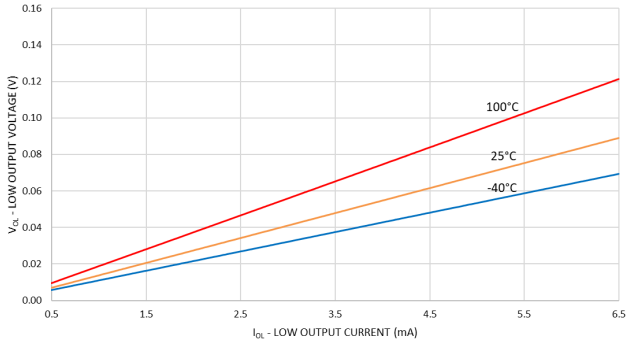



**Figure 10. $V_{OL}$ vs. $I_{OL}$ Across Temperatures**

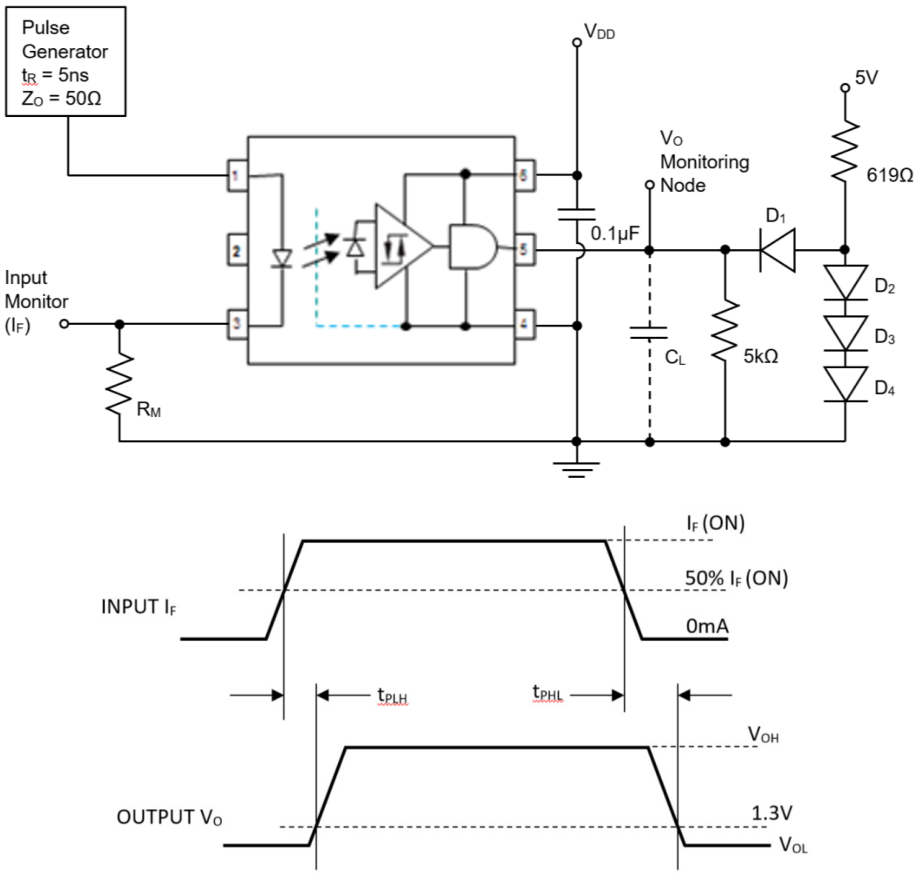



**Figure 11. Test Circuit for Propagation Delay, Rise Time and Fall Time**

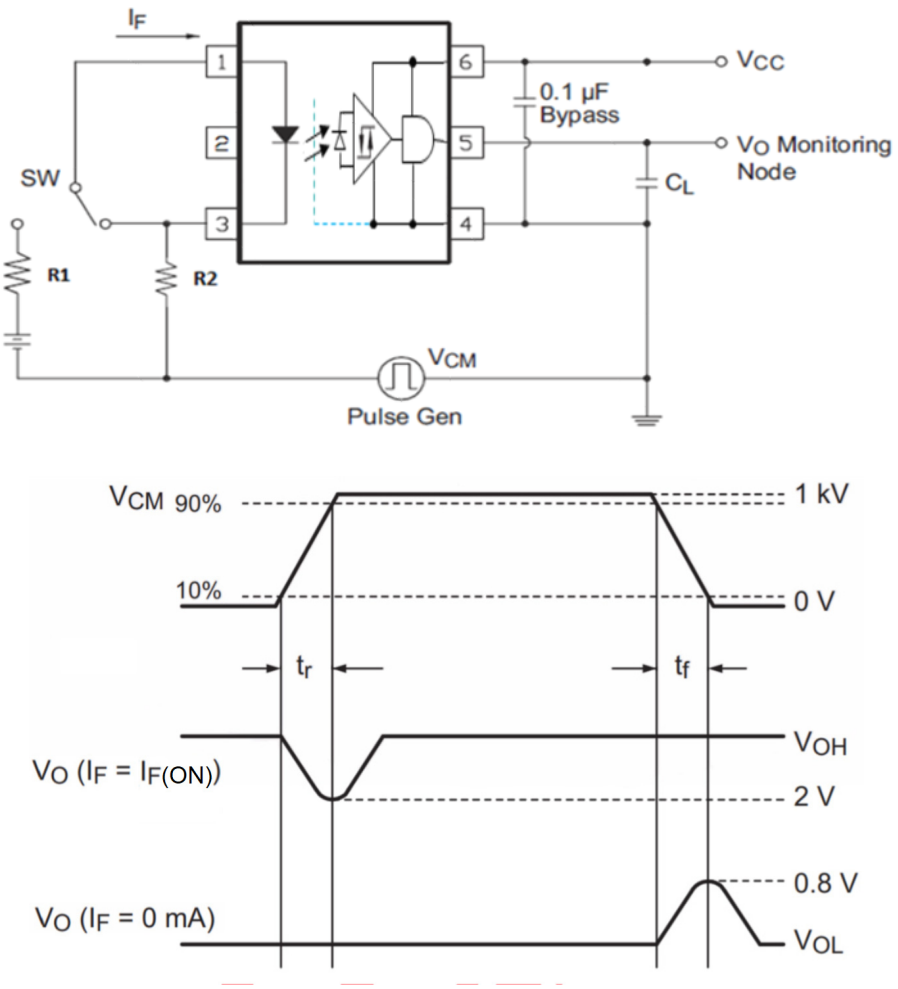
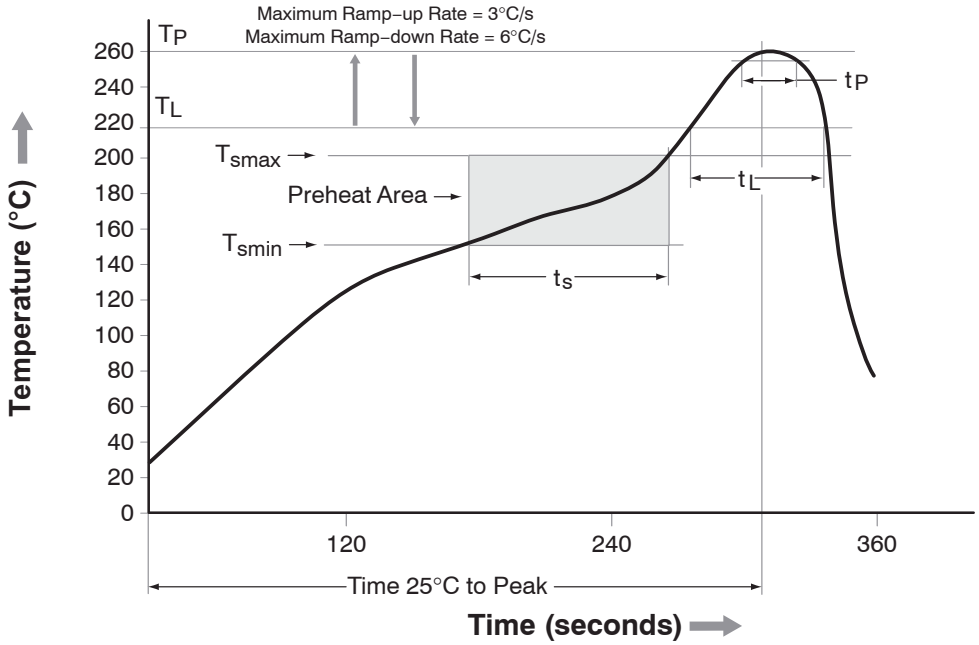



**Figure 12. Test Circuit for Instantaneous Common−Mode Rejection Voltage**

## Reflow Profile




| Profile Freature | Pb−Free Assembly Profile |
|---|---|
| Temperature Minimum ($T_{smin}$) | 150°C |
| Temperature Maximum ($T_{smax}$) | 200°C |
| Time ($t_S$) from ($T_{smin}$ to $T_{smax}$) | 60 s to 120 s |
| Ramp−up Rate ($t_L$ to $t_P$) | 3°C/second maximum |
| Liquidous Temperature ($T_L$) | 217°C |
| Time ($t_L$) Maintained Above ($T_L$) | 60 s to 150 s |
| Peak Body Package Temperature | 260°C +0°C / −5°C |
| Time ($t_P$) within 5°C of 260°C | 30 s |
| Ramp−Down Rate ($T_P$ to $T_L$) | 6°C/s maximum |
| Time 25°C to Peak Temperature | 8 minutes maximum |

**Figure 13. Reflow Profile**

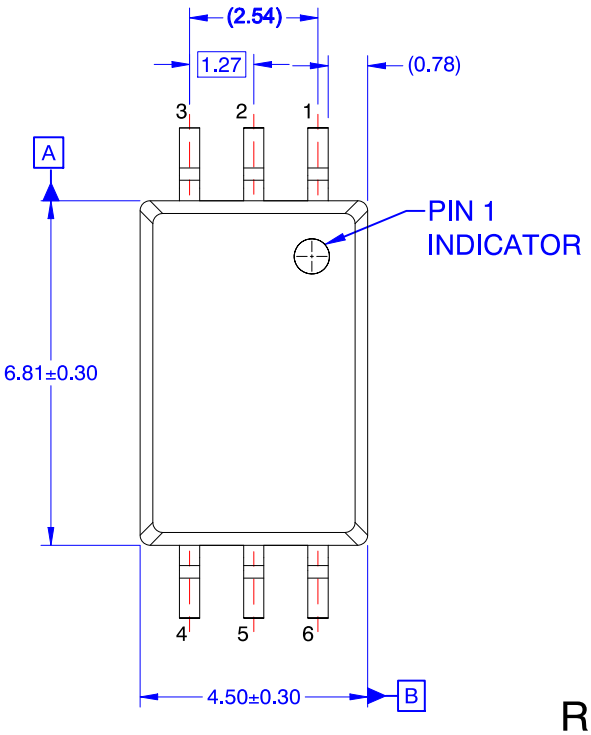
## ORDERING INFORMATION

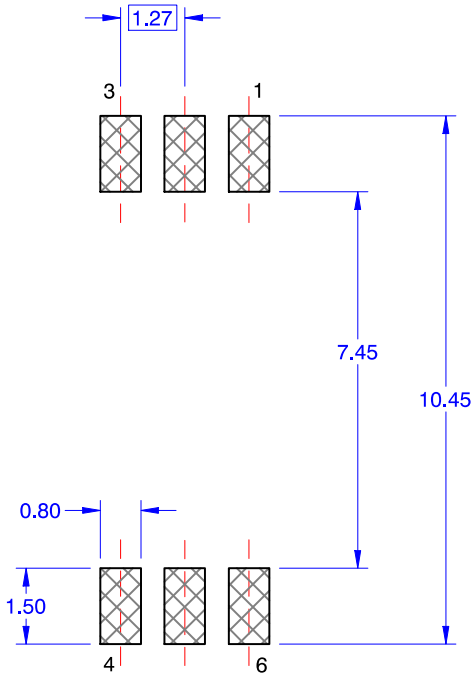
| Part Number | Package | Packing Method |
|---|---|---|
| FOD8480 | Stretched Body SOP 6−Pin | Tube (100 units per tube) |
| FOD8480R2 | Stretched Body SOP 6−Pin | Tape and Reel (1,000 units per reel) |
| FOD8480V | Stretched Body SOP 6−Pin,<br>DIN EN/IEC60747−5−5 Option | Tube (100 units per tube) |
| FOD8480R2V | Stretched Body SOP 6−Pin,<br>DIN EN/ IEC60747−5−5 Option | Tape and Reel (1,000 units per reel) |
| FOD8480T | Stretched Body SOP 6−Pin, Wide Lead | Tube (100 units per tube) |
| FOD8480TR2 | Stretched Body SOP 6−Pin, Wide Lead | Tape and Reel (1,000 units per reel) |
| FOD8480TV | Stretched Body SOP 6−Pin, Wide Lead,<br>DIN EN/IEC60747−5−5 Option | Tube (100 units per tube) |
| FOD8480TR2V | Stretched Body SOP 6−Pin, Wide Lead,<br>DIN EN/ IEC60747−5−5 Option | Tape and Reel (1,000 units per reel) |

*All packages are lead free per JEDEC: J−STD−020B standard.

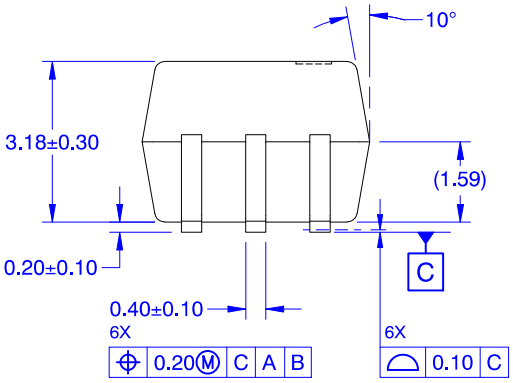
**SOIC6**
CASE 751EL
ISSUE O

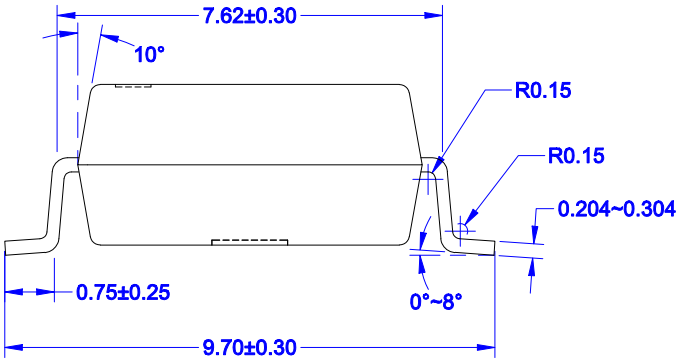
DATE 30 SEP 2016




## RECOMMENDED LAND PATTERN




NOTES: UNLESS OTHERWISE SPECIFIED
A) NO STANDARD APPLIES TO THIS PACKAGE
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH, AND TIE BAR EXTRUSION.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M–2009.

| | | |
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**SOIC6 W**
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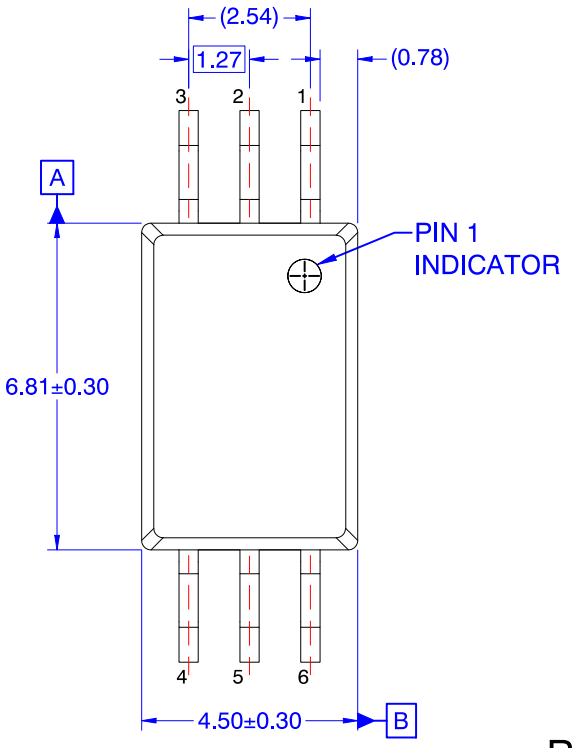
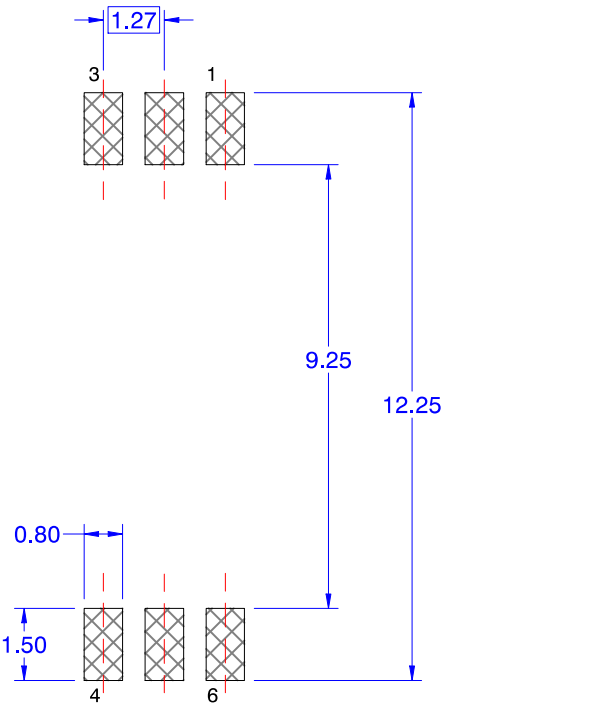
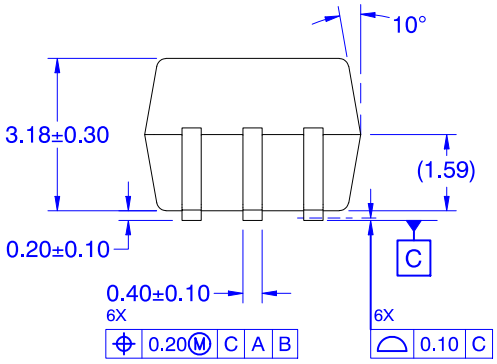
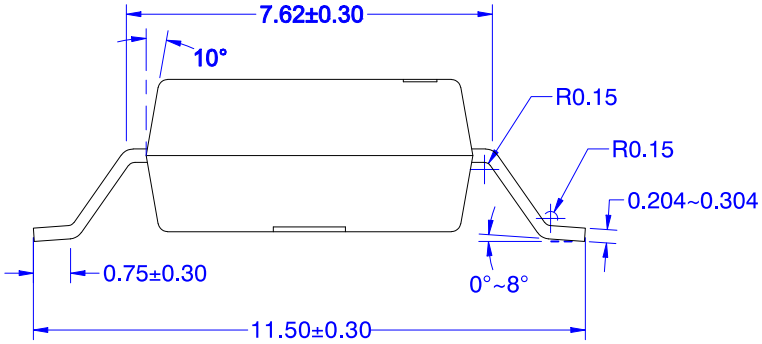
DATE 30 SEP 2016




## RECOMMENDED LAND PATTERN




NOTES: UNLESS OTHERWISE SPECIFIED
A) NO STANDARD APPLIES TO THIS PACKAGE
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH, AND TIE BAR EXTRUSION.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M–2009.

| | | |
|---|---|---|
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| **DESCRIPTION:** | **SOIC6 W** | **PAGE 1 OF 1** |

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