# MP163

## 700V, Non-Isolated, Offline Regulator with Integrated LDO

The Future of Analog IC Technology

## DESCRIPTION

The MP163 is a primary-side regulator that provides accurate, dual-output, constant voltage (CV) regulation without an optocoupler. The MP163 supports buck, boost, buck-boost, and flyback topologies and has an integrated 700V MOSFET and an LDO to simplify the structure and reduce cost. These features make the MP163 an ideal regulator for offline, low-power applications, such as home appliances and standby power.

The MP163 is a green-mode operation regulator. Both the peak current and switching frequency decrease as the load decreases. This feature provides excellent efficiency at light load and improves overall average efficiency.

Full protection features include thermal shutdown, VCC under-voltage lockout (UVLO), overload protection (OLP), short-circuit protection (SCP), and open-loop protection.

The MP163 is available in SOIC16 and SOIC8-7B packages.

| Part Number | Typical HV Regulator Peak Current Limit | Typical HV MOSFET $R_{DS(on)}$ | LDO Output Voltage |
|---|---|---|---|
| MP163A-33 | 210mA | 16Ω | 3.3V |
| MP163A-5 | | | 5V |
| MP163B-33 | 420mA | 14Ω | 3.3V |
| MP163B-5 | | | 5V |
| MP163C-33 | 660mA | 13.5Ω | 3.3V |
| MP163C-5 | | | 5V |

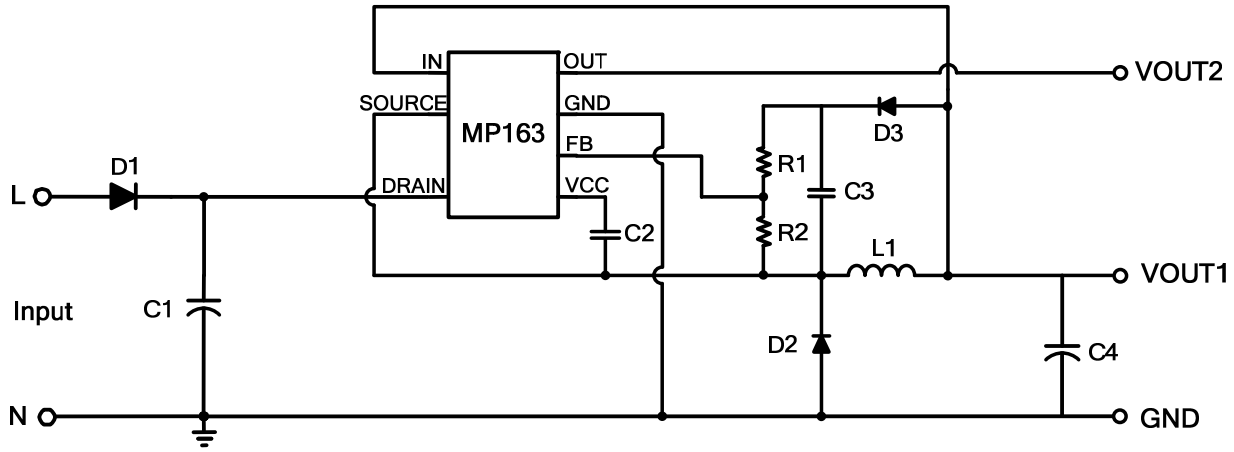
## FEATURES

- Primary-Side Constant Voltage (CV) Control, Supporting Buck, Boost, Buck-Boost, and Flyback Topologies
- Integrated 700V MOSFET and Current Source
- Internal LDO, Optimized for Dual Output Applications
- Less than 30mW of No-Load Power Consumption
- Up to 4W of Output Power
- Low VCC Operating Current
- Frequency Foldback
- Limited Maximum Frequency
- Peak-Current Compression
- Internally Biased VCC
- Thermal Shutdown, UVLO, OLP, SCP, and Open-Loop Protection
- Available in SOIC16 and SOIC8-7B Packages

## APPLICATIONS

- Home Appliances, White Goods, and Consumer Electronics
- Industrial Controls
- Standby Power

## TYPICAL APPLICATION



## ORDERING INFORMATION

| Part Number* | Package | Top Marking |
|---|---|---|
| MP163AGS-5 | SOIC8-7B | *See Below* |
| MP163AGSE-5 | SOIC16 | *See Below* |
| MP163AGS-33 | SOIC8-7B | *See Below* |
| MP163AGSE-33 | SOIC16 | *See Below* |
| MP163BGS-5 | SOIC8-7B | *See Below* |
| MP163BGSE-5 | SOIC16 | *See Below* |
| MP163BGS-33 | SOIC8-7B | *See Below* |
| MP163BGSE-33 | SOIC16 | *See Below* |
| MP163CGS-5 | SOIC8-7B | *See Below* |
| MP163CGSE-5 | SOIC16 | *See Below* |
| MP163CGSE-33 | SOIC16 | *See Below* |
| MP163CGS-33 | SOIC8-7B | *See Below* |

* For Tape & Reel, add suffix –Z (e.g. MP163AGS-33–Z)

## TOP MARKING (MP163AGS-5)

MP163A-5
LLLLLLLL
MPSYWW

M163A-5: Part number
LLLLLLLL: Lot number
MPS: MPS prefix
Y: Year code
WW: Week code

## TOP MARKING (MP163AGSE-5)

MPS YYWW
MP163A-5
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP163A-5: Part number
LLLLLLLLL: Lot number

## TOP MARKING (MP163AGS-33)

M163A-33
LLLLLLLL
MPSYWW

M163A-33: Part number
LLLLLLLL: Lot number
MPS: MPS prefix
Y: Year code
WW: Week code

## TOP MARKING (MP163AGSE-33)

MPS YYWW
MP163A-33
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP163A-33: Part number
LLLLLLLLL: Lot number

## TOP MARKING (MP163BGS-5)

MP163B-5
LLLLLLLL
MPSYWW

MP163B-5: Part number
LLLLLLLL: Lot number
MPS: MPS prefix
Y: Year code
WW: Week code

## TOP MARKING (MP163BGSE-5)

MPS YYWW
MP163B-5
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP163B-5: Part number
LLLLLLLLL: Lot number

## TOP MARKING (MP163BGS-33)

M163B-33
LLLLLLLL
MPSYWW

M163B-33: Part number
LLLLLLLL: Lot number
MPS: MPS prefix
Y: Year code
WW: Week code

## TOP MARKING (MP163BGSE-33)

MPS YYWW
MP163B-33
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP163B-33: Part number
LLLLLLLLL: Lot number

## TOP MARKING (MP163CGS-5)

MP163C-5
LLLLLLLL
MPSYWW

MP163C-5: Part number
LLLLLLLL: Lot number
MPS: MPS prefix
Y: Year code
WW: Week code

## TOP MARKING (MP163CGSE-5)

MPS YYWW
MP163C-5
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP163C-5: Part number
LLLLLLLLL: Lot number

## TOP MARKING (MP163CGS-33)

M163C-33
LLLLLLLL
MPSYWW

M163C-33: Part number
LLLLLLLL: Lot number
MPS: MPS prefix
Y: Year code
WW: Week code

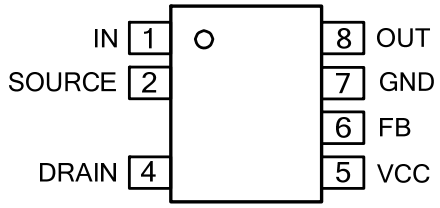
## TOP MARKING (MP163CGSE-33)

MPS YYWW
MP163C-33
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP163C-33: Part number
LLLLLLLLL: Lot number

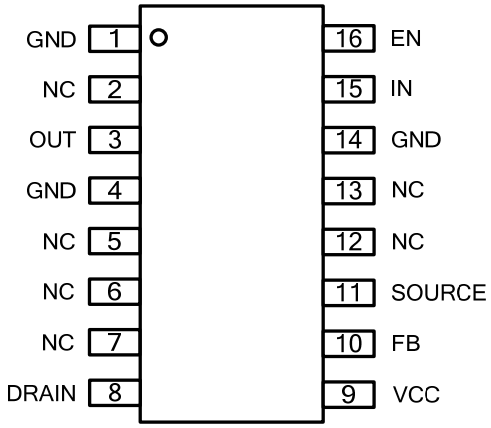
## PACKAGE REFERENCE

**TOP VIEW**




**SOIC-8-7B**

**TOP VIEW**




**SOIC-16**

## ABSOLUTE MAXIMUM RATINGS (1)

DRAIN to all other pins ..... -0.3V to 700V
SOURCE, VCC, FB to all other pins (except DRAIN)..... -0.3V to 700V
EN, IN to GND ..... -0.3V to 42V
OUT to GND..... -0.3V to 17V
VCC, FB to SOURCE ..... -0.3V to 6.5V
Continuous power dissipation ($T_A$ = +25°C) (2)
SOIC-8-7B .....1.45W
SOIC-16 ..... 1.56W
Junction temperature ..... 150°C
Lead temperature..... 260°C
Storage temperature .....-60°C to +150°C
ESD capability human body model ..... 2.0kV

## *Recommended Operating Conditions* (3)

Operating junction temp. ($T_J$)....-40°C to +125°C

| *Thermal Resistance* (4) | $\theta_{JA}$ | $\theta_{JC}$ | |
|---|---|---|---|
| SOIC-8-7B | 86 | 38 | °C/W |
| SOIC-16 | 80 | 35 | °C/W |

**NOTES:**

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature $T_J$(MAX), the junction-to-ambient thermal resistance $\theta_{JA}$, and the ambient temperature TA. The maximum allowance continuous power dissipation at any ambient temperature is calculated by $P_D(MAX)=(T_J(MAX)-T_A)/\theta_{JA}$. Exceeding the maximum allowance power dissipation will produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuit protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS

**VCC = 5.5V, $T_J$ = -40°C ~ 125°C, min and max are guaranteed by characterization, typical is tested at 25°C, unless otherwise specified.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Start-Up Current Source and Internal MOSFET (DRAIN)** | | | | | | |
| Internal regulator supply current | $I_{regulator}$ | VCC = 4V, $V_{DRAIN}$ = 100V | 2.2 | 4.1 | 6 | mA |
| DRAIN leakage current | $I_{Leak}$ | VCC = 5.8V, $V_{DRAIN}$ = 400V | | 10 | 17 | µA |
| Breakdown voltage | $V_{(BR)DSS}$ | $T_J$ = 25°C | 700 | | | V |
| On resistance | $R_{on}$ | MP163AGS-5, MP163AGS-33, MP163AGSE-5, MP163AGSE-33, $T_J$ = 25°C | | 16 | 20 | Ω |
| | | MP163BGS-5, MP163BGS-33, MP163BGSE-5, MP163BGSE-33, $T_J$ = 25°C | | 14 | 18 | |
| | | MP163CGS-5, MP163CGS-33, MP163CGSE-5, MP163CGSE-33, $T_J$ = 25°C | | 13.5 | 17 | |
| **Supply Voltage Management (VCC)** | | | | | | |
| VCC level (increasing) where the internal regulator stops | $VCC_{OFF}$ | | 5.4 | 5.6 | 6 | V |
| VCC level (decreasing) where the internal regulator turns on | $VCC_{ON}$ | | 5.1 | 5.3 | 5.8 | V |
| VCC regulator on and off hysteresis | | | 130 | 250 | | mV |
| VCC level (decreasing) where the IC stops | $VCC_{stop}$ | | 3 | 3.4 | 3.6 | V |
| VCC level (decreasing) where the protection phase ends | $VCC_{pro}$ | | | 2.4 | 2.8 | V |
| Internal IC consumption | $I_{CC}$ | $T_{ON}$ = $\tau_{maxon}$, $T_{OFF}$ = $\tau_{minoff}$ | | | 720 | µA |
| Internal IC consumption (no switching) | $I_{CC}$ | | | | 200 | µA |
| Internal IC consumption, latch-off phase | $I_{CCLATCH}$ | VCC = 5.3V | | 16 | 24 | µA |
| **Internal Current Sense** | | | | | | |
| Leading-edge blanking | $\tau_{LEB1}$ | | | 350 | | ns |
| Leading-edge blanking for SCP (5) | $\tau_{LEB1}$ | | | 180 | | ns |
| Peak current limit | $I_{Limit}$ | MP163AGS-5, MP163AGS-33, MP163AGSE-5, MP163AGSE-33, $T_J$ = 25°C | 188 | 210 | 232 | mA |
| | | MP163BGS-5, MP163BGS-33, MP163BGSE-5, MP163BGSE-33, $T_J$ = 25°C | 380 | 420 | 460 | |
| | | MP163CGS-5, MP163CGS-33, MP163CGSE-5, MP163CGSE-33, $T_J$ = 25°C | 600 | 660 | 720 | |

## ELECTRICAL CHARACTERISTICS *(continued)*

**VCC = 5.5V, $T_J$ = -40°C ~ 125°C, min and max are guaranteed by characterization, typical is tested at 25°C, unless otherwise specified.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| SCP threshold | $I_{SCP}$ | MP163AGS-5, MP163AGS-33, MP163AGS-5, MP163AGS-33, $T_J$ = 25°C | 330 | 400 | 510 | mA |
| | | MP163BGS-5, MP163BGS-33, MP163BGSE-5, MP163BGSE-33, $T_J$ = 25°C | 500 | 600 | 760 | |
| | | MP163CGS-5, MP163CGS-33, MP163CGSE-5, MP163CGSE-33, $T_J$ = 25°C | 750 | 900 | | |
| **Feedback Input (FB)** | | | | | | |
| Minimum off time | $\tau_{minoff}$ | MP163AGS-5, MP163AGS-33, MP163AGS-5, MP163AGS-33 | 7.5 | 10 | 12.5 | µs |
| | | MP163BGS-5, MP163BGS-33, MP163BGSE-5, MP163BGSE-33 | 9 | 12 | 15 | |
| | | MP163CGS-5, MP163CGS-33, MP163CGSE-5, MP163CGSE-33 | 9.5 | 12 | 15 | |
| Maximum on time | $\tau_{maxon}$ | MP163AGS-5, MP163AGS-33, MP163AGS-5, MP163AGS-33 | 13 | 18 | 23 | µs |
| | | MP163BGS-5, MP163BGS-33, MP163BGSE-5, MP163BGSE-33 | 17 | 24 | 31 | |
| | | MP163CGS-5, MP163CGS-33, MP163CGSE-5, MP163CGSE-33 | 19 | 24 | 31 | |
| Primary MOSFET feedback turn-on threshold | $V_{FB}$ | | 2.45 | 2.55 | 2.65 | V |
| OLP feedback trigger threshold | $V_{FB\_OLP}$ | MP163AGS-5, MP163AGS-33, MP163AGSE-5, MP163AGSE-33, MP163BGS-5, MP163BGS-33, MP163BGSE-5, MP163BGSE-33, | 1.64 | 1.74 | 1.84 | V |
| | | MP163CGS-5, MP163CGS-33, MP163CGSE-5, MP163CGSE-33, | 1.6 | 1.7 | 1.8 | |
| OLP delay time | $\tau_{OLP}$ | MP163AGS-5, MP163AGS-33, MP163AGSE-5, MP163AGSE-33, $T_{ON} = \tau_{maxon}$, $T_{OFF} = \tau_{minoff}$ | | 175 | | ms |
| | | MP163BGS-5, MP163BGS-33, MP163BGSE-5, MP163BGSE-33, MP163CGS-5, MP163CGS-33, MP163CGSE-5, MP163CGSE-33, $T_{ON} = \tau_{maxon}$, $T_{OFF} = \tau_{minoff}$ | | 220 | | |
| Open-loop detection | $V_{OLD}$ | | 0.4 | 0.5 | 0.6 | V |
| **Thermal Shutdown** | | | | | | |
| Thermal shutdown threshold (5) | | | | 150 | | °C |
| Thermal shutdown recovery hysteresis (5) | | | | 30 | | °C |

## ELECTRICAL CHARACTERISTICS *(continued)*

**$V_{EN}$ = $V_{IN}$, $C_{OUT}$ = 1µF, $T_J$ = -40°C ~ 125°C, min and max are guaranteed by characterization, typical is tested at 25°C, unless otherwise specified.**

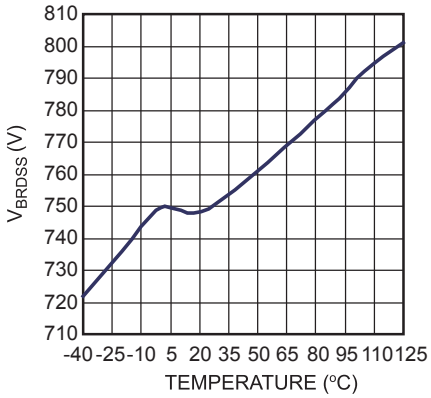
| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **LDO** | | | | | | |
| LDO load current limit | $I_{LDO}$ | MP163AGS-33, MP163AGSE-33, MP163BGS-33, MP163BGSE-33, MP163CGS-33, MP163CGSE-33 $V_{OUT}$ = 0V, $V_{IN}$ = 4.3V, $T_J$ = 25°C | 180 | 270 | 390 | mA |
| | | MP163AGS-5, MP163AGSE-5, MP163BGS-5, MP163BGSE-5, MP163CGS-5, MP163CGSE-5, $V_{OUT}$ = 0V, $V_{IN}$ = 6V, $T_J$ = 25°C | | | | |
| Dropout voltage | $V_{DROPOUT}$ | $I_{LOAD}$ = 150mA, $V_{IN}$ = $V_{OUT(NOM)}$ - 0.1V | | 620 | 1100 | mV |
| Output voltage | $V_{LDO}$ | MP163AGS-33, MP163AGSE-33, MP163BGS-33, MP163BGSE-33, MP163CGS-33, MP163CGSE-33, $V_{IN}$ = 4.3V, $I_{OUT}$ = 0A | 3.234 | 3.3 | 3.366 | V |
| | | MP163AGS-5, MP163AGSE-5, MP163BGS-5, MP163BGSE-5, MP163CGS-5, MP163CGSE-5, $V_{IN}$ = 6V, $I_{OUT}$ = 0A | 4.9 | 5 | 5.1 | |
| EN rising threshold | $EN_{TH\_R}$ | MP163AGSE-5, MP163AGSE-33, MP163BGSE-5, MP163BGSE-33, MP163CGSE-5, MP163CGSE-33, $V_{IN}$ = $V_{OUT(NOM)}$ + 1V | 1.32 | 1.48 | 1.64 | V |
| EN falling threshold | $EN_{TH\_F}$ | MP163BGSE-5, MP163BGSE-33, MP163BGSE-5, MP163BGSE-33, MP163CGSE-5, MP163CGSE-33, $V_{IN}$ = $V_{OUT(NOM)}$ + 1V | 1.07 | 1.26 | 1.46 | V |
| Shutdown supply current | $I_{SHDN}$ | MP163AGSE-5, MP163AGSE-33, MP163BGSE-5, MP163BGSE-33, MP163CGSE-5, MP163CGSE-33, $V_{EN}$ = 0V, $V_{IN}$ = 40V | | 3 | 9 | µA |
| EN input current | $I_{EN}$ | MP163AGSE-5, MP163AGSE-33, MP163BGSE-5, MP163BGSE-33, MP163CGSE-5, MP163CGSE-33, VEN = 15V, VIN = 40V | | | 0.1 | µA |
| Thermal shutdown (5) | | | | 165 | | °C |
| Thermal shutdown hysteresis (5) | | | | 20 | | °C |

**NOTE:**

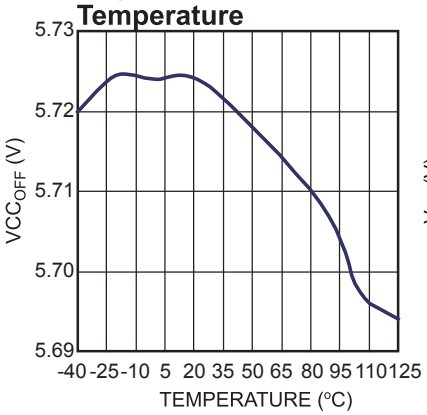
5) Guaranteed by design.

## TYPICAL CHARACTERISTICS

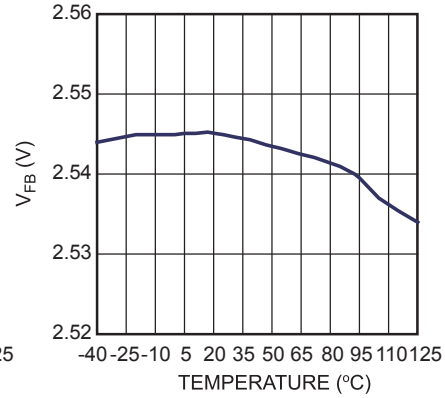
### Breakdown Voltage vs. Temperature



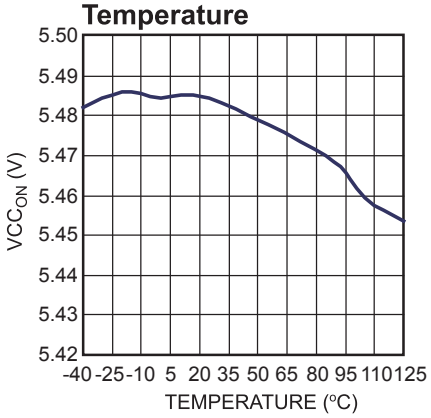

### VCC Increasing Level at which the Internal Regulator Stops vs. Temperature



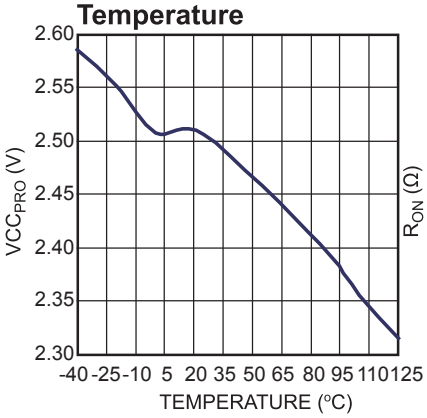

### Feedback Voltage vs. Temperature



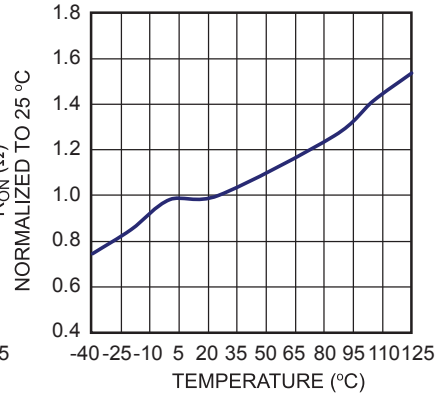

### VCC Decreasing Level at which the Internal Regulator Turns On vs. Temperature



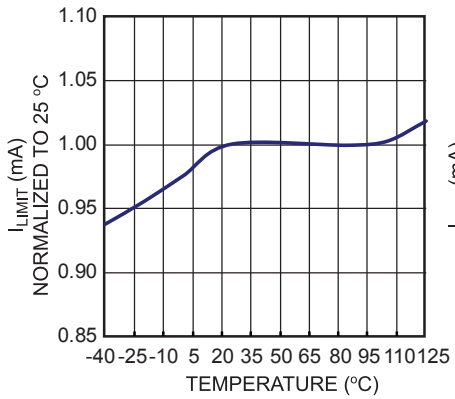

### VCC Decreasing Level at which the Protection Phase Ends vs. Temperature



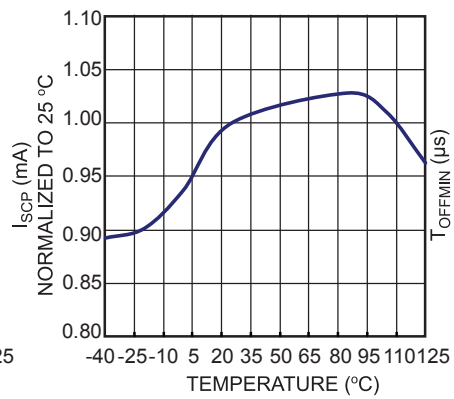

### On State Resistance vs. Temperature



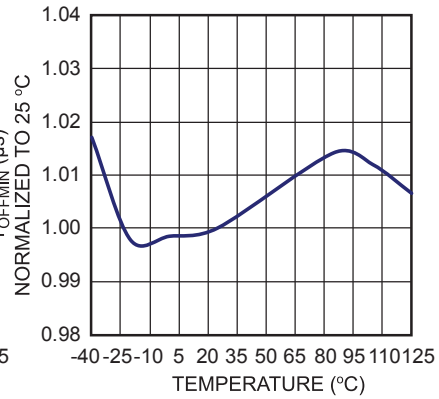

### Peak Current Limit vs. Temperature




### SCP Point vs. Temperature




### Minimum Off Time vs. Temperature

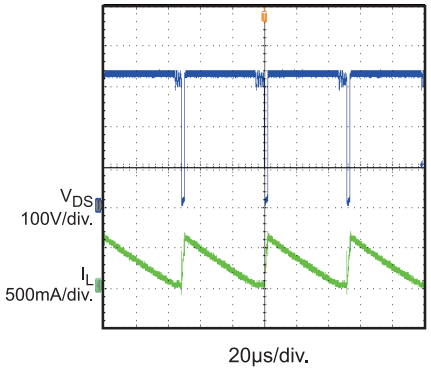


## TYPICAL PERFORMANCE CHARACTERISTICS

**MP163CGS-5, $V_{IN}$ = 230$V_{AC}$, $V_{OUT1}$ = 12V, $I_{OUT1}$ = 200mA, $V_{OUT2}$ = 5V, $I_{OUT2}$ = 50mA, L = 1mH, $T_A$ = +25°C, unless otherwise noted.**

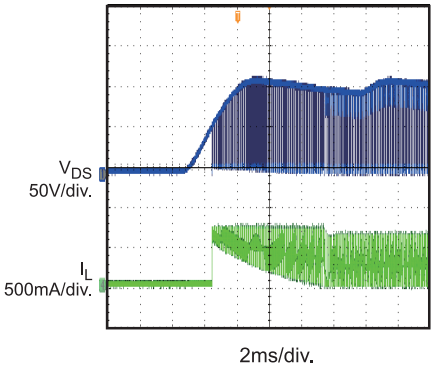
### Normal Opration

$V_{IN}$=230VAC,Full Load



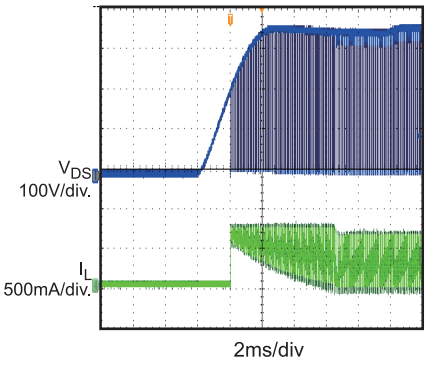

### Soft Start

$V_{IN}$=85VAC



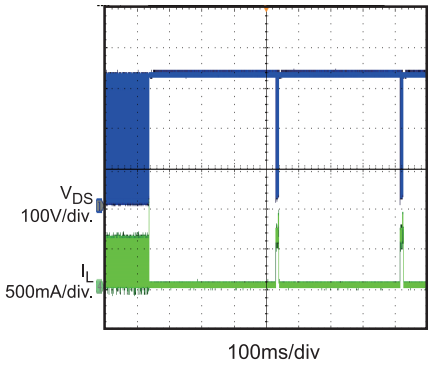

### Soft Start

$V_{IN}$=265VAC



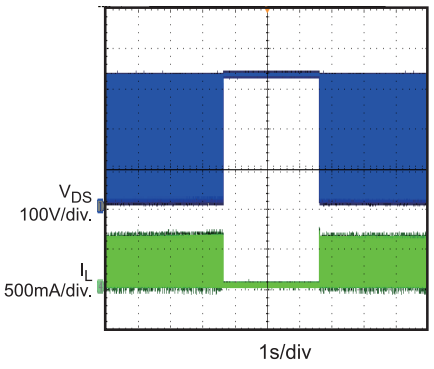

### SCP

$V_{IN}$=230VAC



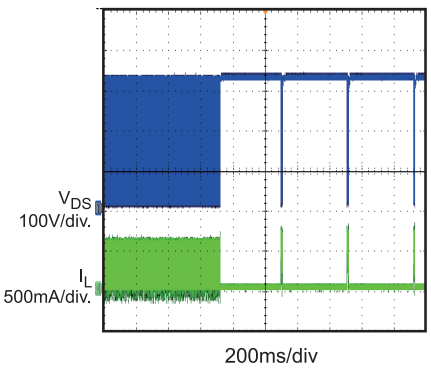

### Thermal Down

$V_{IN}$=230VAC



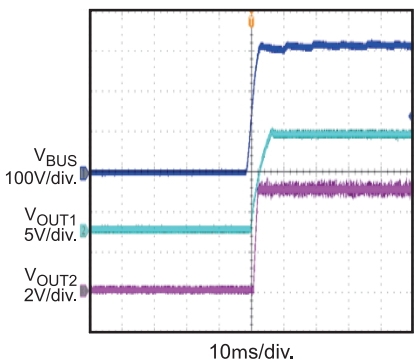

### Open Loop

$V_{IN}$=230VAC,Full Load



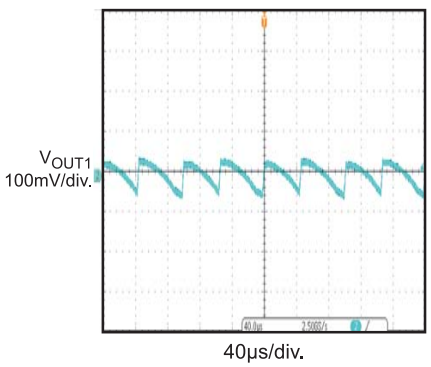

### Turn-On Delay

$V_{IN}$ = 230VAC, Full Load




### Output1 Ripple

$V_{IN}$ = 230VAC, Full Load



## PIN FUNCTIONS

| Pin # SOIC8-7B | Pin # SOIC16 | Name | Description |
|---|---|---|---|
| 1 | 15 | IN | **Input voltage of the LDO.** |
| 2 | 11 | SOURCE | **Internal power MOSFET source.** SOURCE is also the ground reference for VCC and FB. |
| 4 | 8 | DRAIN | **Internal power MOSFET drain.** DRAIN is also the high-voltage current source input. |
| 5 | 9 | VCC | **Control circuit power supply.** |
| 6 | 10 | FB | **Regulator feedback.** |
| 7 | 1, 4, 14 | GND | **Ground of the LDO.** |
| 8 | 3 | OUT | **Output voltage of the LDO.** |
| - | 16 | EN | **Enable of the integrated LDO.** Drive EN to logic high to enable the LDO. Drive EN to logic low to shut down the LDO. |
| - | 2, 5, 6, 7, 12, 13 | NC | **No connection.** |

## BLOCK DIAGRAM

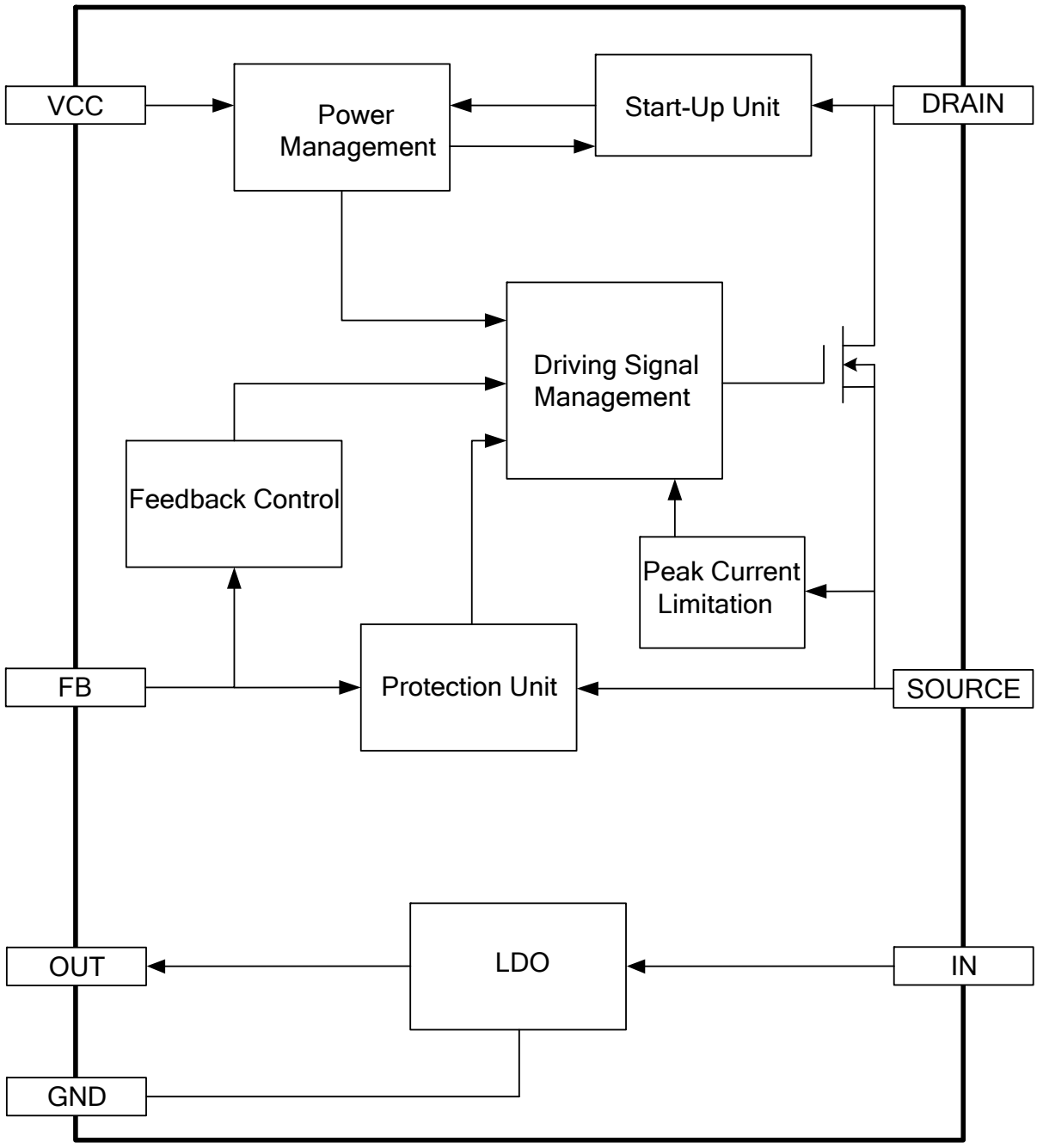



**Figure 1: Functional Block Diagram**

# OPERATION

The MP163 is a green-mode operation regulator. The peak current and the switching frequency both decrease with a decreasing load. As a result, the MP163 offers excellent light-load efficiency and improves overall average efficiency. The regulator also incorporates multiple features and operates with a minimum number of external components.

The MP163 acts as a fully integrated regulator when used in a buck topology (see the Typical Application on page 2).

### Start-Up and Under-Voltage Lockout (UVLO)

The internal high-voltage regulator self-supplies the IC from DRAIN. When VCC reaches $VCC_{OFF}$, the IC starts switching, and the internal high-voltage regulator turns off. The internal high-voltage regulator turns on to charge the external VCC capacitor when VCC falls below $VCC_{ON}$. A small capacitor (in the low µF range) maintains VCC and lowers the capacitor cost.

The IC stops switching when VCC drops below $VCC_{stop}$.

Under fault conditions (such as OLP, SCP, and TSD) the IC stops switching, and an internal current source (~16µA) discharges the VCC capacitor. The internal high-voltage regulator will not charge the VCC capacitor until VCC drops below $VCC_{pro}$. The restart time can be estimated using Equation (1):

$$T_{restart} = C_{VCC} \times \left( \frac{VCC - VCC_{pro}}{I_{CCLATCH}} + \frac{VCC_{OFF} - VCC_{pro}}{I_{regulator}} \right) \quad (1)$$

### Soft Start (SS)

The IC stops operation when VCC drops below $VCC_{stop}$. The IC begins operation when VCC charges to $VCC_{OFF}$. There is a soft-start period whenever the chip starts operation. Soft start prevents the inductor current from overshooting by limiting the minimum off time.

The MP163 adopts a two-phase minimum off-time limit soft start. Each soft-start phase lasts for 128 switching cycles. During soft start, the off-time limit shortens gradually from $\tau_{minoff\_SS1}$ to $\tau_{minoff\_SS2}$ and reaches $\tau_{minoff}$ (see Figure 2).

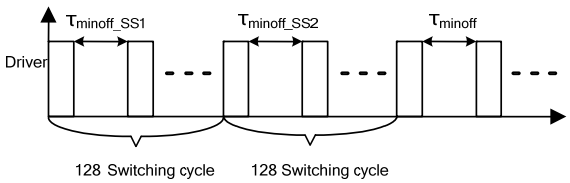



**Figure 2: Minimum Off Time at Start-Up**

### Constant Voltage (CV) Operation

The MP163 regulates the output voltage by monitoring the sampling capacitor (C3).

At the beginning of each cycle, the integrated MOSFET turns on while the feedback voltage drops below the 2.55V reference voltage, which indicates an insufficient output voltage. The peak current limitation determines the on period. After the on period elapses, the integrated MOSFET turns off. The sampling capacitor (C3) voltage is charged to the output voltage through D3 when the freewheeling diode (D2) turns on. This way, the sampling capacitor (C3) samples and holds the output voltage for output regulation. The sampling capacitor (C3) voltage decreases when the inductor (L1) current falls below the output current. When the feedback voltage falls below the 2.55V reference voltage, a new switching cycle begins. Figure 3 shows this operation in continuous conduction mode (CCM).

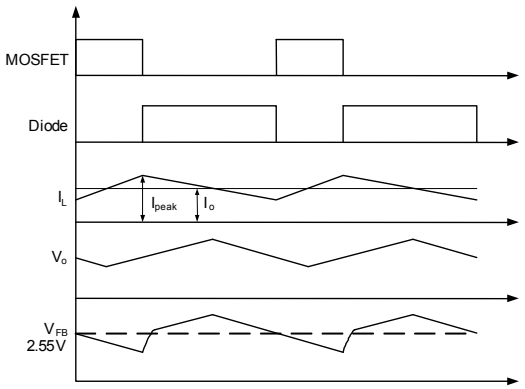



**Figure 3: $V_{FB}$ vs. $V_O$**

Determine the output voltage with Equation (2):

$$Vo = 2.55V \times \frac{R1 + R2}{R2} \quad (2)$$

### Frequency Foldback and Peak Current Compression

The MP163 remains highly efficient at light-load condition by reducing the switching frequency automatically.

Under light-load or no-load conditions, the output voltage drops very slowly, which increases the MOSFET off time, and the frequency decreases with the load.

The switching frequency in CCM is determined with Equation (3):

$$f_s = \frac{(V_{in} - V_o)}{2L(I_{peak} - I_o)} \cdot \frac{V_o}{V_{in}} \quad (3)$$

The switching frequency in discontinuous conduction mode (DCM) is determined with Equation (4):

$$f_s = \frac{2(V_{in} - V_O)}{LI^2_{peak}} \cdot \frac{I_o V_o}{V_{in}} \quad (4)$$

As the peak current limit decreases from $I_{Limit}$, the off time increases. In standby mode, the frequency and the peak current are both minimized, allowing for a smaller dummy load. As a result, peak current compression helps further reduce no-load consumption. The peak current limit can be estimated with Equation (5):

$$I_{Peak} = (1 - 0.0038 \times (T_{off} - \tau_{min\,off})/\mu s) \times I_{Limit} \quad (5)$$

Where $T_{off}$ is the off time of the power module.

### Error Amplifier (EA) Compensation

The MP163 has an internal error amplifier (EA) compensation loop that samples the feedback voltage 6μs after the MOSFET turns off and regulates the output based on the 2.55V reference voltage.

### Ramp Compensation

An internal ramp compensation circuit improves the load regulation. An exponential voltage signal is added to pull down the reference voltage of the feedback comparator (see Figure 4). The ramp compensation is a function of the load conditions. The compensation is about 1mV/μs in full-load condition and increases exponentially as the peak current decreases.

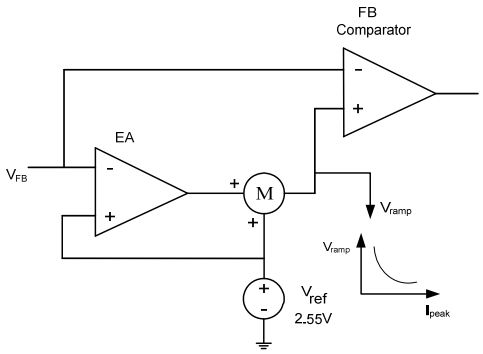



**Figure 4: EA and Ramp Compensation**

### Overload Protection (OLP)

The maximum output power of the MP163 is limited by the maximum switching frequency and peak current limit. If the load current is too large, the output voltage drops, causing the FB voltage to drop.

When FB voltage drops below $V_{FB\_OLP}$, this is considered to be an error flag, and the timer starts. If the timer reaches 220ms ($f_S$ = 28kHz), overload protection (OLP) occurs. This timer duration prevents OLP from being triggered when the power supply starts up or the load transitions. The power supply should start up in less than 220ms ($f_S$ = 28kHz). The OLP delay time is calculated using Equation (6):

$$\tau_{Delay} \approx 220ms \times \frac{28kHz}{f_s} \quad (6)$$

### Short-Circuit Protection (SCP)

The MP163 monitors the peak current and shuts down the MOSFET when the peak current rises above the short-circuit protection (SCP) threshold. The power supply resumes operation with the removal of the fault.

### Thermal Shutdown

To prevent thermal-induced damage, the MP163 stops switching when the junction temperature exceeds 150°C. During thermal shutdown, the VCC capacitor is discharged to $VCC_{pro}$, and then the internal high-voltage regulator re-charges. The MP163 recovers when the junction temperature drops below 120°C.

### Open-Loop Detection

If FB voltage is less than 0.5V, the IC stops switching, and a restart cycle begins. During a soft start, the open-loop detection is blanked.

### Leading-Edge Blanking (LEB)

An internal leading-edge blanking (LEB) unit avoids premature switching pulse termination due to a turn-on spike. A turn-on spike is caused by parasitic capacitance and reverse recovery of the freewheeling diode. During the blanking time, the current comparator is disabled and cannot turn off the external MOSFET. Figure 5 shows the leading-edge blanking.

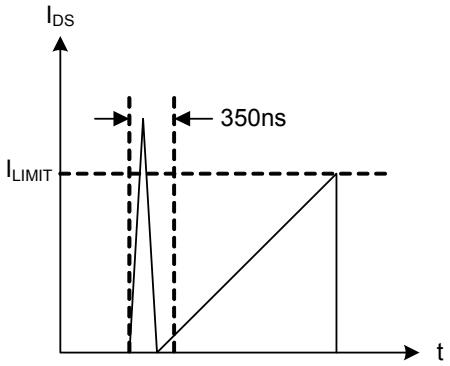



**Figure 5: Leading-Edge Blanking**

### Integrated LDO

The continuous output current of the integrated LDO is up to 150mA but is also limited by the thermal performance. The peak output current is limited to 270mA in OLP.

When the input of the integrated LDO (usually the high-side buck output of the MP163) is much higher than its output, there is a large power dissipation on the MP163, which worsens the thermal performance. An external resistor connected to IN can help with the LDO thermal by sharing part of the total voltage drop.

# APPLICATION INFORMATION

### Topology Options

The MP163 can be used in common topologies such as buck, boost, buck-boost, and flyback.

Component selection is based on the Typical Application shown on page 2.

### Selecting the Input Capacitor

The input capacitor supplies DC input voltage for the converter. Figure 6 shows the typical DC bus voltage waveform of a half-wave rectifier and a full-wave rectifier.

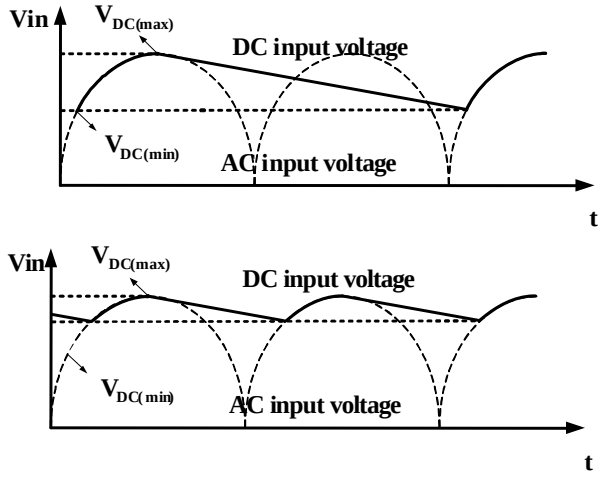



**Figure 6: Input Voltage Waveform**

Typically, the use of a half-wave rectifier requires an input capacitor rated at 3μF/W for the universal input condition. When using a full-wave rectifier, the input capacitor is chosen between 1.5 ~ 2μF/W for the universal input condition. A half-wave rectifier is recommended for output applications less than 2W. Otherwise, use a full-wave rectifier.

Under very low input voltages, the inductor current ramps up slowly. It may not reach the current limit during $\tau_{maxon}$, so the MOSFET on time should be less than the minimum value of $\tau_{maxon}$.

### Selecting the Inductor

The MP163 has a minimum off time limit that determines the maximum power output. A power inductor with a larger inductance increases the maximum power. Using a very small inductor may cause failure at full load. The maximum power in CCM can be calculated with Equation (7)

$$P_{omax} = V_o(I_{peak} - \frac{V_o \tau_{minoff}}{2L}) \quad (7)$$

The maximum power in DCM can be calculated with Equation (8):

$$P_{omax} = \frac{1}{2} L I_{peak}^2 \cdot \frac{1}{\tau_{minoff}} \quad (8)$$

For mass production, tolerance on the parameters (such as peak-current limitation and the minimum off time) should be taken into consideration.

### Freewheeling Diode

Select a diode with a maximum reverse voltage rating greater than the maximum input voltage and a current rating determined by the output current.

The reverse recovery of the freewheeling diode can affect efficiency and circuit operation during CCM, so use an ultra-fast diode, such as the UGC10JH.

### Selecting the Output Capacitor

The output capacitor is required to maintain the DC output voltage. Estimate the output voltage ripple in CCM using Equation (9):

$$V_{CCM\_ripple} = \frac{\Delta i}{8 f_s C_o} + \Delta i \cdot R_{ESR} \quad (9)$$

Estimate the output voltage ripple in DCM with Equation (10):

$$V_{DCM\_ripple} = \frac{I_o}{f_s C_o} \cdot \left( \frac{I_{pk} - I_o}{I_{pk}} \right)^2 + I_{pk} \cdot R_{ESR} \quad (10)$$

It is recommended to use ceramic, tantalum, or low ESR electrolytic capacitors to reduce the output voltage ripple.

### Feedback Resistors

The resistor divider connected to FB determines the output voltage. Choose appropriate R1 and R2 values to set the output voltage. R2 should be about a few kΩ to tens of kΩ in value.

### Feedback Capacitor

The feedback capacitor provides a sample-and-hold function. Small capacitors result in poor regulation at light loads, and large capacitors affect the circuit operation. Roughly estimate an optimal capacitor value using Equation (11):

$$\frac{1}{2}\frac{V_o}{R_1+R_2}\cdot\frac{C_o}{I_o}\le C_{FB}\le\frac{V_o}{R_1+R_2}\cdot\frac{C_o}{I_o} \quad (11)$$

### Dummy Load

A dummy load is required to maintain the load regulation. This ensures sufficient inductor energy to charge the sample-and-hold capacitor to detect the output voltage. Normally, a 3mA dummy load is needed and can be adjusted according to the regulated voltage. There is a compromise between small, no-load consumption and good, no-load regulation, especially for applications that require 30mW of no-load consumption. Use a Zener diode to reduce the no-load consumption if no-load regulation is not a concern.

### Auxiliary VCC Supply

For MP163 applications which have a $V_{OUT}$ above 7V, a less than 30mW no-load power consumption can be achieved by adopting an external VCC supply to reduce overall power consumption (see Figure 7).

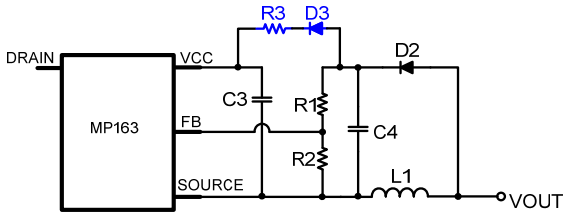



**Figure 7: Auxiliary VCC Supply Circuit**

This auxiliary VCC supply is derived from the resistor connected between C3 and C4. C4 should be larger than the value recommended above. D3 is used in case that VCC interferes with FB. R3 is determined using Equation (12):

$$R3\approx\frac{V_{OUT}-V_{FW}-5.8V}{I_S} \quad (12)$$

Where $I_S$ is the VCC consumption under a no-load condition, and $V_{FW}$ is the forward voltage drop of D3. Because $I_S$ varies in different applications, R3 should be adjusted to meet the application's specific $I_S$. In a particular configuration, $I_S$ is measured at about 200μA.

### Surge Performance

An appropriate input capacitor value should be chosen to obtain a good surge performance. Figure 8 shows the half-wave rectifier. Table 1 shows the capacitance required under normal conditions for different surge voltages. FR1 is a 20Ω/2W fused resistor, and L1 is 1mH for this recommendation.

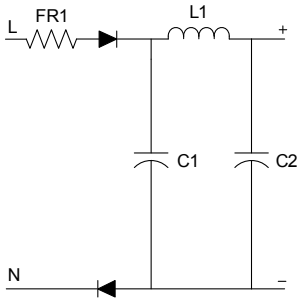



**Figure 8: Half-Wave Rectifier**

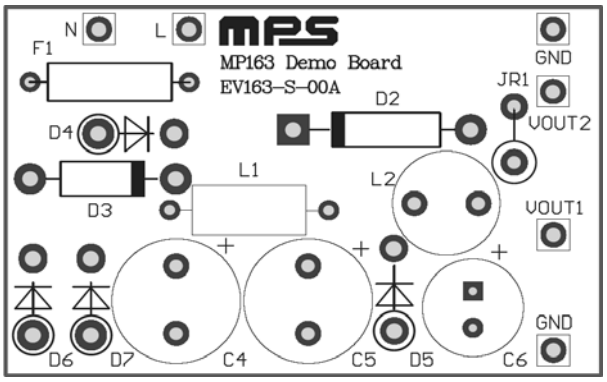
**Table 1: Recommended Capacitance**

| Surge Voltage | 500V | 1000V | 2000V |
|---|---|---|---|
| **C1** | 1μF | 2.2μF | 3.3μF |
| **C2** | 1μF | 2.2μF | 3.3μF |

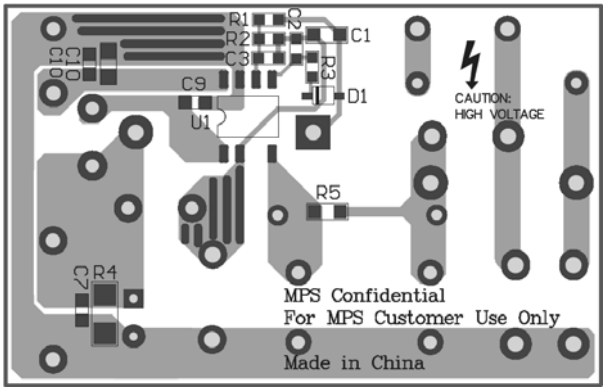
## PCB Layout Guidelines

Efficient PCB layout is critical for stable operation, good EMI, and good thermal performance. For best results, refer to Figure 9 and follow the guidelines below.

1) Minimize the loop area formed by the input capacitor, IC, freewheeling diode, inductor, and output capacitor.
2) Place the power inductor far away from the input filter while keeping the loop area to the inductor at a minimum.
3) Place a capacitor valued at several hundred pF between FB and SOURCE as close to the IC as possible.
4) Connect the exposed pads or large copper area with DRAIN to improve thermal performance.




**Top Layer**




**Bottom Layer**

**Figure 9: Recommended Layout**

## Design Example

Table 2 shows a design example for the following application guideline specifications.

**Table 2: Design Example**

| | |
|---|---|
| $V_{IN}$ | $85V_{AC}$ to $265V_{AC}$ |
| $V_{OUT1}$ | 12V |
| $I_{OUT1}$ | 200mA |
| $V_{OUT2}$ | 5V |
| $I_{OUT2}$ | 50mA |

The detailed application schematic is shown in Figure 10. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section. For additional device applications, please refer to the related evaluation board datasheets.

## TYPICAL APPLICATION CIRCUIT

Figure 10 shows a typical application example of a 12V/200mA and 5V/50mA non-isolated power supply using the MP163CGS-5.

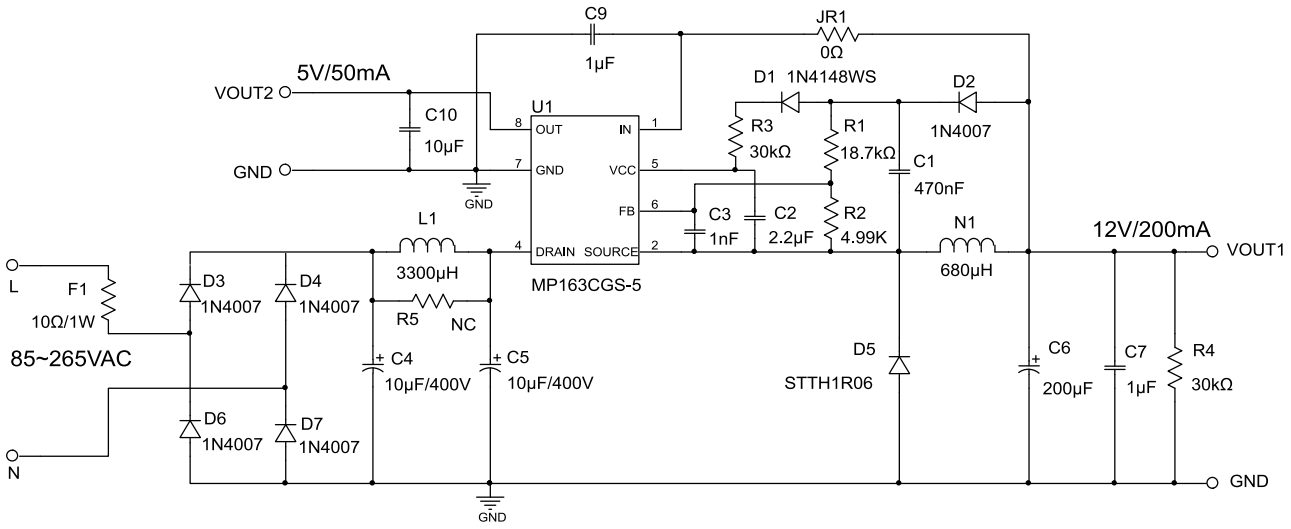
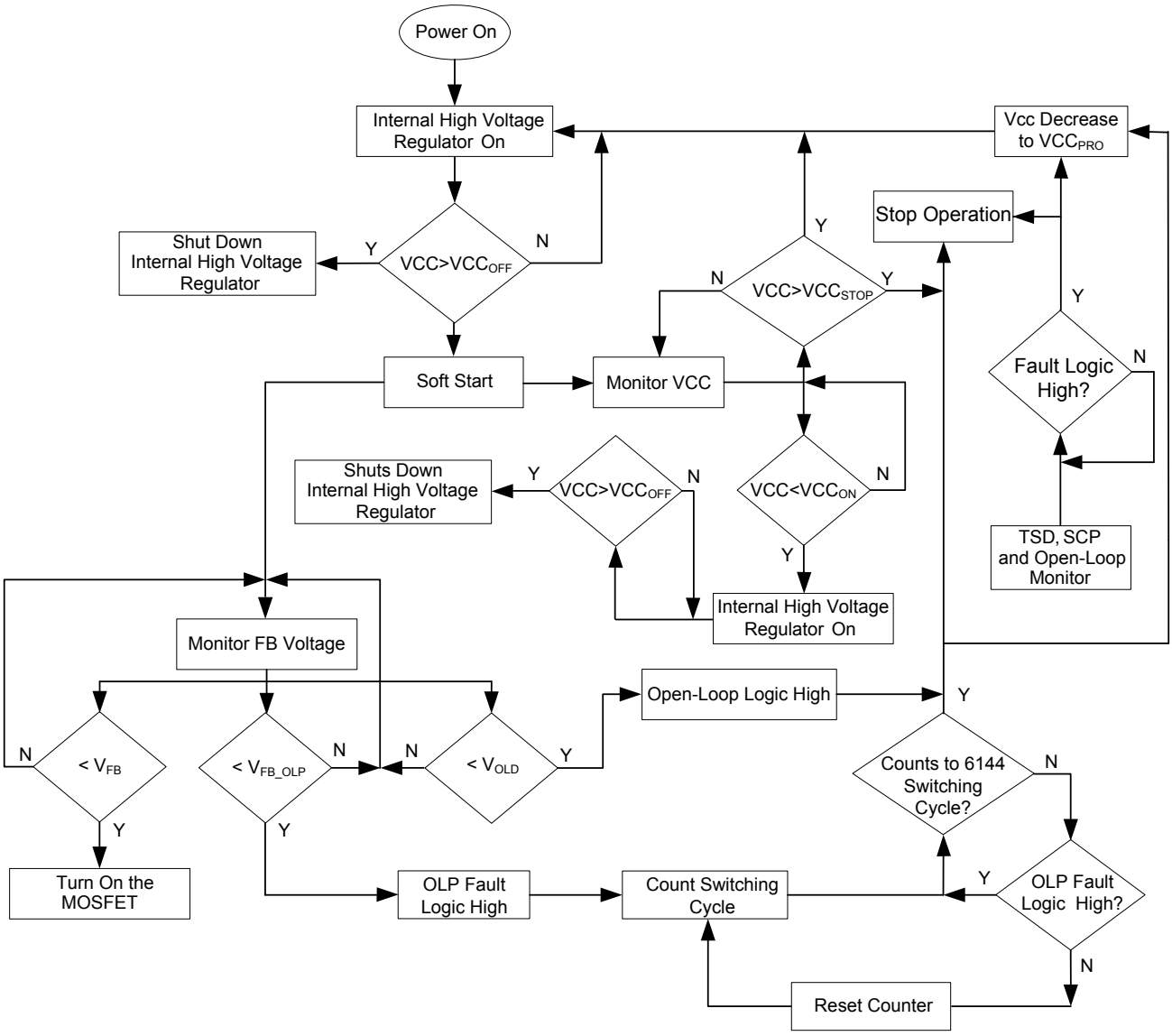



**Figure 10: Typical Application at 12V/200mA and 5V/50mA**

## FLOW CHART




UVLO, SCP, OLP, OTP and Open-Loop Protections are Auto Restart

**Figure 11: Control Flow Chart**

## SIGNAL SEQUENCE

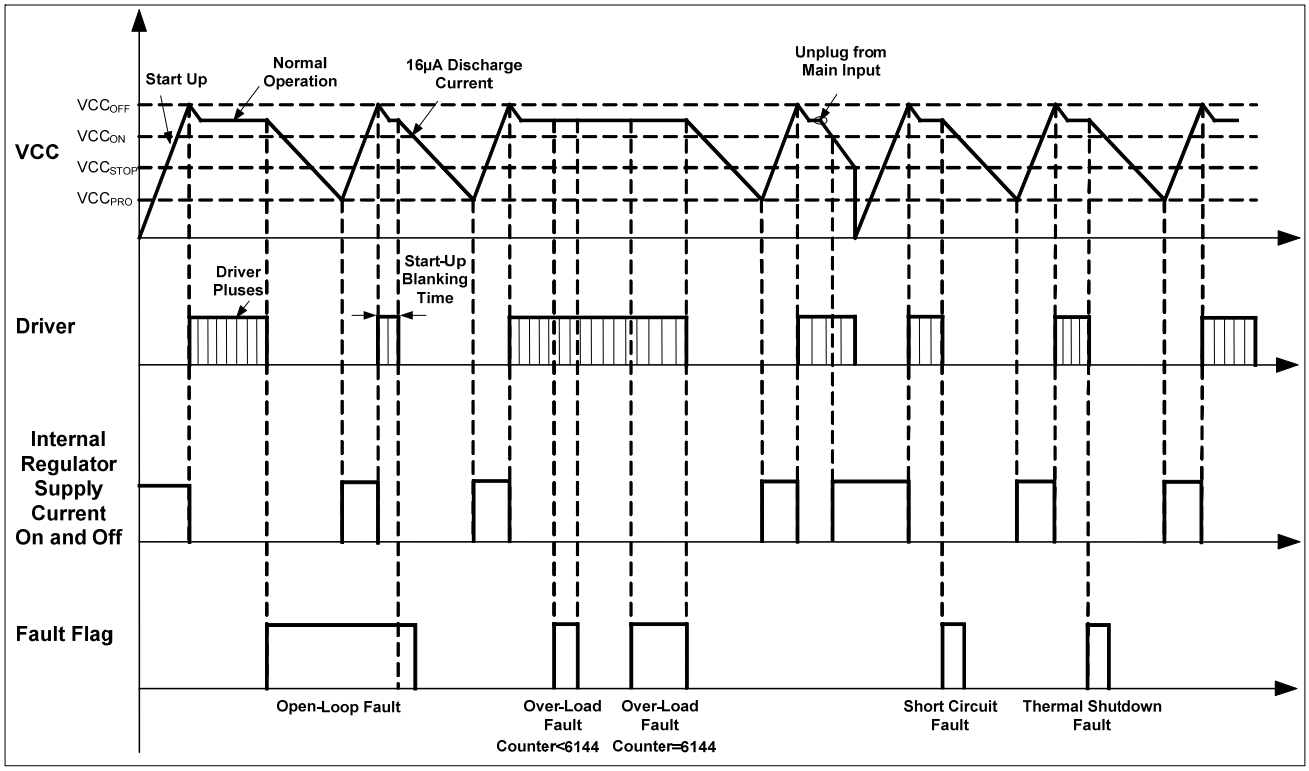
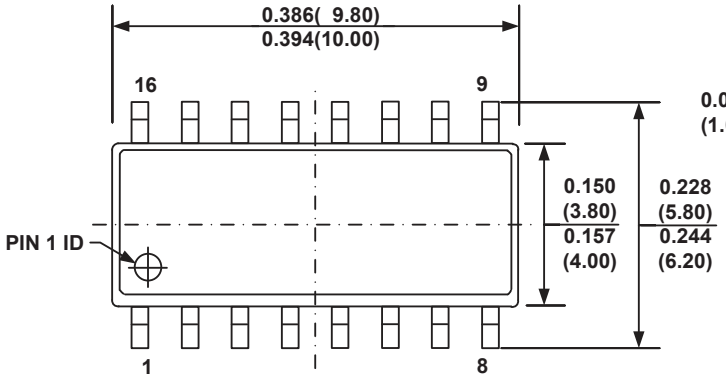


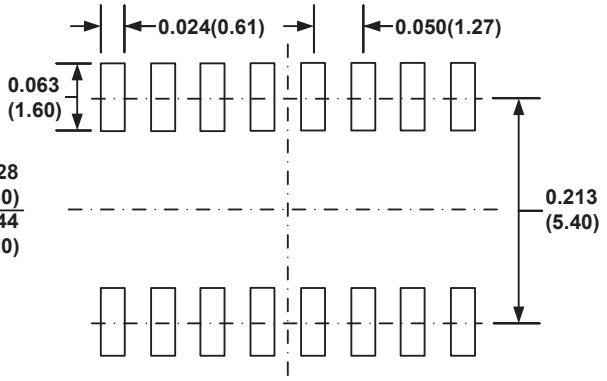

**Figure 11: Signal Evolution in the Presence of a Fault**

## PACKAGE INFORMATION

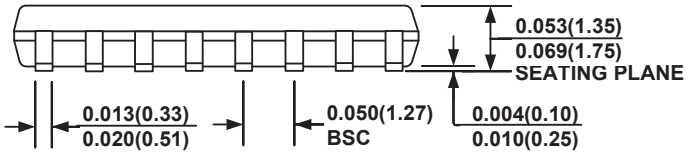
**SOIC16**



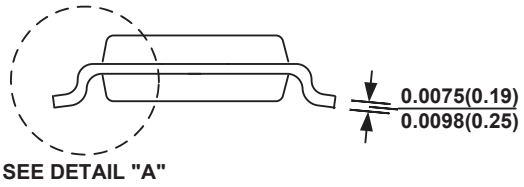

**TOP VIEW**



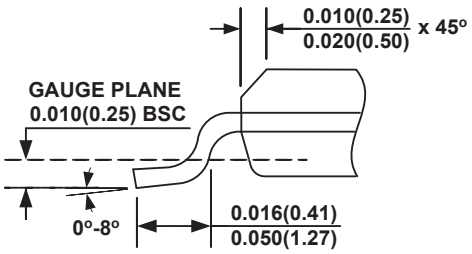

**RECOMMENDED LAND PATTERN**




**FRONT VIEW**




**SIDE VIEW**



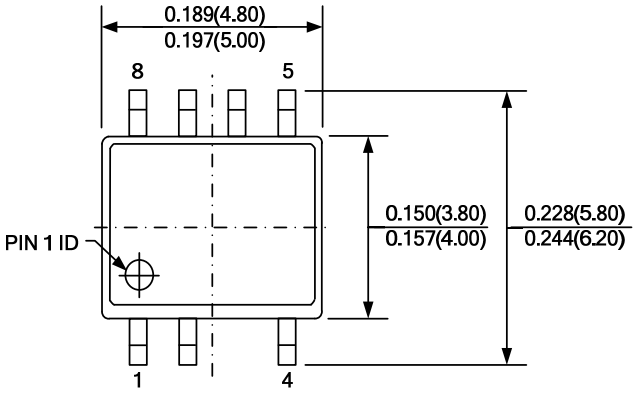

**DETAIL "A"**

**NOTE:**

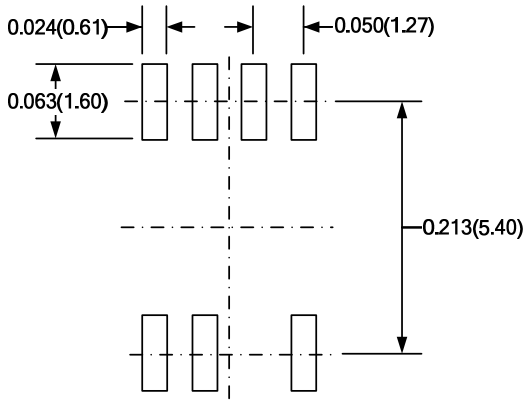
1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AC.
6) DRAWING IS NOT TO SCALE.

## PACKAGE INFORMATION *(continued)*

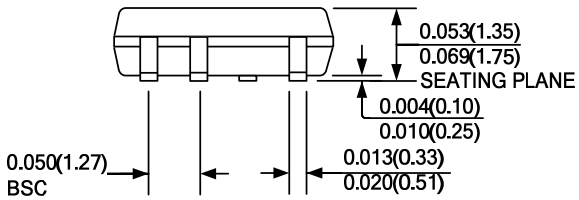
**SOIC8-7B**



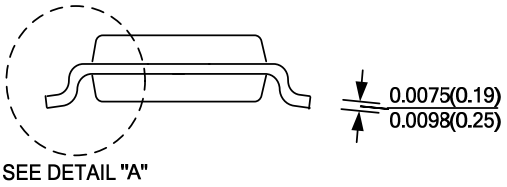

TOP VIEW



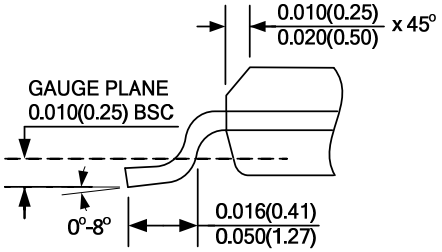

RECOMMENDED LAND PATTERN




FRONT VIEW




SIDE VIEW

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5) JEDEC REFERENCE IS MS-012.
6) DRAWING IS NOT TO SCALE.