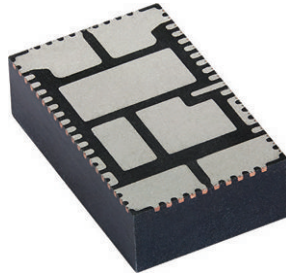


## 4.5 V to 20 V Input, 25 A microBRICK® DC/DC Regulator Module With PMBus Interface



Top view



Bottom view

### LINKS TO ADDITIONAL RESOURCES



### DESCRIPTION

The SiC951 is a PMBus 1.3 compliant non-isolated DC/DC buck regulator module with integrated MOSFETs and inductor in a 10.6 mm x 6.5 mm x 3 mm thermally efficient package. It is capable of supplying 25 A continuously with 30 A peak. Its output voltage is digitally adjustable from 0.3 V to 5.5 V from a 4.5 V to 20 V input with switching frequencies up to 1.5 MHz. The SiC951 can accommodate a variety of applications, including computing, consumer electronics, telecom, and industrial.

SiC951 architecture delivers ultrafast transient response with minimum output capacitance and tight regulation over a broad load range. The device has integrated internal compensation and is stable with any type of output capacitor. The device incorporates a power saving scheme that significantly increases light load efficiency.

The SiC951 allows power block configuration programs to be stored in non volatile memory (NVM). Operation parameters such as  $V_{OUT}$ ,  $I_{OUT}$ , over temperature etc. can all be locally stored and used to determine fault behavior. Operation is firmware based and is field upgradable.

The SiC951 is available in lead (Pb)-free power enhanced MLP59-A6C package.

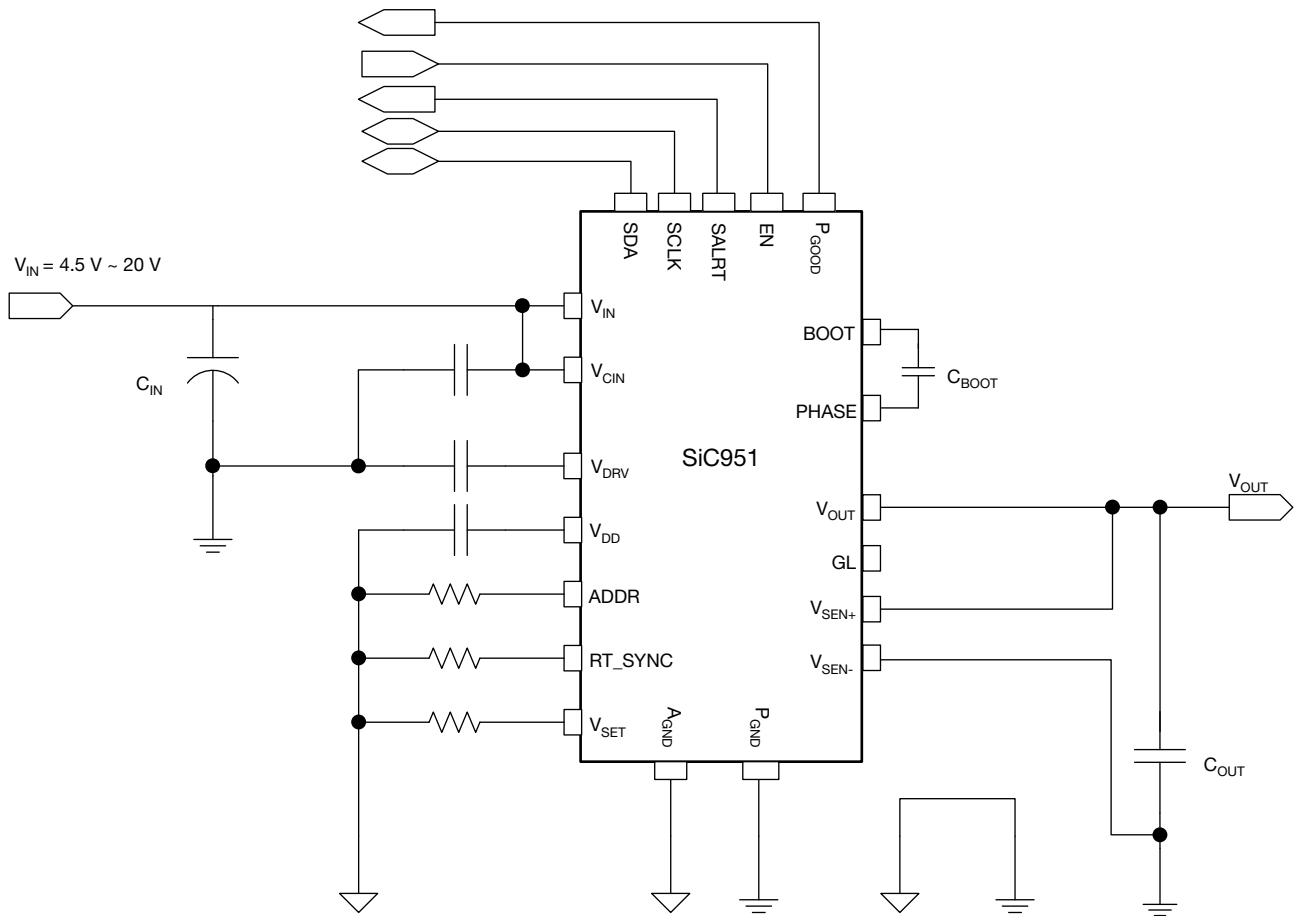
A full featured GUI and interface board is available to program and facilitate development of SiC951 based systems.

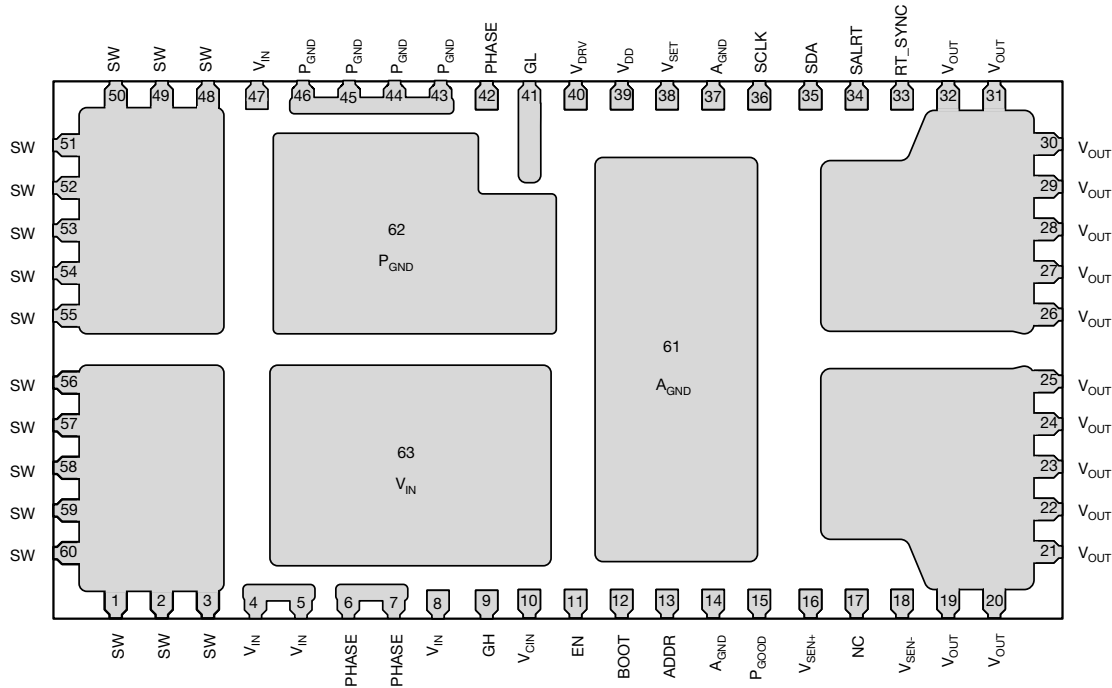
### FEATURES

- Versatile
  - Single supply operation from 4.5 V to 20 V input voltage
  - Output current: 25 A continuous with 30 A peak
  - Adjustable output voltage from 0.3 V to 5.5 V
  - Built in 5 V regulator for internal circuits and driver supply
  - 1 % output voltage accuracy over temperature
- Highly efficient
  - Close to 97 % peak efficiency
- Highly configurable
  - PMBus 1.3 compliant with 1 MHz bus speed
  - Internal NVM
  - $V_{OUT}$  adjustability and reading resolution of 2 mV
  - Supports over 50 PMBus commands
  - Ability to support sequential, tracking and simultaneous operation
  - Supports in phase or 180° out of phase synchronization
  - Output voltage source and sink capability
- Robust and reliable
  - $V_{IN}$ ,  $V_{OUT}$  and temperature reporting over PMBus
  - Over current protection in pulse-by-pulse mode
  - Output over voltage protection
  - Output under voltage protection
  - Over temperature protection with hysteresis
  - Dedicated enable pin for easy power sequencing
  - Power good open drain output
  - Remote sense amplifier with true differential voltage sensing
  - Ultrafast transient response
  - Optional power saving mode

### APPLICATIONS

- Servers
- Networking, telecom, storage applications
- Ultrabook, notebook, desktop
- Distributed point of load power architectures
- Storage applications
- DDR memory

**TYPICAL APPLICATION CIRCUIT**

**Fig. 1 - Typical Application Circuit**

**PIN CONFIGURATION**

**Fig. 2 - Pin Configuration - Transparent View**

| PIN DESCRIPTION  |                   |   |
|------------------|-------------------|---|
| PIN NUMBER       | SYMBOL            | DESCRIPTION   |
| 1 to 3, 48 to 60 | SW                | Switch node   |
| 4, 5, 8, 47, 63  | V <sub>IN</sub>   | Input voltage for power stage   |
| 6, 7, 42         | PHASE             | Phase node, return of high side gate driver   |
| 9                | GH                | High side gate signal for test purpose  |
| 10               | V <sub>CIN</sub>  | Input to the internal 5 V LDO. Connect this pin to V <sub>IN</sub> on PCB   |
| 11               | EN                | Enable pin. Active high   |
| 12               | BOOT              | Bootstrap voltage for high side gate driver   |
| 13               | ADDR              | PMBus address configuration pin   |
| 14, 37, 61       | A <sub>GND</sub>  | Analog ground   |
| 15               | P <sub>GOOD</sub> | Power good pin with open drain connection   |
| 16               | V <sub>SEN+</sub> | Positive input for output remote sense  |
| 17               | NC                | Leave this pin not connected  |
| 18               | V <sub>SEN-</sub> | Negative input for output remote sense  |
| 19 to 32         | V <sub>OUT</sub>  | Output voltage terminals  |
| 33               | RT_SYNC           | Clock synchronization pin. Frequency can be set by connecting a resistor to A <sub>GND</sub> . Pending on master / slave configuration, a clock can be send / receive via the pin |
| 34               | SALRT             | PMBus alert. Connect to external host interface if desired  |
| 35               | SDA               | PMBus data. Connect to external host interface  |
| 36               | SCLK              | PMBus clock. Connect to external host interface   |
| 38               | V <sub>SET</sub>  | Output voltage set point by connecting a resistor from V <sub>SET</sub> to A <sub>GND</sub>   |
| 39               | V <sub>DD</sub>   | Internal 5 V circuits supply voltage. V <sub>DD</sub> is a LDO output, connect a 1 μF decoupling capacitor to A <sub>GND</sub>  |
| 40               | V <sub>DRV</sub>  | Supply voltage for internal gate drive. V <sub>DRV</sub> is a LDO output. Connect a 4.7 μF decoupling capacitor to P <sub>GND</sub>   |
| 41               | GL                | Low side MOSFET gate monitor  |
| 43 to 46, 62     | P <sub>GND</sub>  | Power ground. Common return for internal MOSFETs  |

| ORDERING INFORMATION |   |                                    |                 |                                |          |               |                        |
|----------------------|---|------------------------------------|-----------------|--------------------------------|----------|---------------|------------------------|
| PART NUMBER          | PART MARKING                              | V <sub>DD</sub> , V <sub>DRV</sub> | LIGHT LOAD MODE | OPERATING JUNCTION TEMPERATURE | PACKAGE  | PACKAGING     | MINIMUM ORDER QUANTITY |
| SiC951ED-T1-GE3      | SiC951                                    | Internal                           | Power save mode | -40 °C to +125 °C              | MLP60-A6 | Tape and reel | 1050                   |
| SiC951ED-Y1-GE3      | SiC951                                    | Internal                           | Power save mode | -40 °C to +125 °C              | MLP60-A6 | Tray          | 210                    |
| SiC951EVB-A          | Reference board                           |                                    |                 |                                |          |               |                        |
| SiC951EVB-KIT-A      | Reference board kit with dongle and cable |                                    |                 |                                |          |               |                        |

**PART MARKING INFORMATION**

|    |             |                         |
|----|-------------|-------------------------|
|    | ●           | = pin 1 indicator       |
|    | P/N         | = part number code      |
|    |             | = Siliconix logo        |
|    |             | = ESD symbol            |
|    | F           | = assembly factory code |
|    | Y           | = year code             |
| WW | = week code |                         |
| LL | = lot code  |                         |

| ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted) |  |  |      |
|---|--|--|------|
| ELECTRICAL PARAMETER  | CONDITIONS                             | LIMITS                                     | UNIT |
| PV <sub>IN</sub> , V <sub>IN</sub>  | Reference to P <sub>GND</sub>          | -0.3 to +28                                | V    |
| SW / PH   | Reference to P <sub>GND</sub>          | -0.3 to +28                                |      |
| SW / PH (AC)  | Reference to P <sub>GND</sub> (100 ns) | -8 to +33                                  |      |
| BOOT  |  | -0.3 to V <sub>PH</sub> + V <sub>VCC</sub> |      |
| BOOT to SW  |  | -0.3 to +6                                 |      |
| Drive supply voltage (PV <sub>CC</sub> )                                  |  | -0.3 to +6                                 |      |
| Bias supply voltage (V <sub>DD</sub> )                                    |  | -0.3 to +6                                 |      |
| A <sub>GND</sub> to P <sub>GND</sub>                                      |  | -0.3 to +0.3                               |      |
| All other pins  | Reference to A <sub>GND</sub>          | -0.3 to V <sub>DD</sub> + 0.3              |      |
| <b>Temperature</b>  |  |  |      |
| Junction temperature  |  | -40 to +150                                | °C   |
| Storage temperature   |  | -65 to +150                                |      |
| <b>Power Dissipation</b>  |  |  |      |
| Junction-to-ambient thermal impedance (R <sub>thJA</sub> )                |  | 10   | °C/W |
| Thermal resistance from junction to case (R <sub>thJ-C</sub> )            |  | 2.5  |      |
| Thermal resistance from junction to PCB (R <sub>thJ-PCB</sub> )           |  | 5  |      |
| <b>ESD Protection</b>   |  |  |      |
| Electrostatic discharge protection  | HBM                                    | 2  | kV   |
|   | CDM                                    | 750  | V    |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating / conditions for extended periods may affect device reliability.

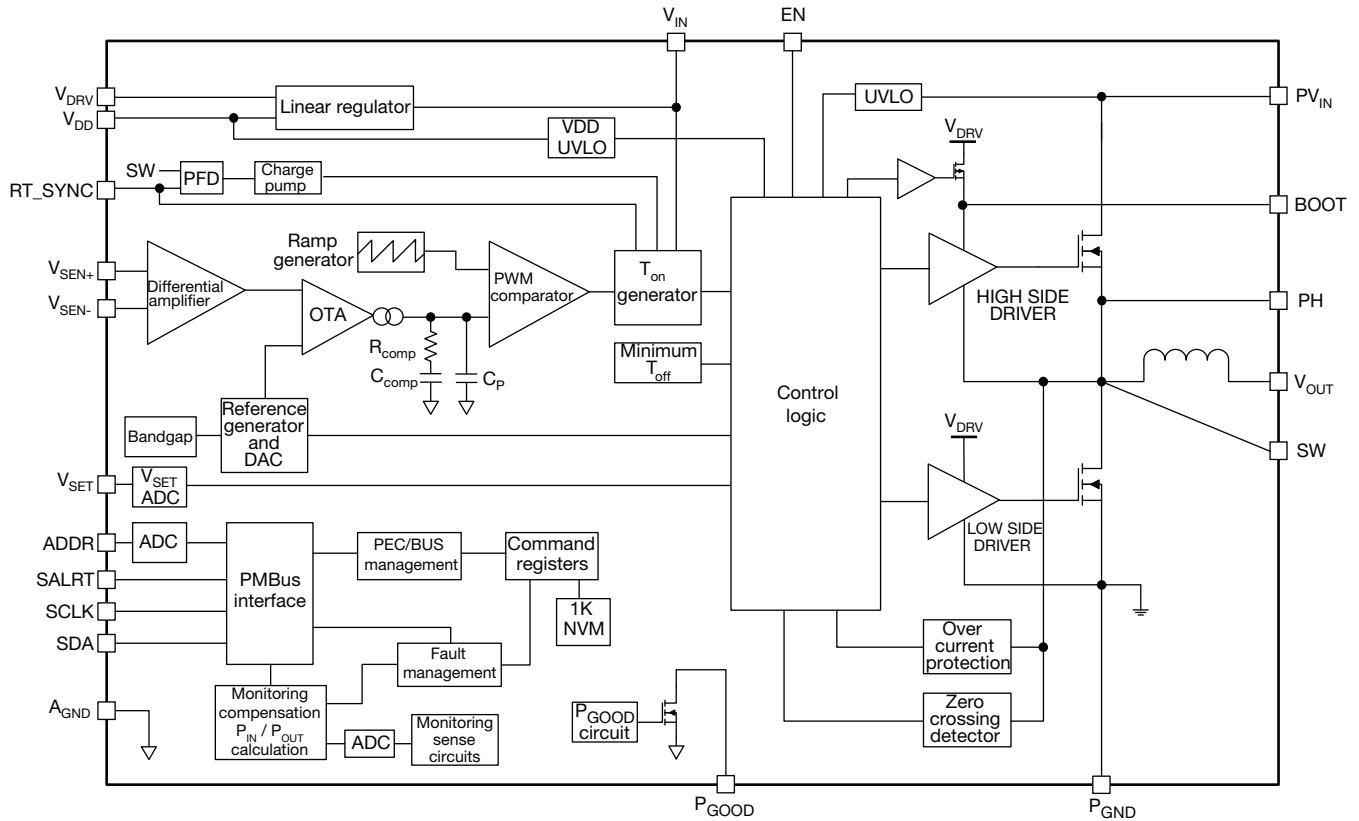


| <b>RECOMMENDED OPERATING CONDITIONS</b> (all voltages referenced to GND = 0 V) |             |      |      |      |
|--|-------------|------|------|------|
| ELECTRICAL PARAMETER   | MIN.        | TYP. | MAX. | UNIT |
| PV <sub>IN</sub> , V <sub>IN</sub>   | 4.5         | -    | 20   | V    |
| Logic pins   | 0           | -    | 5.5  |      |
| V <sub>OUT</sub>   | 0.3         | -    | 5.5  |      |
| Drive supply voltage (P <sub>VCC</sub> )                                       | 4.75        | 5    | 5.25 |      |
| Bias supply voltage (V <sub>DD</sub> )   | 4.75        | 5    | 5.25 |      |
| <b>Temperature</b>   |             |      |      |      |
| Recommended ambient temperature  | -40 to +85  |      |      | °C   |
| Operating junction temperature   | -40 to +125 |      |      |      |

| <b>ELECTRICAL SPECIFICATIONS</b> (PV <sub>IN</sub> = 12 V, T <sub>J</sub> = -40 °C to +125 °C, unless otherwise specified) |   |        |      |      |      |
|--|---|--------|------|------|------|
| PARAMETER  | TEST CONDITIONS   | LIMITS |      |      | UNIT |
|  |   | MIN.   | TYP. | MAX. |      |
| <b>Power Supplies</b>  |   |        |      |      |      |
| PV <sub>IN</sub> , V <sub>IN</sub>   |   | 4.5    | -    | 20   | V    |
| V <sub>IN_ON</sub>   | Default setting,<br>other settings may be programmed via PMBus  | -      | 10   | -    |      |
| V <sub>IN_OFF</sub>  | Default setting,<br>other settings may be programmed via PMBus  | -      | 9    | -    |      |
| PV <sub>CC</sub> supply  | V <sub>IN</sub> = 4.5 V to 20 V   | 4.5    | 5    | 5.5  |      |
| V <sub>DD</sub> supply   | Logic supply voltage  | 4.5    | 5    | 5.5  |      |
| PV <sub>CC</sub> UVLO threshold  |   | 3.4    | 3.6  | 3.8  |      |
| PV <sub>CC</sub> UVLO hysteresis   |   | -      | 300  | -    |      |
| Input current  | T <sub>J</sub> = 25 °C, non-switching, no load, V <sub>FB</sub> > 0.5 V,<br>I <sub>PVCC</sub> + I <sub>PVDD</sub> + I <sub>PVIN</sub> | -      | -    | 1    | mA   |
| Shutdown current   | EN = 0 V, I <sub>PVCC</sub> + I <sub>PVDD</sub> + I <sub>PVIN</sub>   | -      | -    | 1    |      |
| <b>PV<sub>IN</sub> Monitoring</b>  |   |        |      |      |      |
| PV <sub>IN</sub> monitor accuracy  |   | -      | 5    | -    | %    |
| PV <sub>IN</sub> min. monitor resolution   |   | -      | 70   | -    | mV   |
| PV <sub>IN</sub> monitor full scale  |   | -      | 30   | -    | V    |
| PV <sub>IN</sub> read frequency  |   | -      | 78   | -    | Hz   |
| <b>PV<sub>IN</sub> Fault Response Time</b>   |   |        |      |      |      |
| Time to detect faults  | OV fault, UV fault (configurable)   | -      | 100  | -    | ns   |
| Time to set fault registers for faults   | OV warn, UV warn  | -      | 78   | -    | Hz   |
| <b>Output Voltage</b>  |   |        |      |      |      |
| V <sub>OUT</sub> set-point accuracy  | Measured as ΔV (V <sub>SEN+</sub> - V <sub>SEN-</sub> )   | -1     | -    | 1    | %    |
| V <sub>SEN+</sub> + common mode range  |   | -0.2   | -    | 12   | V    |
| V <sub>SEN-</sub> - common mode range  |   | -200   | -    | +200 | mV   |
| V <sub>OUT</sub> set-point range   | (Does not include margining)  | 0.3    | -    | 12   | V    |
| V <sub>OUT</sub> set-point resolution  |   | -      | 2    | -    | mV   |
| Line regulation  |   | -      | 0.4  | -    | %    |
| Load regulation  |   | -      | 0.2  | -    |      |
| V <sub>OUT</sub> monitor accuracy  | V <sub>OUT</sub> scale loop = 1   | -      | -    | 1    |      |
| V <sub>OUT</sub> min. monitor resolution   | V <sub>OUT</sub> scale loop = 1   | -      | 5    | -    | mV   |
| V <sub>OUT</sub> start up delay range  | From PV <sub>IN</sub> valid until 1 <sup>st</sup> PWM pulse   | 0      | -    | 127  | ms   |
| V <sub>OUT</sub> read conversion frequency   |   | -      | 78   | -    | Hz   |



| <b>ELECTRICAL SPECIFICATIONS</b> ( $PV_{IN} = 12\text{ V}$ , $T_J = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$ , unless otherwise specified) |   |        |         |      |                  |
|--|---|--------|---------|------|------------------|
| PARAMETER  | TEST CONDITIONS   | LIMITS |         |      | UNIT             |
|  |   | MIN.   | TYP.    | MAX. |                  |
| <b>Controller and Timing</b>   |   |        |         |      |                  |
| Minimum on-time  |   | -      | 50      | -    | ns               |
| $t_{ON}$ accuracy  |   | -10    | -       | 10   | %                |
| Frequency accuracy   | Default frequency is 600 kHz  | 540    | 600     | 660  | kHz              |
| Frequency setting range  | CCM mode  | 300    | -       | 1500 |                  |
| Minimum off-time   |   | -      | 250     | -    | ns               |
| <b><math>V_{OUT}</math> Soft Start / Soft Stop</b>   |   |        |         |      |                  |
| $t_{ON\_RISE}$   | From $V_{OUT} = 0\text{ V}$ to $V_{OUT}$ set point  | 0      | -       | 127  | ms               |
| $t_{ON\_DELAY}$  | From ON_OFF_CONFIG invoked until $V_{OUT}$ set point  | 0      | -       | 127  |                  |
| $t_{OFF\_FALL}$  | From the end of the turn-off delay time until the voltage is commanded to zero $I_{OUT\_OC\_FAULT\_LIMIT}$ current must not be exceeded | 0      | -       | 127  |                  |
| $t_{OFF\_DELAY}$   | From ON_OFF_CONFIG invoked until $V_{OUT} = 0\text{ V}$   | 0      | -       | 127  |                  |
| <b><math>V_{OUT}</math> Faults</b>   |   |        |         |      |                  |
| Time to detect and set fault registers for $V_{OUT}$ faults  | OV warn, OV fault, (configurable) ( $V_{OUT}$ UV warning and fault has 78 Hz filtering time)  | -      | 100     | -    | ns               |
| $t_{ON\_MAX\_FAULT\_LIMIT}$  | Time to power up the output without reaching the output under voltage fault limit   | 0      | -       | 127  | ms               |
| $t_{OFF\_MAX\_WARN\_LIMIT}$  | Time to power down the output without reaching 12.5 % of $V_{OUT}$ set point  | 0      | -       | 127  |                  |
| <b>Power Good</b>  |   |        |         |      |                  |
| Power good output threshold  | $V_{OUT}$ rising (default value, can be changed by PMBus)   | -      | 90      | -    | %                |
|  | $V_{OUT}$ falling (default value, can be changed by PMBus)  | -      | 85      | -    |                  |
| Power good hysteresis  | Default rising and falling thresholds   | -      | 5       | -    |                  |
| Power good on resistance   |   | -      | 5.5     | -    | $\Omega$         |
| Power good delay time (rising)   |   | -      | 25      | -    | $\mu\text{s}$    |
| Power good delay time (falling)  |   | -      | 30      | -    |                  |
| <b>Temperature Monitor and Temperature Shutdown</b>  |   |        |         |      |                  |
| Resolution   |   | -      | 1       | -    | $^\circ\text{C}$ |
| Range  |   | -40    | -       | 150  |                  |
| Accuracy   |   | -      | $\pm 5$ | -    |                  |
| Thermal shutdown   |   | -      | 125     | -    |                  |
| Thermal shutdown hysteresis  |   | -      | 35      | -    |                  |
| <b>Digital Inputs</b>  |   |        |         |      |                  |
| <b>ADDR, SALRT, SCLK, SDA, EN</b>  |   |        |         |      |                  |
| $V_{IH}$   | Input high threshold  | 2      | -       | -    | V                |
| $V_{IL}$   | Input low threshold   | -      | -       | 0.8  |                  |
| $V_{HYST}$   | Input hysteresis  | -      | 0.1     | -    |                  |
| $C_{PIN}$  | Input C   | -      | 5       | -    |                  |

**FUNCTIONAL BLOCK DIAGRAM**

**Fig. 3 - Functional Block Diagram**



| PMBus COMMAND |                  |               |  |              |         |               |              |  |
|---------------|------------------|---------------|--|--------------|---------|---------------|--------------|--|
| COMM. CODES   | PMBus COMMANDS   | COMM. STRUCT. | DESCRIPTION  | # DATA BYTES | DEFAULT | DEFAULT VALUE | EXP. (FIXED) | VALID VALUES                                 |
| 0x00          | Page             |               |  | 119          |         |               |              |  |
| 0x01          | OPERATION        | Byte          | Set the operation mode, on / off and margining bit 7 set to 1: ON, 0: OFF<br>bit 6 set to<br>1: use TOFF_DELAY setting<br>0: fast turn off<br>bit 5 and 4 output setting<br>00: VOUT_COMMAND<br>01: VOUT_MARGIN_LOW<br>10: VOUT_MARGIN_HIGH<br>11: AVS (disabled)<br>bit 3 and 2 fault setting, in case VOUT_MARGIN_LOW/HIGH exceed VOUT_OV/UV_FAULT_LIMIT<br>01: ignore<br>10: alert according to VOUT_OV/UV_FAULT_RESPONSE<br>bit 0 and 1 NA | 1            | 0x88    |               |              |  |
| 0x02          | ON_OFF_CONFIG    | Byte          | Sets the ON / OFF behavior<br>bit 4 - power up, set to<br>1: according to OPERATION<br>0: when power is present<br>bit 3 - PMBUS OPERATION<br>0: ignore ON / OFF<br>1: use ON / OFF<br>bit 2 - CONTROL pin<br>0: ignore CONTROL<br>1: use CONTROL<br>bit 1 - control pin polarity<br>0: active low<br>1: active high<br>bit 0 - turn OFF delay and fall time<br>0: use settings<br>1: fast   | 1            | 0x1F    |               |              |  |
| 0x03          | CLEAR_FAULTS     | Send byte     | Clears all faults and SMB_ALERT<br>If device is still in fault mode it will alert again does not release from latch condition.   | 1            |         |               |              |  |
| 0x10          | WRITE_PROTECT    | Byte          | Set the write protection   | 1            | 0x00    |               |              |  |
| 0x15          | STORE_USER_ALL   | Send byte     | Stores all user registers to NVM   | 1            |         |               |              |  |
| 0x16          | RESTORE_USER_ALL | Send byte     | Restores all user registers from NVM   | 1            |         |               |              |  |
| 0x19          | CAPABILITY       | Byte          | Sets capabilities of PMBUS<br>bit 7 - PEC<br>1: enable<br>bit 6 and 5 - bus speed:<br>10: 1 MHz<br>bit 4 - SMB_ALERT<br>1: pin available<br>bit 3 - numeric format<br>0: linear<br>bit 2 - AVSBUS<br>0: no   | 1            | 0xD0    |               |              | PEC<br>(ON / OFF)<br>SMB_ALERT<br>(ON / OFF) |
| 0x1b          | SMBALERT_MASK    | Block         | SMBALERT mask vectors:<br>NVM / registers<br>2 bytes - 1 <sup>st</sup> :<br>STATUS_x command code,<br>2 <sup>nd</sup> : mask byte (retrieve mask data is elaborated in spec)   | 7            |         |               |              |  |





| PMBus COMMAND |                        |               |   |              |         |                       |              |                            |
|---------------|------------------------|---------------|---|--------------|---------|-----------------------|--------------|----------------------------|
| COMM. CODES   | PMBus COMMANDS         | COMM. STRUCT. | DESCRIPTION   | # DATA BYTES | DEFAULT | DEFAULT VALUE         | EXP. (FIXED) | VALID VALUES               |
| 0x20          | VOUT_MODE              | Byte          | Sets V <sub>OUT</sub> format<br>bit 7<br>0: absolute<br>1: relative<br>bit 6 and 5<br>00: ULINEAR16 / SLINEAR16<br>01: VID<br>10: direct<br>11: IEEE half precision FP<br>bit 4, 3, and 2<br>ULINEAR16 : N<br>(X = VOUT_COMMANDx2^N) = -9 (10111)<br>VID: VID code type<br>Direct: 00000<br>IEEE: 00000 | 1            | 0x17    | -9                    |              |                            |
| 0x21          | VOUT_COMMAND           | Word          | Sets V <sub>OUT</sub> (V)<br>2 bytes SLINEAR16  | 2            | 0x0133  | 0.6                   | -9           | 0.3-14                     |
| 0x22          | VOUT_TRIM              | Word          | User trimming offset to be added in SLINEAR16 format (2's complement) (V)<br>2 bytes SLINEAR16  | 2            | 0x0000  | 0                     | -9           | (-2)-2                     |
| 0x24          | VOUT_MAX               |               | Sets maximum V <sub>OUT</sub> for alert and limiting V <sub>OUT</sub> (V)<br>2 bytes SLINEAR16  | 2            | 0x1C00  | 14                    | -9           | 0.3-14                     |
| 0x25          | VOUT_MARGIN_HIGH       | Word          | 5 %<br>Set the MARGIN HIGH voltage<br>2 bytes SLINEAR16   | 2            | 0x0142  | 0.63                  | -9           | 0.3-14                     |
| 0x26          | VOUT_MARGIN_LOW        | Word          | -5 %<br>Set the MARGIN LOW voltage<br>2 bytes SLINEAR16 11  | 2            | 0x0123  | 0.57                  | -9           | 0.3-14                     |
| 0x27          | VOUT_TRANSITION_RATE   | Word          | Sets the slew rate in mV/μs<br>2 bytes ULINEAR11  | 2            | 0xE002  | 0.125                 | -4           | 0.0625-2                   |
| 0x29          | VOUT_SCALE_LOOP        | Word          | Sets the V <sub>OUT</sub> /FB ratio in digital mode<br>2 bytes SLINEAR11, 0.125,0.25, 0.5, 1 allowed  | 2            | 0xE808  | 1                     | -3           | 0.125, 0.25, 0.5, 1        |
| 0x33          | FREQUENCY_SWITCH       | Word          | Switching frequency: (kHz)<br>2 bytes LINEAR11,<br>(200K to 1500K, 50K steps)   | 2            | 0x0258  | 600                   | 0            | 300K to 1500K, 50K steps   |
| 0x35          | VIN_ON                 | Word          | V <sub>IN</sub> in which the device starts<br>2 bytes SLINEAR11   | 2            | 0xF814  | 10                    | -1           | 1-80                       |
| 0x36          | VIN_OFF                | Word          | V <sub>IN</sub> in which the device stops<br>2 bytes SLINEAR11  | 2            | 0xF812  | 9                     | -1           | 1-80                       |
| 0x37          | Interleave             | Word          | Set master / slave clock 0° or 180° out of phase. See INTERLEAVE description for detail   | 2            | 0x0000  | 0                     |              | See INTERLEAVE description |
| 0x40          | VOUT_OV_FAULT_LIMIT    | Word          | Sets the OVP DAC level above V <sub>OUT</sub> in digital mode<br>Default analog = 115 % V <sub>OUT</sub><br>2 bytes SLINEAR16   | 2            | 0x0161  | 0.69                  | -9           | 0.3-14                     |
| 0x41          | VOUT_OV_FAULT_RESPONSE | Word          | Bit 7, 6 to 11:<br>shut down until fault is disabled<br>bit 3, 4, and 5 - 111:<br>restart continuously<br>bit 0, 1, and 2 - 000:<br>no delay  | 1            | 0xF8    | According to settings |              | All                        |
| 0x42          | VOUT_OV_WARN_LIMIT     | Word          | Telemetry warn limit (V)<br>2 bytes SLINEAR16   | 2            | 0x0151  | 0.66                  | -9           | 0.3-14                     |
| 0x43          | VOUT_UV_WARN_LIMIT     | Word          | Telemetry warn limit (V)<br>2 bytes SLINEAR16   | 2            | 0x0114  | 0.54                  | -9           | 0-14                       |



| PMBus COMMAND |                        |               |  |              |         |                                  |              |   |
|---------------|------------------------|---------------|--|--------------|---------|----------------------------------|--------------|---|
| COMM. CODES   | PMBus COMMANDS         | COMM. STRUCT. | DESCRIPTION  | # DATA BYTES | DEFAULT | DEFAULT VALUE                    | EXP. (FIXED) | VALID VALUES                                |
| 0x44          | VOUT_UV_FAULT_LIMIT    | Word          | Sets the UVP in digital mode (V)<br>Default analog = 20 % V <sub>OUT</sub><br>2 bytes SLINEAR16  | 2            | 0x00F5  | 0.48                             | -9           | 0-14  |
| 0x45          | VOUT_UV_FAULT_RESPONSE | Byte          | Bit 7 and 6 - 10:<br>shut down with hiccup<br>bit 3, 4, and 5 - 111:<br>restart continuously<br>bit 0, 1, and 2 - 001:<br>delay 20 ms  | 1            | 0xB9    | According to settings            |              | All   |
| 0x46          | IOUT_OC_FAULT_LIMIT    | Word          | Cycle by cycle temperature compensated OCP detector (A)<br>2 bytes LINEAR11 exp. -1  | 2            | 0xF83C  | 30                               | -1           | 0-127                                       |
| 0x47          | IOUT_OC_FAULT_RESPONSE | Byte          | Bit 7 and 6 - 10:<br>Continue for number of pulses set by event count than hiccup forever<br>bit 3, 4, and 5 - 100:<br>128 OCP counts<br>bit 0, 1, and 2 - 001:<br>delay 20 ms | 1            | 0xA1    | According to settings            |              | All   |
| 0x4f          | OT_FAULT_LIMIT         | Word          | Over temperature limit (°C),<br>35 °C hysteresis<br>2 bytes LINEAR11 exp. -1   | 2            | 0x007D  | 125                              | 0            | 0-150                                       |
| 0x50          | OT_FAULT_RESPONSE      | Byte          | Bit 7 and 6 - 10:<br>shut down with hiccup<br>bit 3, 4, and 5 - 111:<br>restart continuously<br>bit 0, 1, and 2 - 001:<br>delay 20 ms  | 1            | 0xB9    | According to settings            |              | All   |
| 0x51          | OT_WARN_LIMIT          | Word          | Telemetry warn limit (°C)<br>2 bytes LINEAR11 exp. 0   | 2            | 0x0069  | 105                              | 0            | 0-150                                       |
| 0x55          | VIN_OV_FAULT_LIMIT     | Word          | V <sub>IN</sub> OV fault limit (V)<br>2 bytes LINEAR11   | 2            | 0xF81E  | 15                               | -1           | 1-80  |
| 0x56          | VIN_OV_FAULT_RESPONSE  | Byte          | Bit 7 and 6 - 10:<br>shut down with hiccup<br>bit 3, 4 and 5 - 111:<br>restart continuously<br>bit 0, 1, and 2 - 000:<br>no delay  | 1            | 0xB8    | According to settings            |              | All   |
| 0x58          | VIN_UV_WARN_LIMIT      | Word          | Telemetry warn limit (V)<br>2 bytes LINEAR11   | 2            | 0xF812  | 9                                | -1           | 1-80  |
| 0x5e          | POWER_GOOD_ON          | Word          | POWER GOOD high threshold (V)<br>2 bytes SLINEAR16   | 2            | 0x0123  | 0.57                             | -9           | 0.24-14                                     |
| 0x5F          | POWER_GOOD_OFF         | Word          | POWER GOOD low threshold (V)<br>2 bytes SLINEAR16  | 2            | 0x0114  | 0.54                             | -9           | 0.24-14                                     |
| 0x60          | TON_DELAY              | Word          | Delay from ON (ms)<br>2 bytes LINEAR11   | 2            | 0x0000  | 0                                | 0            | 0-127                                       |
| 0x61          | TON_RISE               | Word          | Rise time (ms)<br>2 bytes LINEAR11   | 2            | 0x0005  | 5                                | 0            | 0-127                                       |
| 0x62          | TON_MAX_FAULT_LIMIT    | Word          | Time until UV/PGOOD is reached (ms)<br>Selectable by MFR_OP_MODE<br>2 bytes LINEAR11   | 2            | 0x0014  | 20                               | 0            | 0-127                                       |
| 0x63          | TON_MAX_FAULT_RESPONSE | Byte          | Bit 7 and 6 - 10:<br>shut down with hiccup<br>bit 3, 4, and 5 - 000:<br>no restart until faults cleared by user (latched)<br>bit 0, 1, and 2 - 001:<br>delay 20 ms             | 1            | 0x81    | Shutdown until fault is disabled |              | Shutdown / shutdown until fault is disabled |
| 0x64          | TOFF_DELAY             | Word          | Delay from OFF (ms)<br>2 bytes LINEAR11  | 2            | 0x0000  | 0                                | 0            | 0-127                                       |



| PMBus COMMAND |                     |               |  |              |         |               |              |              |
|---------------|---------------------|---------------|--|--------------|---------|---------------|--------------|--------------|
| COMM. CODES   | PMBus COMMANDS      | COMM. STRUCT. | DESCRIPTION  | # DATA BYTES | DEFAULT | DEFAULT VALUE | EXP. (FIXED) | VALID VALUES |
| 0x65          | TOFF_FALL           | Word          | Fall time (ms)<br>2 bytes LINEAR11   | 2            | 0x0005  | 5             | 0            | 0-127        |
| 0x66          | TOFF_MAX_WARN_LIMIT | Word          | Time until 12.5 % is reached (ms)<br>2 bytes LINEAR11                                      | 2            | 0x003C  | 60            | 0            | 0-127        |
| 0x78          | STATUS_BYTE         | Byte          | 1 byte   | 1            |         |               |              |              |
| 0x79          | STATUS_WORD         | Word          | 2 bytes  | 1            |         |               |              |              |
| 0x7a          | STATUS_VOUT         | Byte          | 1 byte   | 1            |         |               |              |              |
| 0x7b          | STATUS_IOUT         | Byte          | 1 byte   | 1            |         |               |              |              |
| 0x7c          | STATUS_INPUT        | Byte          | 1 byte   | 1            |         |               |              |              |
| 0x7d          | STATUS_TEMPERATURE  | Byte          | 1 byte   | 1            |         |               |              |              |
| 0x7e          | STATUS_CML          | Byte          | 1 byte   | 1            |         |               |              |              |
| 0x80          | STATUS_MFR_SPECIFIC | Byte          |  | 1            |         |               |              |              |
| 0x88          | READ_VIN            | Word          | V <sub>IN</sub> (V)<br>2 bytes LINEAR11  | 2            |         |               | -4           | 0-80         |
| 0x8b          | READ_VOUT           | Word          | V <sub>OUT</sub> (V)<br>2 bytes LINEAR16   | 2            |         |               | -9           | 0-48         |
| 0x8d          | READ_TEMPERATURE    | Word          | Temperature (°C)<br>2 bytes ULINEAR11  | 2            |         |               | 0            | (-50)-150    |
| 0x94          | READ_DUTY_CYCLE     | Word          | Duty-cycle (t <sub>on</sub> / t <sub>on</sub> + t <sub>off</sub> ) (%)<br>2 bytes LINEAR11 | 2            |         |               | -4           | 0-100        |
| 0x98          | PMBUS_REVISION      | Byte          | 1 byte   | 1            | 0x33    |               |              |              |
| 0x99          | MFR_ID              | Block         | 3 bytes  | 3            | 0x00    |               |              |              |
| 0x9a          | MFR_MODEL           | Block         | 2 bytes  | 2            | 0x00    |               |              |              |
| 0x9b          | MFR_REVISION        | Block         | 2 bytes  | 2            | 0x00    |               |              |              |
| 0x9e          | MFR_SERIAL          | Block         |  | 2            |         |               |              |              |
| 0xad          | IC_DEVICE_ID        | Block         | 2 bytes  | 2            | 0x00    |               |              |              |
| 0xae          | IC_DEVICE_REV       | Block         | 2 bytes  | 2            | 0x00    |               |              |              |

**OPERATIONAL DESCRIPTION**

**Device Overview**

SiC951 is a high efficiency synchronous buck regulator capable of delivering up to 25 A continuous current. The device has programmable switching frequency of 300 kHz to 1.5 MHz. The control scheme delivers fast transient response and minimizes external components. Thanks to the internal current ramp information, no high ESR output bulk or virtual ESR network is required for the loop stability. This device also incorporates a power saving feature by enabling diode emulation mode and frequency fold back as the load decreases.

In addition, a built in PLL allows in phase or 180° out of phase synchronization under master / slave configuration.

SiC951 has a full set of protection and monitoring features with response that can be set with PMBus:

- Over current protection in pulse-by-pulse mode
- Output over voltage protection
- Output under voltage protection
- Over temperature protection with hysteresis
- Dedicated enable pin for easy power sequencing
- Power good open drain output

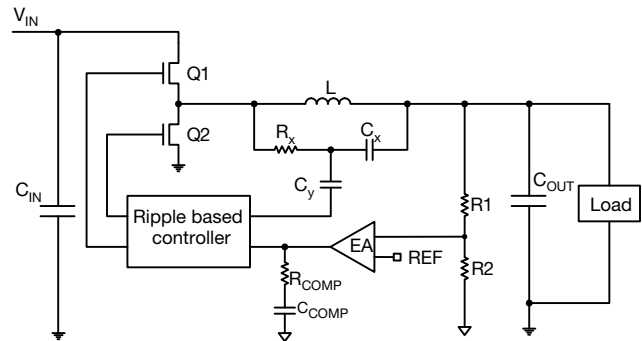
This device is available in MLP59-A6C package to deliver high power density and minimize PCB area.

**PWM Control Mechanism**

SiC951 employs a voltage - mode COT control mechanism. During steady-state operation, feedback voltage is compared with internal reference and the amplified error signal ( $V_{COMP}$ ) is generated in the internal comp node. An internally generated ramp signal and  $V_{COMP}$  are fed into a comparator. Once  $V_{RAMP}$  crosses  $V_{COMP}$ , a single shot on-time pulse is generated for a fixed time, programmed by the external  $R_{FSW}$ . During the on-time pulse, the high side MOSFET will be turned on. Once the on-time pulse expires, the low side MOSFET will be turned on after a break-before-make period. The low side MOSFET will be on for duration of minimum off-time pulse until  $V_{RAMP}$  crosses  $V_{COMP}$ . The cycle is then repeated.

Fig. 4 illustrates the basic block diagram for VM-COT architecture. In this architecture the following is achieved:

- The reference of a basic ripple control regulator is replaced with a high gain error amplifier loop
- This establishes two parallel voltage regulating feedback paths, a fast and slow path
- Fast path is the ripple injection which ensures rapid correction of the transient perturbation
- Slow path is the error amplifier loop which ensures the DC component of the output voltage follows the internal accurate reference voltage



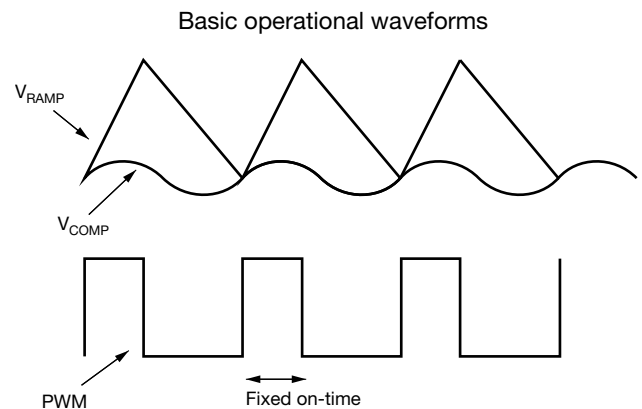
**Fig. 4 - VM-COT Block Diagram**

**Note**

- Control loop representation only, for simplicity remote sensing and output voltage setting not shown

All components for RAMP signal generation and error amplifier compensation required for the control loop are internal to the IC, see Fig. 4. In order for the device to cover a wide range of  $V_{OUT}$  operation, the internal RAMP signal components ( $R_x$ ,  $C_x$ ,  $C_y$ ) are automatically selected depending on the  $V_{OUT}$  voltage and switching frequency. This method allows the RAMP amplitude to remain constant throughout the  $V_{OUT}$  voltage range, achieving low jitter and fast transient response. The error amplifier internal compensation consists of a resistor in series with a capacitor ( $R_{COMP}$ ,  $C_{COMP}$ ).

Fig. 5 demonstrates the basic operational waveforms:



**Fig. 5 - VM-COT Operational Principle**

### Light Load Condition

To improve efficiency at light-load condition, SiC951 provide a set of innovative implementations to eliminate LS recirculating current and switching losses. The internal zero crossing detector monitors SW node voltage to determine when inductor current starts to flow negatively. In power saving mode, as soon as inductor valley current crosses zero, the device deploys diode emulation mode by turning off low side MOSFET. If load further decreases, switching frequency is reduced proportional to load condition to save switching losses while keeping output ripple within tolerance. The switching frequency is set by the controller to maintain regulation. In the standard power save mode, there is no minimum switching frequency. If ultrasonic mode is selected via PMBus, the minimum switching frequency that the regulator will reduce to is > 20 kHz as the part avoids switching frequencies in the audible range.

### Power Stage

SiC951 integrates a high performance power stage with a 4 mΩ n-channel high side MOSFET and a 1.4 mΩ n-channel low side MOSFET. The MOSFETs are optimized to achieve up to 96 % efficiency.

The power input voltage ( $PV_{IN}$ ) can go up to 20 V and down as low as 4.5 V. The output voltage must always be less than the input voltage.

### Sequencing of Input / Output Supplies

SiC951 has no sequencing requirements on any of its input / output,  $PV_{IN}$ ,  $PV_{CC}$ ,  $V_{IN}$ ,  $V_{DD}$  and EN.

### EN

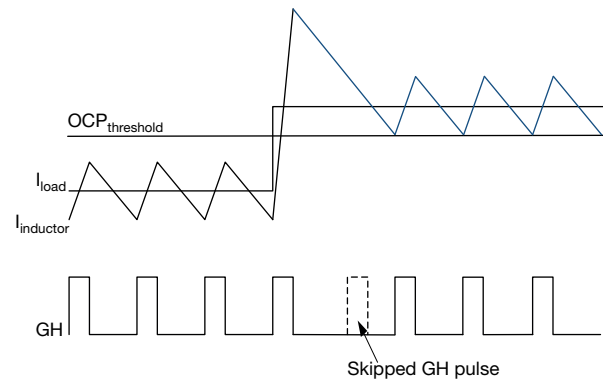
The SiC951 has an EN pin to turn the part on and off. Driving this pin high enables the device, while grounding it turns it off.

There are no sequencing requirements with respect to input / output supplies.

### Output Over-Current Protection (OCP)

SiC951 has pulse-by-pulse over-current limit control. The inductor valley current is monitored during LS FET turn-on period through  $R_{DS(on)}$  sensing. After a pre-defined blanking time, the valley current is compared with internal threshold to determine the over current limit threshold. This threshold can be programmed via PMBus. Default value is 30 A. If monitored current is higher than OCP threshold, HS turn-on pulse is skipped and LS FET is kept on until the valley current returns below OCP limit.

If the OCP persists for more than 128 consecutive cycles, the device latches off and stays off until the fault is cleared. OCP is enabled immediately after  $V_{CC}$  passes UVLO level.



**Fig. 6 - Over-Current Protection Illustration**

### Output Under-Voltage Protection (UVP)

UVP is implemented by monitoring the output voltage. If the output voltage drops below the target  $V_{OUT}$  by more than 20 %, the UVP event is recognized and both HS and LS MOSFETs are turned off. The fault must be cleared before the device can be restarted. Other fault responses may be programmed via PMBus (see PMBus command section).

UVP is only active after the completion of soft-start sequence.

### Output Over-Voltage Protection (OVP)

For OVP implementation, output is monitored through FB pin. After soft start, if the voltage level at FB is above 15 %, OVP is triggered with both the HS and LS MOSFETs turned off. The part can be re-started by cycling the EN pin or  $PV_{IN}$  supplies.

OVP is active immediately after  $V_{CC}$  passes UVLO level.

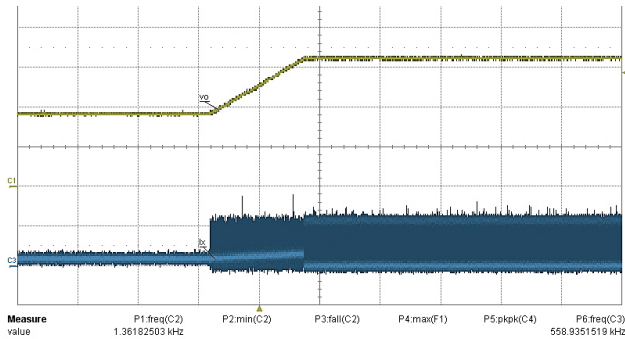
### Over-Temperature Protection (OTP)

SiC951 has internal thermal monitor block that turns off both HS and LS FETs when junction temperature is above 125 °C. The default PMBus setting for an OTP condition is for the device to stay off until the fault is cleared.

In case a retry is programmed via PMBus, a hysteresis of 35 °C is implemented, so when junction temperature drops below 90 °C, the device restarts by initiating soft-start sequence again.

### Pre-Bias Start-Up

In case of pre-bias start up, output is monitored through FB pin. If the sensed voltage on FB is higher than the internal reference ramp value, control logic prevents HS and LS FET from switching to avoid negative output voltage spike and excessive current sinking through LS FET.


**Fig. 7 - Pre-Bias Start-Up**

### Output Voltage Setting

Output voltage ( $V_{OUT}$ ) can be set by connecting a resistor from  $V_{SET}$  to  $A_{GND}$ . The resistor setting can be over-riden by a PMBus command. See below table for the list of output voltage ( $V_{OUT}$ ) set by the  $V_{SET}$  resistor value.

| OUTPUT VOLTAGE SETTING           |               |
|----------------------------------|---------------|
| $V_{SET}$ RESISTOR (k $\Omega$ ) | $V_{OUT}$ (V) |
| 0.845                            | 0.60          |
| 1.3                              | 0.90          |
| 1.78                             | 0.95          |
| 2.32                             | 1.00          |
| 2.87                             | 1.05          |
| 3.48                             | 1.20          |
| 4.12                             | 1.25          |
| 4.75                             | 1.50          |
| 5.49                             | 1.80          |
| 6.19                             | 2.10          |
| 6.98                             | 2.50          |
| 7.87                             | 3.30          |
| 8.87                             | 5.00          |
| 10                               | 5.00          |
| 11                               | 12            |
| 12.1                             | 0.60          |
| Short                            | 0.60          |

A missing or shorted resistor results in the part turning on with the minimum output voltage of 0.6 V. This allows for easy system debug.

### RT / SYNC PIN and Interleave Function Operation

The SiC951 has an RT / SYNC pin. This pin can be used to set the switching frequency and to send / receive a clock signal for synchronization between a master / slave. Connecting a resistor to ground will set the switching frequency according to the table listed below. If no resistor is connected to the RT / SYNC pin, the part will operate at the default frequency of 600 kHz. The default frequency as well as the frequency set by the external resistor, can be overridden by a PMBus command to a different operating frequency.

The following table shows the frequency settings by the RT resistor value.

| FREQUENCY SETTINGS        |                 |
|---------------------------|-----------------|
| RT RESISTOR (k $\Omega$ ) | FREQUENCY (kHz) |
| 0.845                     | 300             |
| 1.3                       | 400             |
| 1.78                      | 500             |
| 2.32                      | 550             |
| 2.87                      | 600             |
| 3.48                      | 650             |
| 4.12                      | 700             |
| 4.75                      | 750             |
| 5.49                      | 800             |
| 6.19                      | 850             |
| 6.98                      | 900             |
| 7.87                      | 950             |
| 8.87                      | 1000            |
| 10                        | 1250            |
| 11                        | 1500            |
| 12.1 (open)               | 600             |
| Short                     | 600             |

SiC951 supports in phase or 180° out of phase synchronization. There are 3 modes of configuration via PMBus.

#### 1. Master

- Mode of operation: determined by PMBus. As a master, it sends its internal clock out onto the RT / SYNC pin
- Operating frequency: frequency can either be the default frequency or programmed frequency via PMBus. If a part is designated as a master, switching frequency cannot be set using an external resistor. A clock signal will be sent via the RT / SYNC pin to the slave

#### 2. Slave

- Mode of operation: determined by PMBus. As a slave, the unit synchronizes its internal clock frequency either in phase or 180° out of phase as selected via the PMBus to the incoming clock applied at its RT / SYNC pin
- Operating frequency: the slave switching frequency will synchronize to the external clock or to the master clock. In case the external clock or master clock signal is lost, the slave will operate at the default frequency or to the frequency programmed via the PMBus; see Fig. 8.



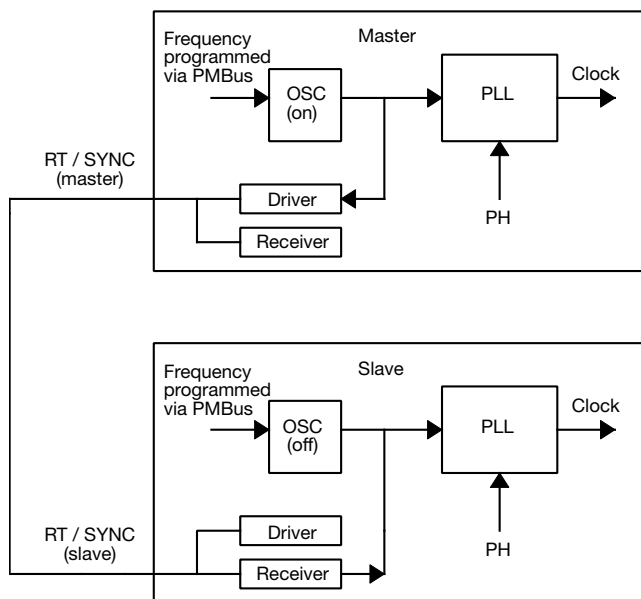


Fig. 8

If the user decides not to set the frequency of the slave via PMBus and also wants to have a frequency other than the default frequency, it is possible to program this by connecting a resistor between RT / SYNC and A<sub>GND</sub>. Additional component, diode and capacitor will be needed. This is illustrated in the Fig. 9:

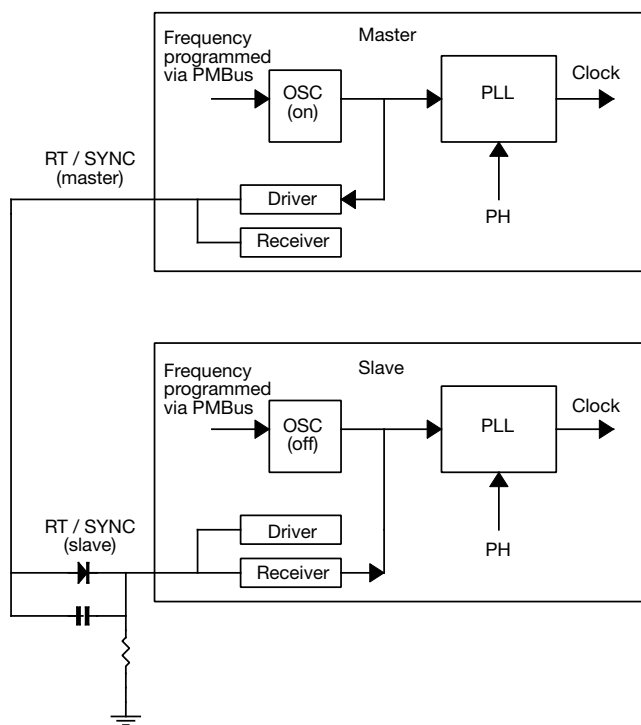


Fig. 9

### 3. Standalone Operation

- Mode of operation: determined by PMBus. The unit is neither master nor slave. It does not drive the RT / SYNC pin and it ignores any clock on RT / SYNC pin.
- Switching frequency: in standalone operation, the part will either operate at the default frequency of 600 kHz or at the frequency programmed by a resistor, both of which can be overridden by a PMBus command

In order to configure the part as a master, slave or standalone operation, the interleave will be used. The interleave command data bytes include three pieces of information:

1. A group identification number (4 bits)
2. The number of units in the group (4 bits)
3. The interleave order for this particular unit (4 bits). This number ranges in value from zero to one less than the number of units in the group

The group identification number allows for up to fifteen groups. Group Identification number 0 is reserved to mean not a member of an interleaved group. If the group identification number is 0, then the number of units in the group and the interleave order shall also be 0.

| BYTE          | HIGH BYTE |   |                 |   | LOW BYTE        |   |                  |   |   |   |   |   |   |   |   |   |
|---------------|-----------|---|-----------------|---|-----------------|---|------------------|---|---|---|---|---|---|---|---|---|
|               | 7         | 6 | 5               | 4 | 3               | 2 | 1                | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Contents      | Not used  |   | Group ID number |   | Number in group |   | Interleave order |   |   |   |   |   |   |   |   |   |
| Default value | 00        |   | 00              |   | 00              |   | 00               |   |   |   |   |   |   |   |   |   |

- Standalone  
 GROUP ID = 0  
 Number of units = 0  
 Interleave order = 0 (0000 0000 0000 0000)
- Master  
 GROUP ID = 1  
 Number of units = 0  
 Interleave order = 0 (0000 0001 0000 0000)
- Slave (in phase)  
 GROUP ID = 1  
 Number of units = 2  
 Interleave order = 0 (0000 0001 0010 0000)
- Slave (180° out of phase)  
 GROUP ID = 1  
 Number of units = 2  
 Interleave order = 1 (0000 0001 0010 0001)

All other combinations are invalid.

The default state can either be “standalone” or one of the two “slave” modes (it cannot be master because un-programmed units would both try to send their clock on the same SYNC line).



**PMBus ADDRESS (ADDR Pin)**

The SiC951 has a 7-bit register that are used to set the base PMBus address of the device. A resistor may be connected between the ADDR and A<sub>GND</sub> pins to set an offset from the default pre-configured MFR base address in the memory. Up to 16 different offsets can be set allowing 16 SiC951 devices with unique addresses in a single system. This offset and therefore the device address is read by the ADC during the initialization sequence. The table below provides the resistor values needed to set the 16 offsets from the base address:

A missing or shorted resistor results in the part turning on with the default PMBus settings and output voltage based on the V<sub>SET</sub> resistor. This allows for easy system debug.

**Note**

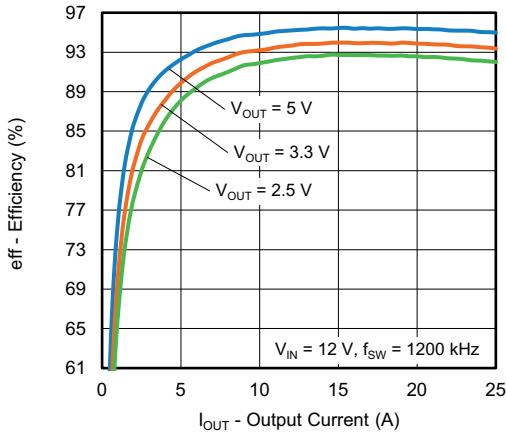
- The ADDR resistor will set the initial position of the MFR\_BASE\_ADDRESS (see PMBus command table)

| <b>WRITE</b>      |                |            |            |
|-------------------|----------------|------------|------------|
| <b>CONNECTION</b> | <b>ADDRESS</b> | <b>HEX</b> | <b>BIN</b> |
| Short / open      | 0              | 1E         | 00011110   |
| 0.845K            | 1              | 20         | 00100000   |
| 1.3K              | 2              | 22         | 00100010   |
| 1.78K             | 3              | 24         | 00100100   |
| 2.32k             | 4              | 26         | 00100110   |
| 2.87K             | 5              | 28         | 00101000   |
| 3.48K             | 6              | 2A         | 00101010   |
| 4.12K             | 7              | 2C         | 00101100   |
| 4.75K             | 8              | 2E         | 00101110   |
| 5.49K             | 9              | 30         | 00110000   |
| 6.19K             | 10             | 32         | 00110010   |
| 6.98K             | 11             | 34         | 00110100   |
| 7.87K             | 12             | 36         | 00110110   |
| 8.87K             | 13             | 38         | 00111000   |
| 10K               | 14             | 3A         | 00111010   |
| 11K               | 15             | 3C         | 00111100   |

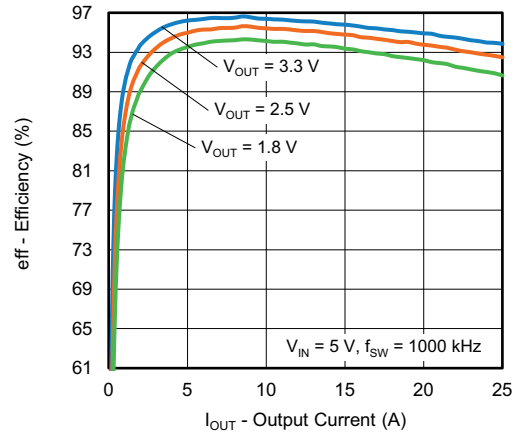
| <b>READ</b>       |                |            |            |
|-------------------|----------------|------------|------------|
| <b>CONNECTION</b> | <b>ADDRESS</b> | <b>HEX</b> | <b>BIN</b> |
| Short / open      | 0              | 1F         | 00011111   |
| 0.845K            | 1              | 21         | 00100001   |
| 1.3K              | 2              | 23         | 00100011   |
| 1.78K             | 3              | 25         | 00100101   |
| 2.32k             | 4              | 27         | 00100111   |
| 2.87K             | 5              | 29         | 00101001   |
| 3.48K             | 6              | 2B         | 00101011   |
| 4.12K             | 7              | 2D         | 00101101   |
| 4.75K             | 8              | 2F         | 00101111   |
| 5.49K             | 9              | 31         | 00110001   |
| 6.19K             | 10             | 33         | 00110011   |
| 6.98K             | 11             | 35         | 00110101   |
| 7.87K             | 12             | 37         | 00110111   |
| 8.87K             | 13             | 39         | 00111001   |
| 10K               | 14             | 3B         | 00111011   |
| 11K               | 15             | 3D         | 00111101   |



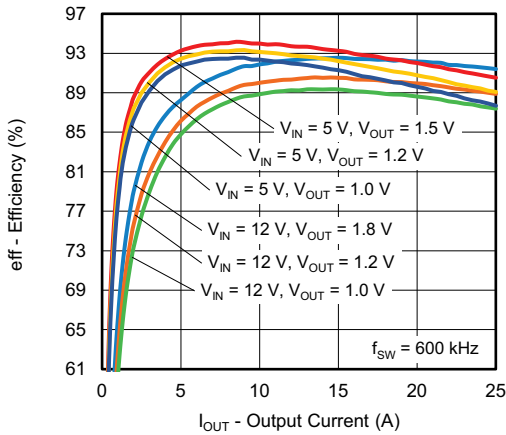
**ELECTRICAL CHARACTERISTICS** ( $V_{IN} = 12\text{ V}$ ,  $V_{OUT} = 1.2\text{ V}$ ,  $f_{SW} = 600\text{ kHz}$ , SiC951 (25 A),  $C_{IN} = 2.2\text{ }\mu\text{F} \times 3$ ,  $C_{OUT} = 47\text{ }\mu\text{F} \times 12$ , unless otherwise noted)



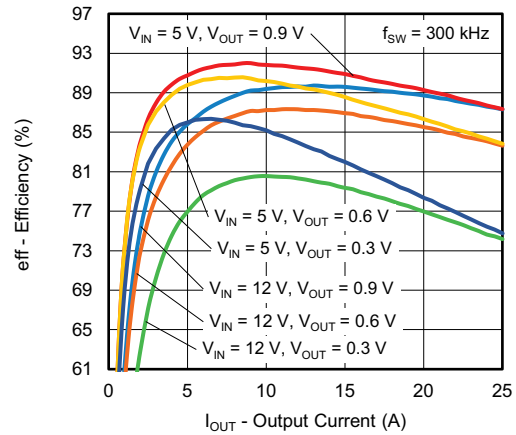
**Fig. 10 - Efficiency vs. Output Current**



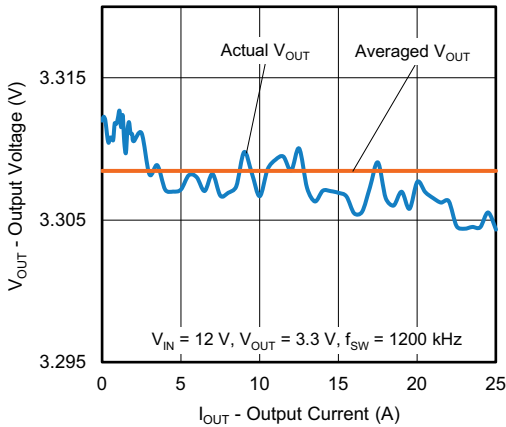
**Fig. 13 - Efficiency vs. Output Current**



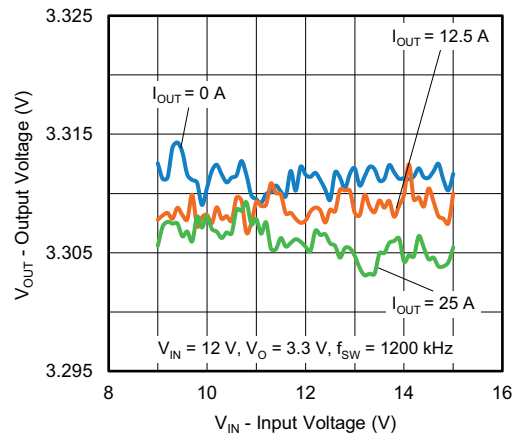
**Fig. 11 - Efficiency vs. Output Current**



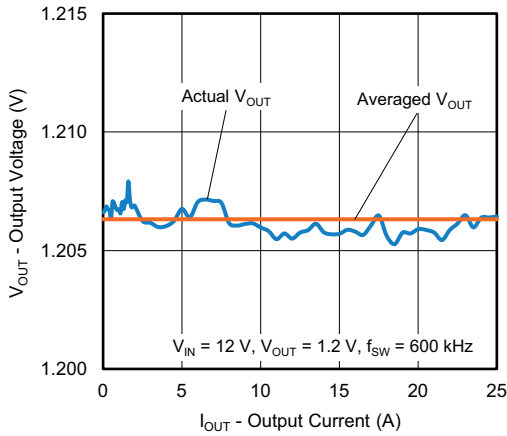
**Fig. 14 - Efficiency vs. Output Current**



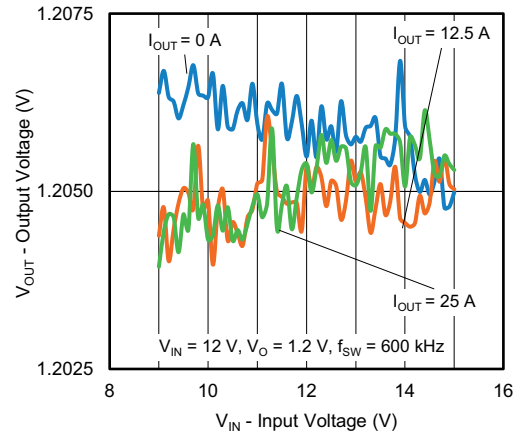
**Fig. 12 - Load Regulation,  $V_O = 3.3\text{ V}$**



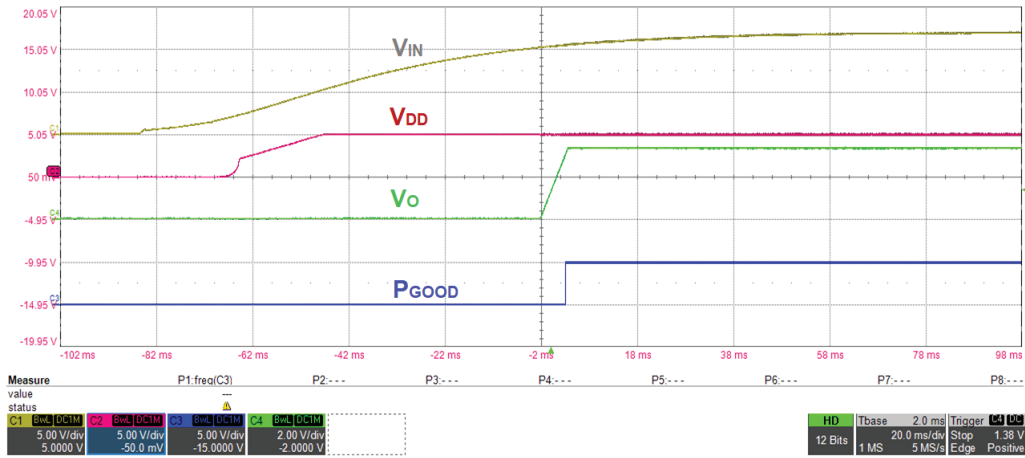
**Fig. 15 - Line Regulation,  $V_O = 3.3\text{ V}$**



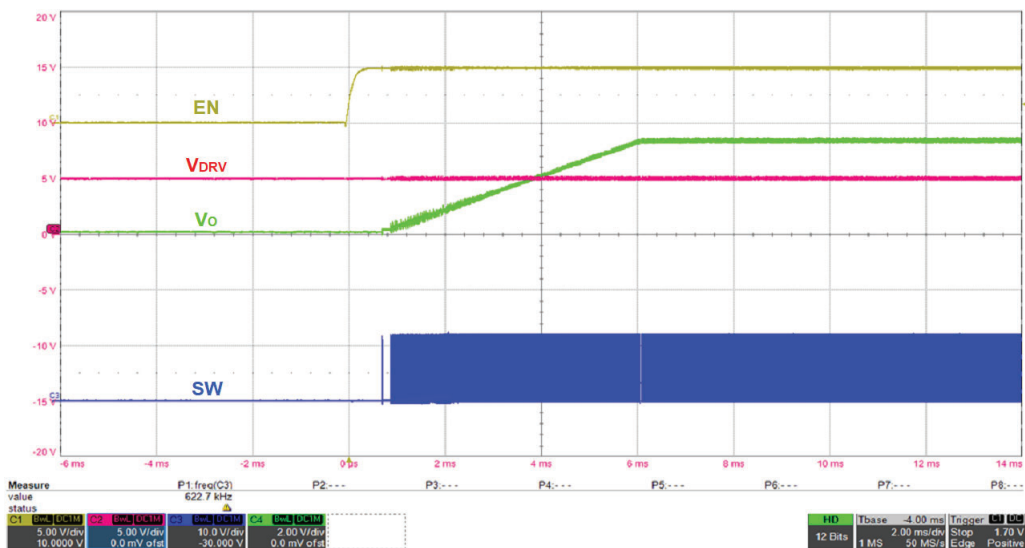
**Fig. 16 - Load Regulation,  $V_O = 1.2\text{ V}$**



**Fig. 17 - Line Regulation,  $V_O = 1.2\text{ V}$**



**Fig. 18 - Startup With  $V_{IN}$ , no load**



**Fig. 19 - Startup With EN, no load**

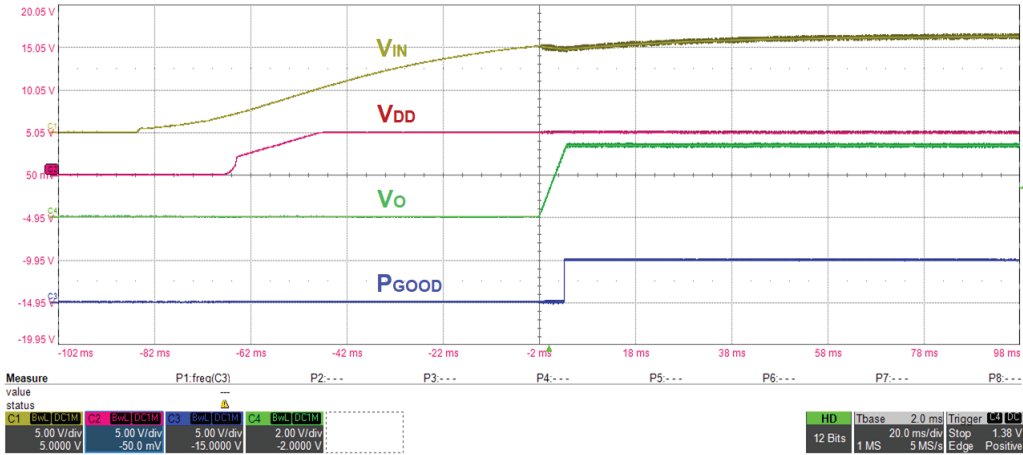


Fig. 20 - Startup With  $V_{IN}$ , 25 A load

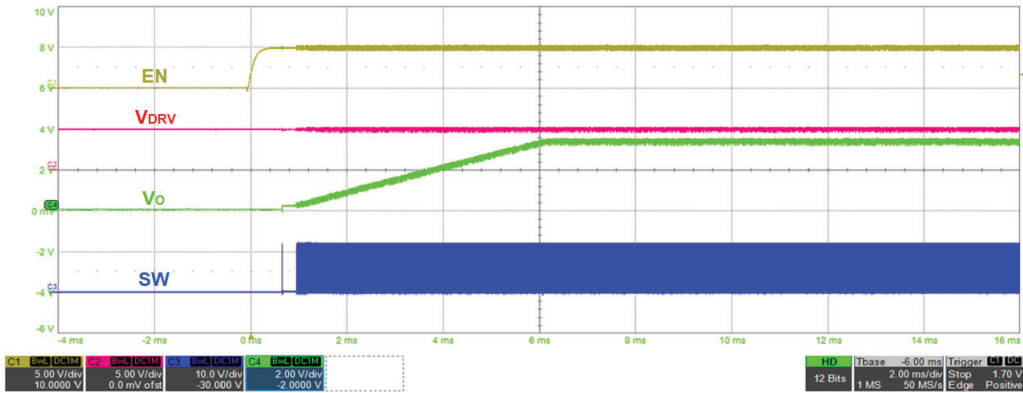


Fig. 21 - Startup with EN, 25 A load

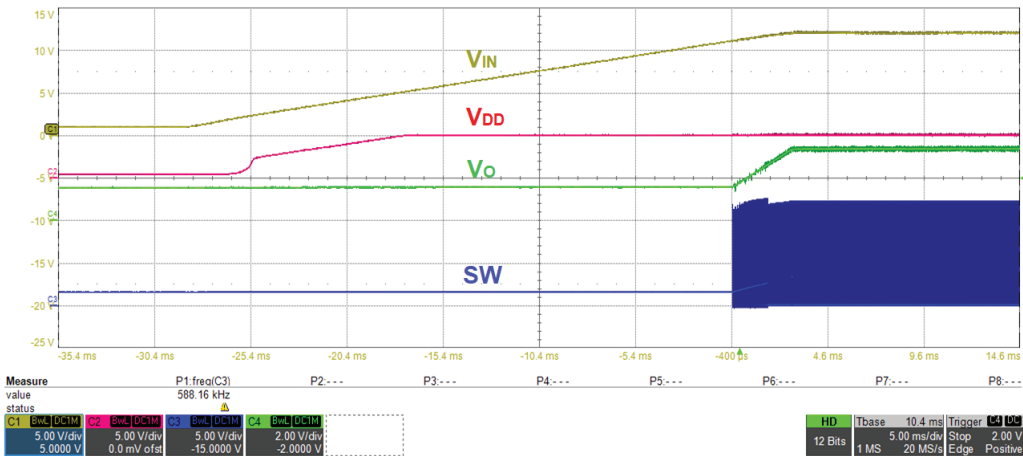


Fig. 22 - Startup With  $V_{IN}$ , no load, 1.5 V  $V_O$  pre-bias

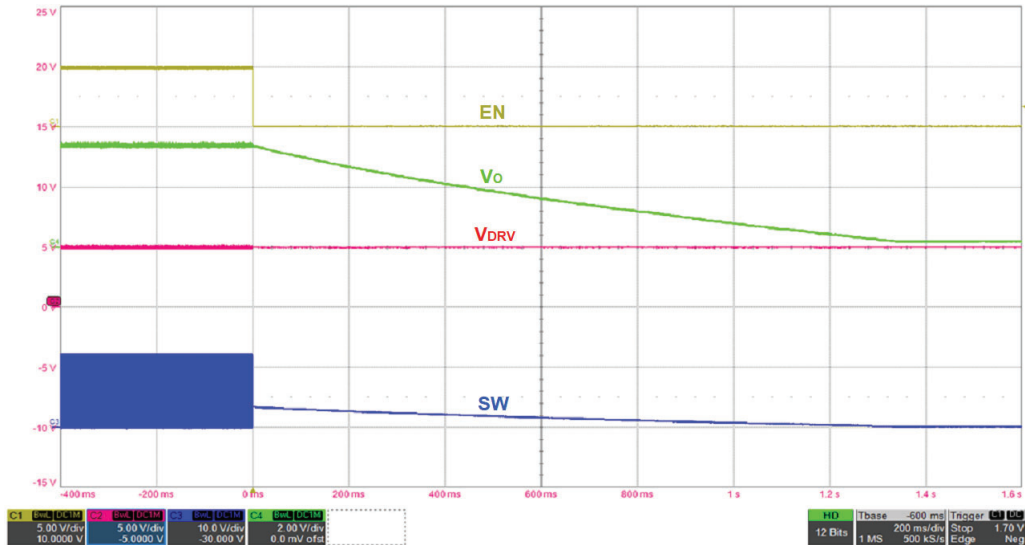


Fig. 23 - Shutdown with EN, no load

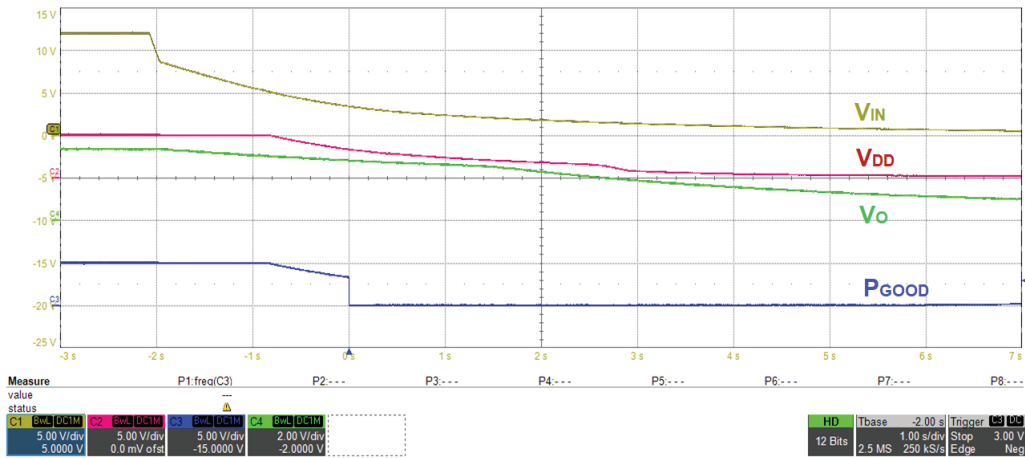


Fig. 24 - Shutdown with  $V_{IN}$ , no load

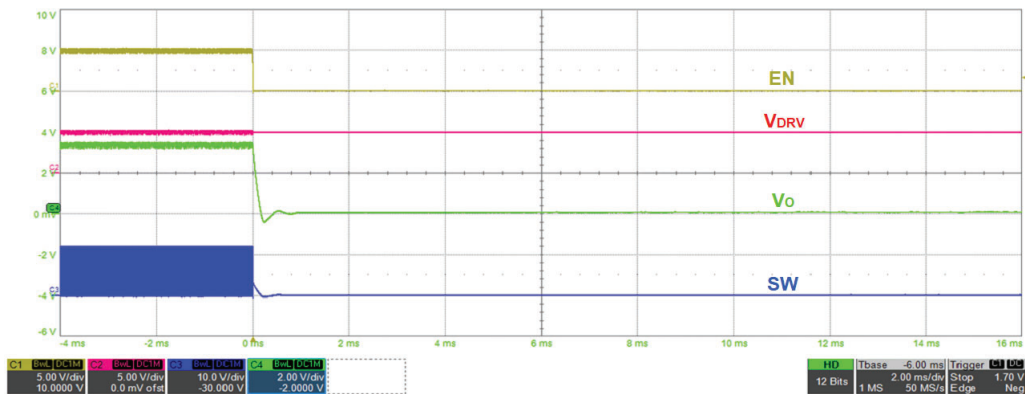


Fig. 25 - Shutdown with EN, 25 A load

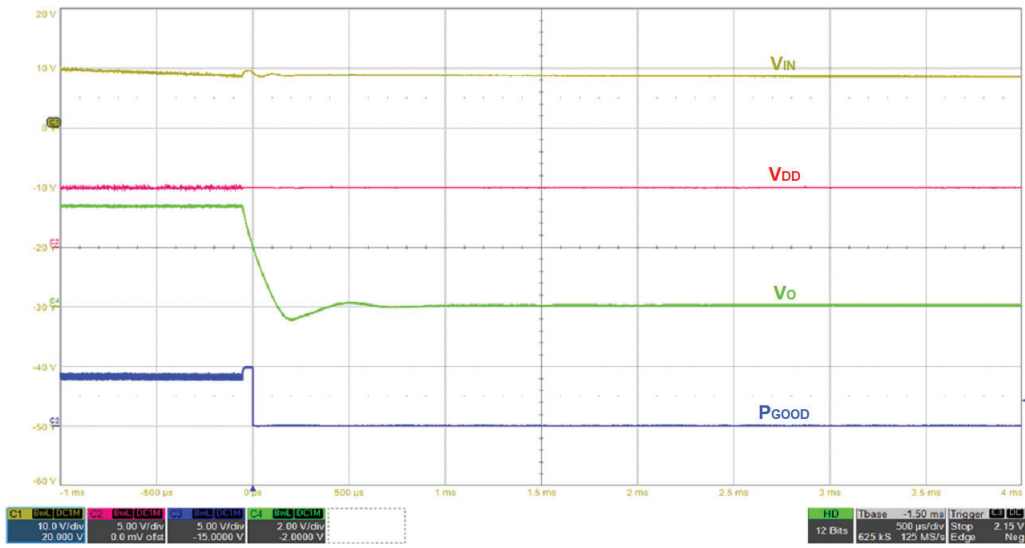


Fig. 26 - Shutdown with  $V_{IN}$ , 25 A load

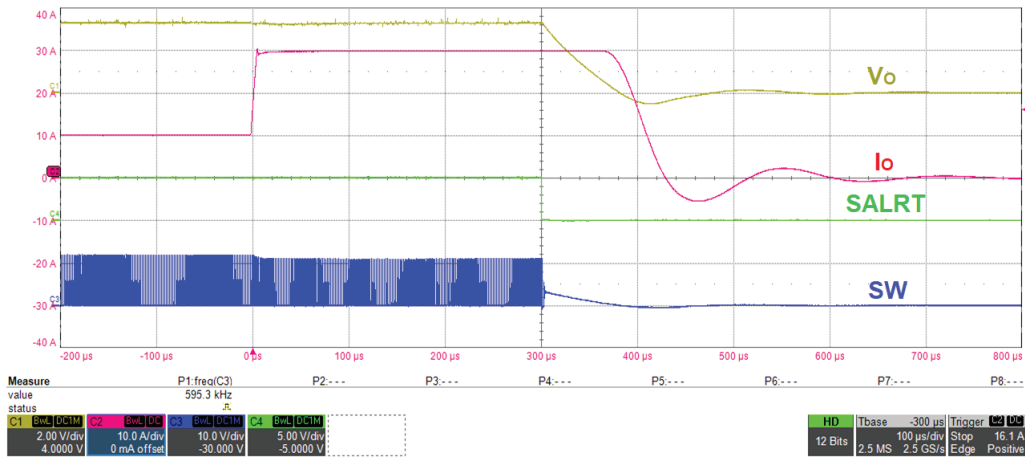


Fig. 27 - OCP

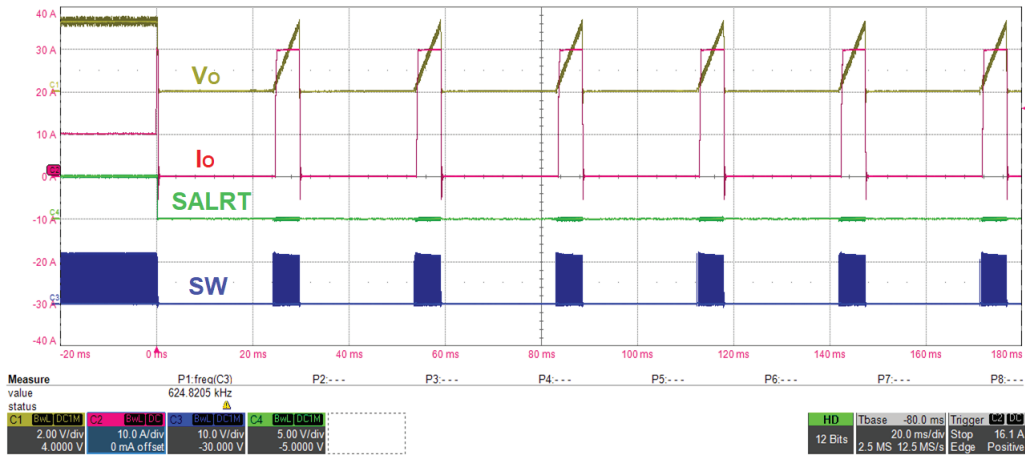


Fig. 28 - OCP

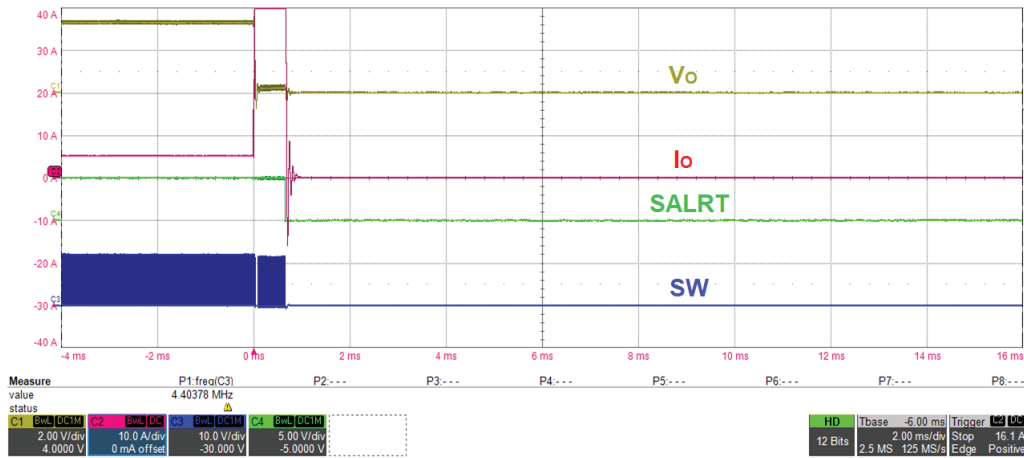


Fig. 29 - SCP

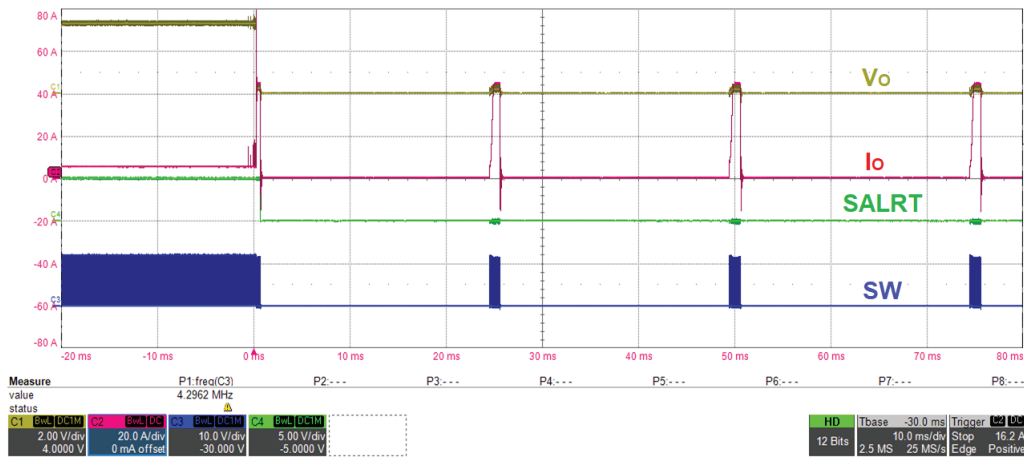


Fig. 30 - SCP

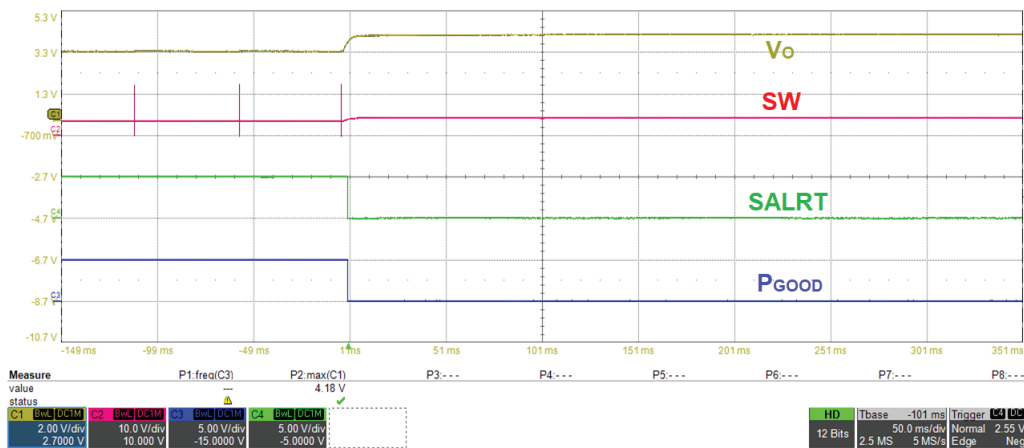
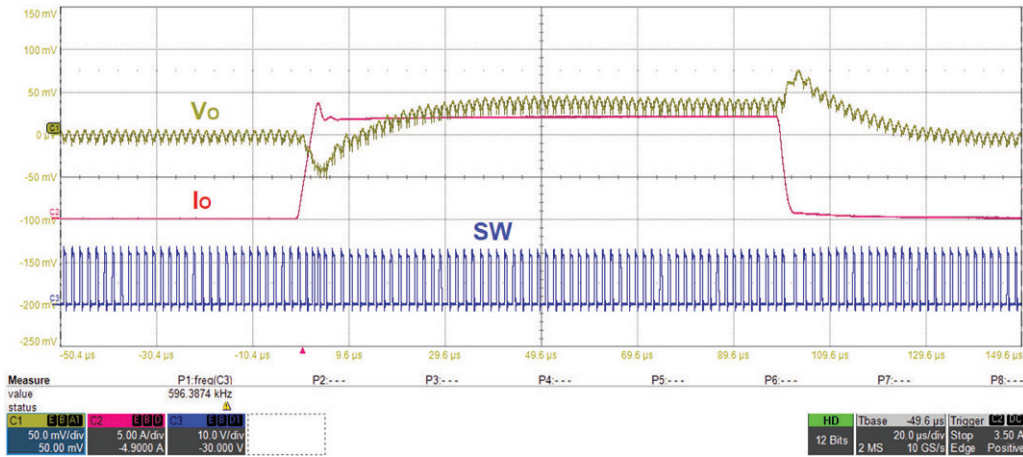
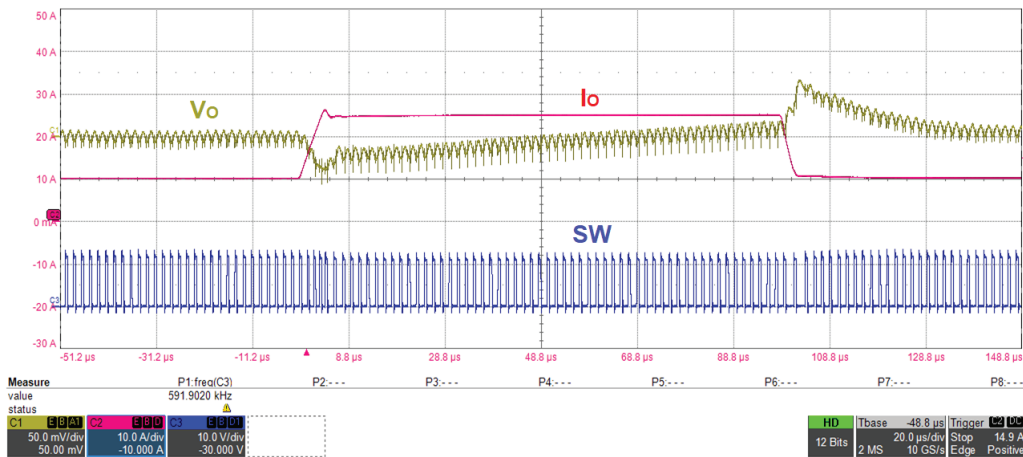
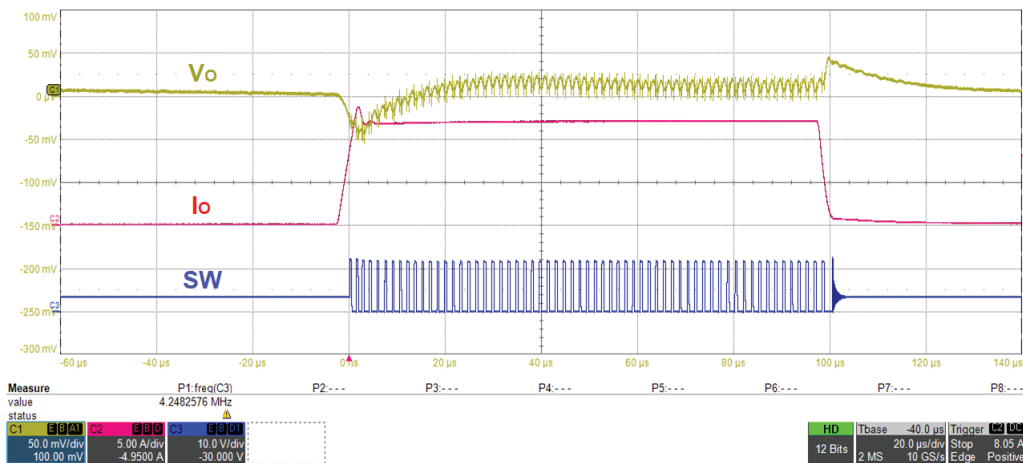
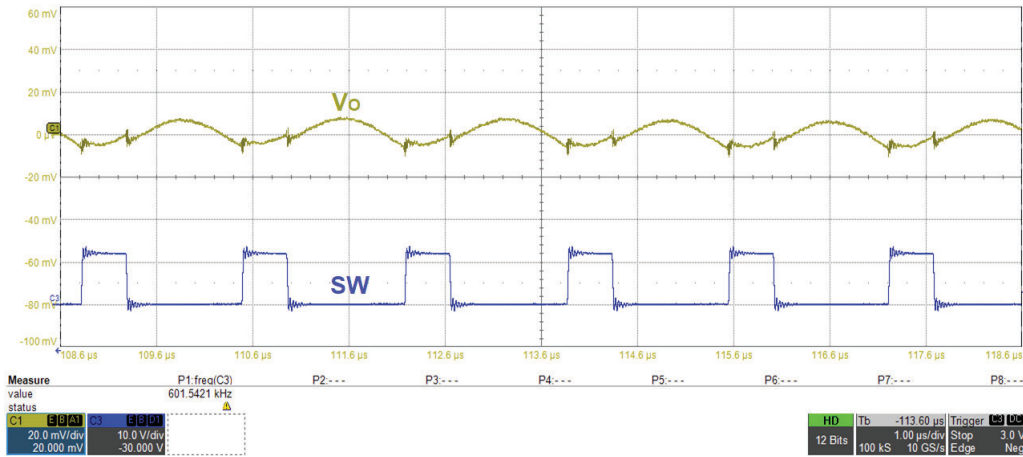


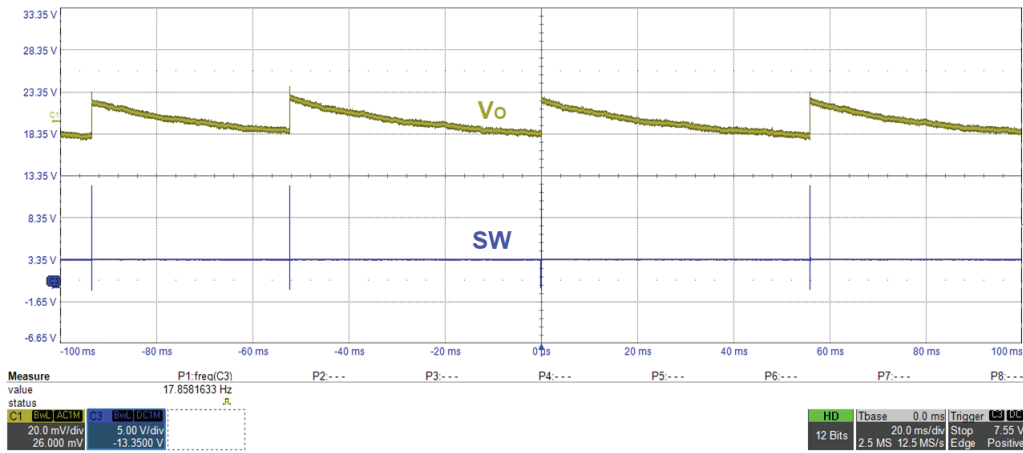
Fig. 31 - OVP



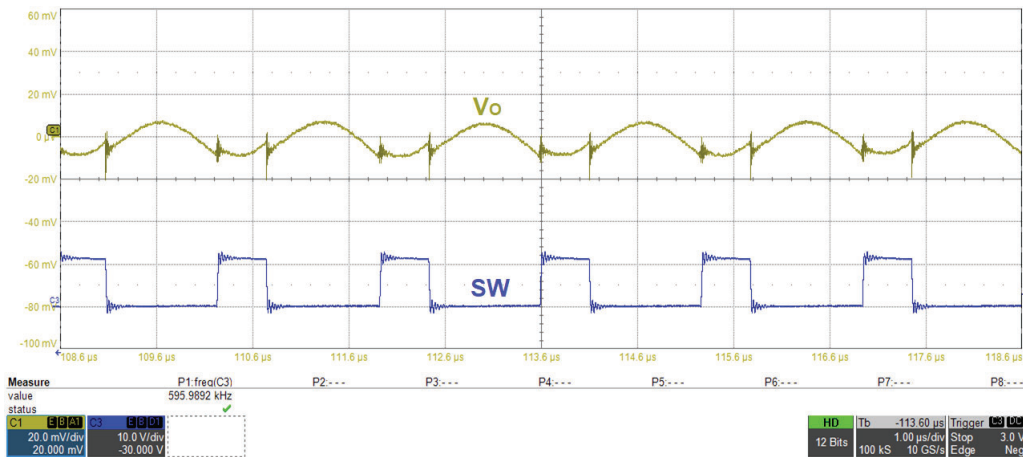

**Fig. 32 - Load step, 0 A to 12 A to 0 A, CCM**

**Fig. 33 - Load step, 10 A to 25 A to 10 A**

**Fig. 34 - Load step, 0 A to 12 A to 0 A, PSM**



**Fig. 35 - Output Ripple at no load, CCM**



**Fig. 36 - Output Ripple at no load, PSM**



**Fig. 37 - Output Ripple at 25 A**

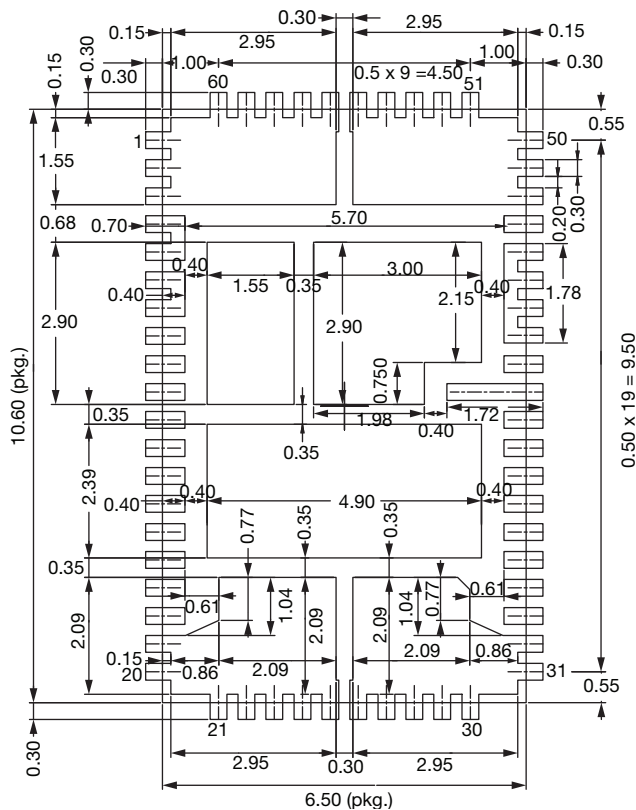
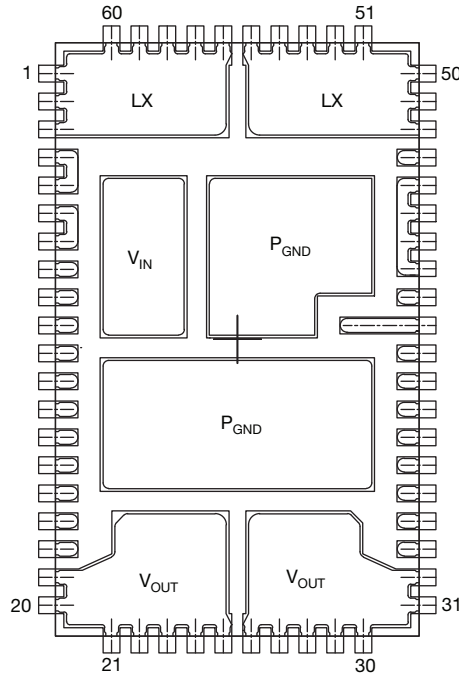




| PRODUCT SUMMARY               |   |
|-------------------------------|---|
| Part number                   | SiC951  |
| Description                   | 4.5 V to 20 V input 25 A microBRICK® DC/DC converter with PMBus |
| Input voltage min. (V)        | 4.5   |
| Input voltage max. (V)        | 20  |
| Output voltage min. (V)       | 0.3   |
| Output voltage max. (V)       | 5.5   |
| Continuous current (A)        | 25  |
| Switch frequency min. (kHz)   | 300   |
| Switch frequency max. (kHz)   | 1500  |
| Pre-bias operation (yes / no) | Yes   |
| Internal bias reg. (yes / no) | Yes   |
| Compensation                  | Internal  |
| Enable (yes / no)             | Yes   |
| P <sub>GOOD</sub> (yes / no)  | Yes   |
| Over current protection       | Yes   |
| Protection                    | OVP, OCP, UVP/SCP, OTP, UVLO                                    |
| Light load mode               | Power save  |
| Peak efficiency (%)           | 96.6  |
| Package type                  | PowerPAK MLP59-A6C  |
| Package size (W, L, H) (mm)   | 10.6 x 6.5 x 3  |
| Status code                   | 1   |
| Product type                  | microBRICK® (step down regulator)                               |
| Applications                  | n/a   |

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?71554](http://www.vishay.com/ppg?71554).

**Recommended Land Pattern PowerPAK® MLP59-A6C**



**Note**

- Dimensions in mm

ECN: T24-0079-Rev. A, 11-Mar-2024  
 DWG: 3025



## Disclaimer

ALL PRODUCT, PRODUCT SPECIFICATIONS AND DATA ARE SUBJECT TO CHANGE WITHOUT NOTICE TO IMPROVE RELIABILITY, FUNCTION OR DESIGN OR OTHERWISE.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, "Vishay"), disclaim any and all liability for any errors, inaccuracies or incompleteness contained in any datasheet or in any other disclosure relating to any product.

Vishay makes no warranty, representation or guarantee regarding the suitability of the products for any particular purpose or the continuing production of any product. To the maximum extent permitted by applicable law, Vishay disclaims (i) any and all liability arising out of the application or use of any product, (ii) any and all liability, including without limitation special, consequential or incidental damages, and (iii) any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.

Statements regarding the suitability of products for certain types of applications are based on Vishay's knowledge of typical requirements that are often placed on Vishay products in generic applications. Such statements are not binding statements about the suitability of products for a particular application. It is the customer's responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application. Parameters provided in datasheets and / or specifications may vary in different applications and performance may vary over time. All operating parameters, including typical parameters, must be validated for each customer application by the customer's technical experts. Product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein.

Hyperlinks included in this datasheet may direct users to third-party websites. These links are provided as a convenience and for informational purposes only. Inclusion of these hyperlinks does not constitute an endorsement or an approval by Vishay of any of the products, services or opinions of the corporation, organization or individual associated with the third-party website. Vishay disclaims any and all liability and bears no responsibility for the accuracy, legality or content of the third-party website or for that of subsequent links.

Except as expressly indicated in writing, Vishay products are not designed for use in medical, life-saving, or life-sustaining applications or for any other application in which the failure of the Vishay product could result in personal injury or death. Customers using or selling Vishay products not expressly indicated for use in such applications do so at their own risk. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay. Product names and markings noted herein may be trademarks of their respective owners.