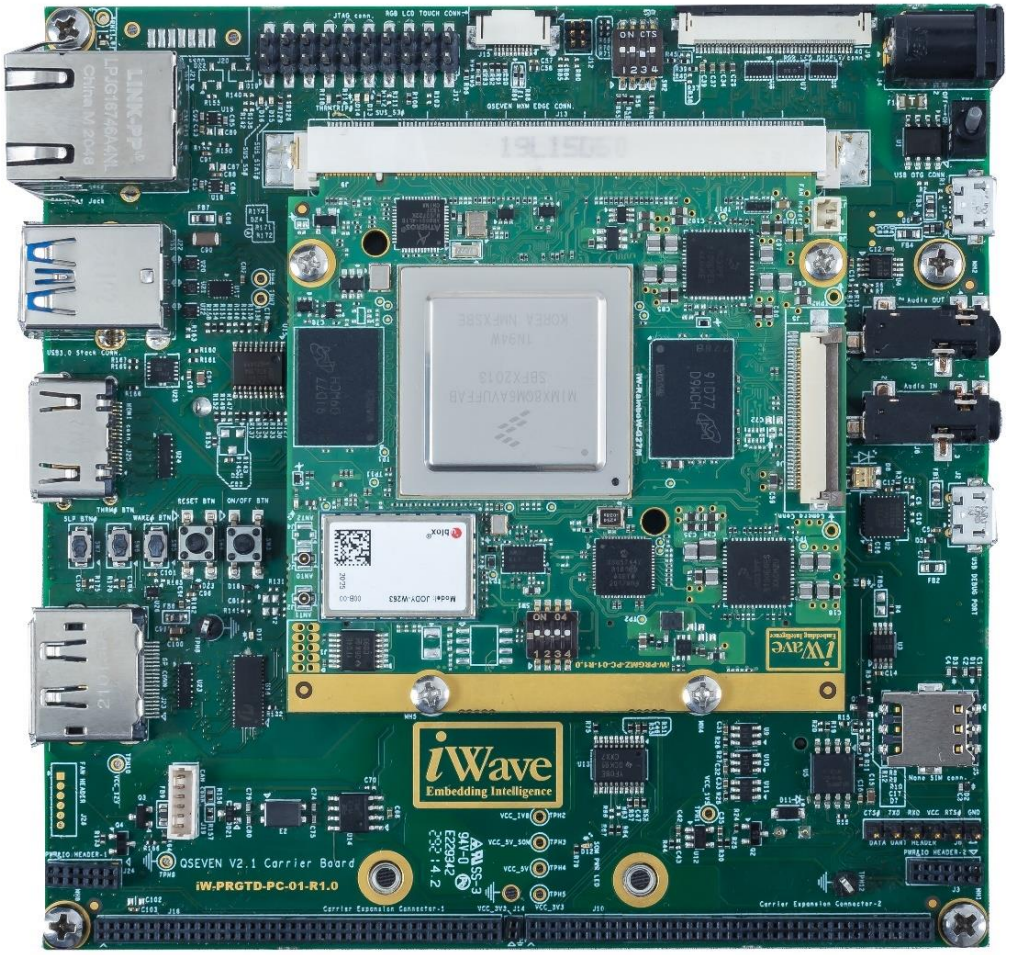
iW-RainboW-G27D
i.MX8 QuadMax/QuadPlus
Qseven Development Platform
Hardware User Guide



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1. INTRODUCTION

1.1 Purpose

This document is the Hardware User Guide for the i.MX 8 QM/QP Qseven V2.1 Development platform "iW-RainboW-G27D" based on the NXP's i.MX8 Application processor. This board is fully supported by iWave Systems Technologies Pvt. Ltd. This Guide provides detailed information on the overall design and usage of the i.MX 8 QM/QP based Qseven development platform from a Hardware Systems perspective. Complete information about the i.MX 8 QM/QP Qseven SOM is explained in another document "iW-RainboW-G27M_i.MX8QM_QP_Qseven_SOM-HardwareUserGuide".

1.2 Overview

The Qseven V2.1 concept is an off-the-shelf, multi-vendor, Computer-On-Module that integrates all the core components of a common PC and is mounted onto an application specific carrier board.

iW-RainboW-G27D Development Platform comes with Qseven V2.1 Generic Carrier, i.MX 8 QM/QP based Qseven V2.1 SOM. The development board can be used for quick prototyping of various applications targeted by the i.MX8 processor. With 120mmx120mm Nano ITX size, Qseven carrier board is highly packed with all the necessary on-board connectors to validate the Qseven features of i.MX 8 QM/QP Qseven SOM.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
CAN	Controller Area Network
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
CSI	Camera Serial Interface
DP	Display Port
DSI	Display Serial Interface
eMMC	Enhanced Multi Media Card
GB	Giga Byte
Gbps	Gigabits per sec
GPIO	General Purpose Input Output
HDMI	High-Definition Multimedia Interface
Hz	Hertz
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
IC	Integrated Circuit
LVDS	Low Voltage Differential Signalling

Acronyms	Abbreviations
MIPI	Mobile Industry Processor Interface
MLB	Media Local Bus
MXM	Mobile PCI Express Module
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
RoHS	Restriction of Hazardous Substances
RTC	Real Time Clock
SATA	Serial Advanced Technology Attachment
SD	Secure Digital
SOM	System On Module
TBD	To Be Defined
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
USB OTG	USB On The Go
V	Voltage

1.4 Terminology Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
DIFF	Differential Signal
LVDS	Low Voltage Differential Signal
GBE	Gigabit Ethernet Media Dependent Interface differential pair signals
USB HS	Universal Serial Bus High Speed differential pair signals
USB SS	Universal Serial Bus Super Speed differential pair signals
MIPI	Mobile Industry Processor Interface signals
HDMI	High-Definition Multimedia Interface Differential Signal
DP	Display Port Differential Signal
OD	Open Drain Signal
OC	Open Collector Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented On- Qseven *SOM.*

1.5 References

- IMX8QMAEC_Revx.pdf
- iMX8QM_RM_Rev_x.pdf
- Qseven® Specification Version 2.1
- Qseven® Design Guide 2.0

2. ARCHITECTURE AND DESIGN

This section provides detailed information about the i.MX 8 QM/QP Qseven SOM features and Hardware architecture with high level block diagram.

2.1 I .MX 8 QM/QP Qseven Development Platform Block Diagram

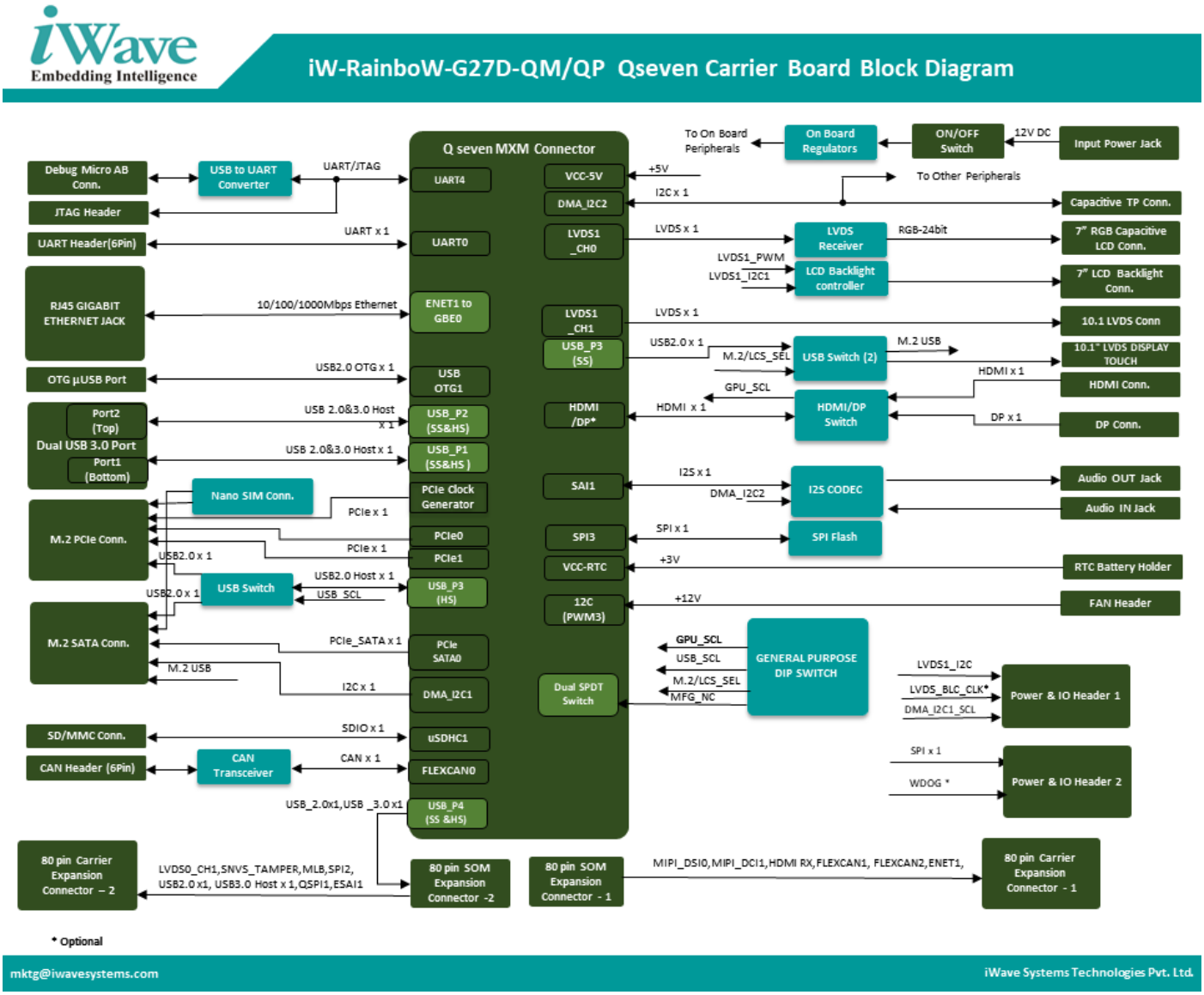


Figure 1: i.MX 8 QM/QP Qseven Development Platform Block Diagram

2.2 i.MX 8 QM/QP Qseven Development Platform Features

The NXP's i.MX8 QM/QP Qseven carrier board supports the following features to validate the NXP's i.MX8 QM/QP Qseven SOM Edge connector interface.

Serial Interface Features

- Debug UART through USB Micro AB Connector
- Data UART x 1 Port through Header

High Speed Interface Features

- M.2 PCIe connector
- M.2 SATA Connector
- USB 3.0 Host x 2 Port through USB 3.0 Type A Connector[1]

Communication Features

- 10/100/1000Mbps Ethernet through RJ45MagJack
- USB 2.0 Host x 1 Port through Type A Connector (Dual stack USB 3.0 - Top)
- USB 2.0 OTG x 1 Port through Micro AB Connector
- SDHC/SDIO (4bit) x 1 Port through Standard SD Connector
- CAN x 1 Port Through Header

Audio/Video Features

- I2S Audio Codec with 3.5mm Audio IN and OUT jack
- HDMI X 1 Port through Type A Connector
- DP x 1 Port Through Type A Connecter[2] (Optional Shared With HDMI)
- 7'' RGB Display Connector through LVDS to RGB Transmitter with Capacitive Touch
- 2nd LVDS Port display Connector

Additional Features

- SPI Flash
- RTC Coin Cell holder
- Buzzer
- Fan Header
- 20 - Pin JTAG Header

On Board Switches

- Power ON/OFF Switch
- Board Configuration Switch
- Reset Switch

Carrier board Expansion Connector: 1

- MIPI_DSI x 2
- HDMI_RX x1
- CAN x 2
- ENET x1

Carrier board Expansion Connector: 2

- LVDS_0 x 1
- SNVS_TAMPER X1
- MLB x1
- SPI X 1
- USB 2.0 x 1
- USB 3.0 x 1
- QSPI x 1
- ESAI x 1

General Specification

- Power Supply : 12V, 2A Power Input Jack
- Temperature Supported : 0°C to +60°C
- Form Factor : 120mm X 120mm Nano ITX

[1] Either USB 2.0 in Mini PCIe connector or USB 3.0 Type A TOP connector can be supported at a time. Anyone can be selected using on Board Switches.

2.3 Qseven MXM Connector

The i.MX 8 QM/QP Qseven carrier board supports 230Pin Qseven MXM Edge mating connector for Qseven SOM attachment. This standard 230-pin robust connector is capable of handling high-speed serialized signals and can be used for size constrained embedded applications. This Qseven MXM connector (J13) is physically located at the top of the board as shown below.

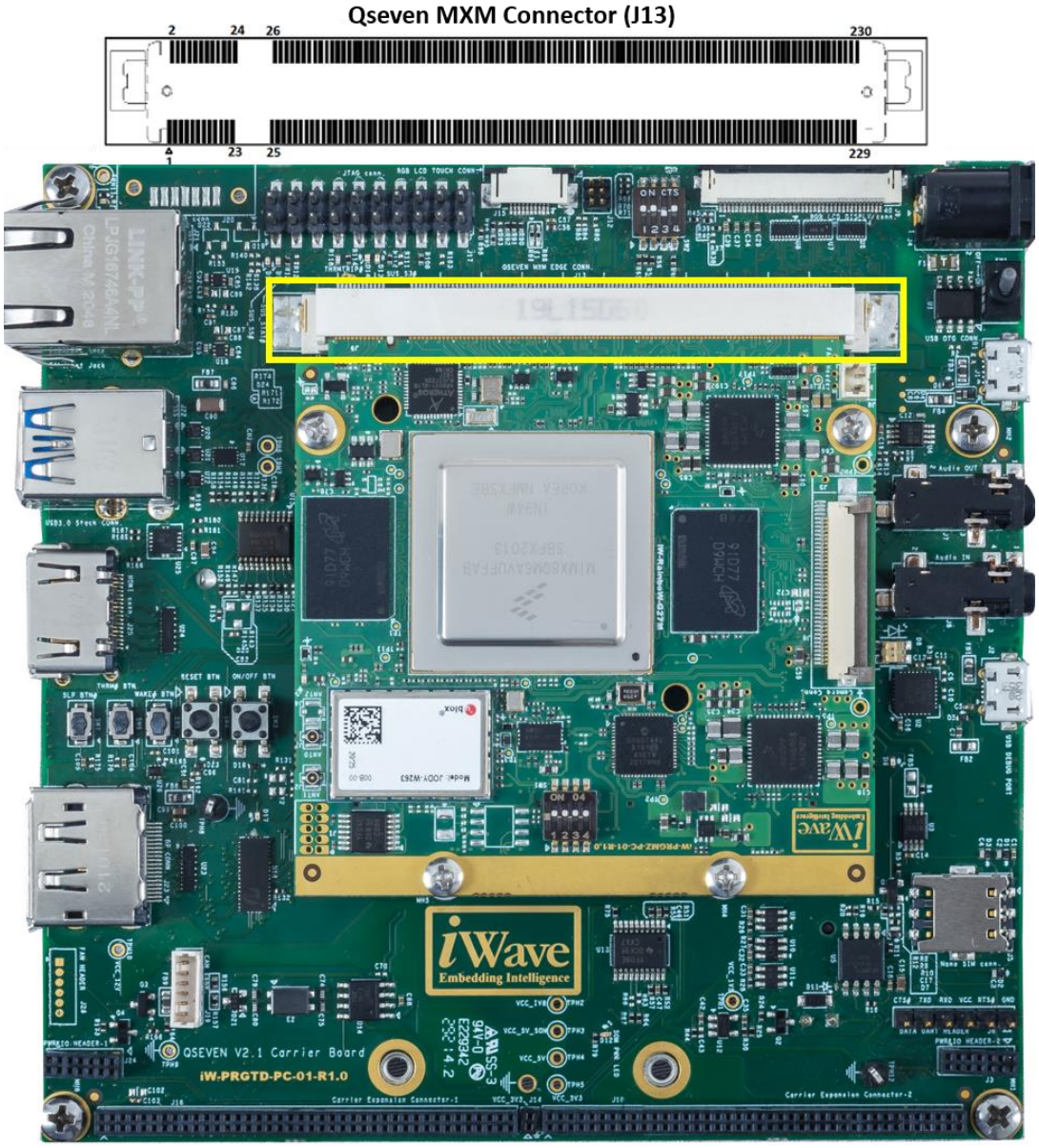


Figure 2: Qseven MXM Connector

2.3.1 Qseven PCB Edge Connector Pin Assignment

Table 3: Qseven PCB Edge Connector Pin Assignment

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
1	GND	GND	NA	Power	Ground.
2	GND	GND	NA	Power	Ground.
3	GBE_MDI3-	GBE0_MDI3-	NA	IO, DIFF	Gigabit Ethernet MDI differential pair 3 negative.
4	GBE_MDI2-	GBE0_MDI2-	NA	IO, DIFF	Gigabit Ethernet MDI differential pair 2 negative.
5	GBE_MDI3+	GBE0_MDI3+	NA	IO, DIFF	Gigabit Ethernet MDI differential pair 3 positive.
6	GBE_MDI2+	GBE0_MDI2+	NA	IO, DIFF	Gigabit Ethernet MDI differential pair 2 positive.
7	GBE_LINK100#	GBE0_LINK100#	NA	I, 3.3V CMOS	100Mbps Ethernet link status LED.
8	GBE_LINK1000#	GBE0_LINK1000#	NA	I, 3.3V CMOS	Gigabit Ethernet link status LED
9	GBE_MDI1-	GBE0_MDI1-	NA	IO, DIFF	Gigabit Ethernet MDI differential pair 1 negative.
10	GBE_MDI0-	GBE0_MDI0-	NA	IO, DIFF	Gigabit Ethernet MDI differential pair 0 negative.
11	GBE_MDI1+	GBE0_MDI1+	NA	IO, DIFF	Gigabit Ethernet MDI differential pair 1 positive.
12	GBE_MDI0+	GBE0_MDI0+	NA	IO, DIFF	Gigabit Ethernet MDI differential pair 0 positive.
13	GBE_LINK#	GPHY_LINK_LED	NA	I, 3.3V CMOS	Gigabit Ethernet link status LED. - This pin is connected to indication LED D24
14	GBE_ACT#	GBE0_LINK_ACT#	NA	I, 3.3V CMOS	Gigabit Ethernet Activity status LED.
15	GBE_CTREF	VPHY0_DVDDL	NA	Power	Power for the Centre Tap of Mack Jack connector
16	SUS_S5#	SUS_S5_Q7	NA	I, 3.3V CMOS /10K PU	S5 State. This pin is connected to indication LED D16.
17	WAKE#	WAKE#(GPIO3_04)	SPI0_SDI/ BA5	O, 3.3V CMOS	This pin is connected to Push button (SW5) in carrier board.
18	SUS_S3#	SUS_S3_Q7	NA	I, 3.3V CMOS/10K PU	S3 state. This pin is connected to indication LED D13. .
19	SUS_STAT#	SUS_STAT_Q7(GPIO2_05)	ESAI1_FST/ BF12	I, 3.3V CMOS/10K PU	Suspend Status.

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
					This pin is connected to indication LED D15.
20	PWRBTN#	PWRBTN#	ON_OFF_BUTTON/ BE47	O, 3.3V CMOS/10K PU	Power Button output. This pin is connected to Push button (SW3) in the carrier board used for SOM On/Off control.
21	SLP_BTN#	GPII_1(GPIO0_04)	LSIO.GPIO0.IO04/ AT48	O, 3.3V CMOS	This pin is connected to Push button (SW7) in carrier board.
22	LID_BTN#	GPII_0(GPIO3_03)	SPI0_SDO/ AY6	I, 3.3V CMOS	This pin is connected from Config Connecter(J12) 1st Pin with Grounded 2nd pin.
23	GND	GND	NA	Power	Ground.
24	GND	GND	NA	Power	Ground.
Key					
25	GND	GND	NA	Power	Ground.
26	PWGIN	PWGIN	NA	O, 5V CMOS/ 10K PU	Power Good Output.
27	BATLOW#	GPII_2(GPIO0_05)	LSIO.GPIO0.IO05/ AP46	I, 3.3V CMOS	This pin is connected from Config Connecter (J12) 5th Pin with Grounded 6th pin.
28	RSTBTN#	RSTBN	NA	O, 3.3V CMOS	Active low Reset button Output. This pin is connected to Push button SW4 in carrier board for reset generation. It's Connected with JTAG
29	SATA0_TX+	PCIE_SATA0_TX0_P	PCIE_SATA0_TX0_P/ B16	I, SATA	This pin is connected to M.2 SATA Connector (J33) for SATA Channel0 Transmit differential pair positive.
30	SATA1_TX+	NC	NA	NC	NC in i.MX8 Qseven SOM. This pin connected to 7pin SATA Connector (J20) in carrier board. (Optional)
31	SATA0_TX-	PCIE_SATA0_TX0_N	PCIE_SATA0_TX0_N/ C17	I, SATA	This pin connected to M.2 SATA Connector (J33) for SATA Channel0 Transmit differential pair negative.
32	SATA1_TX-	NC	NA	NA	NC in i.MX8 Qseven SOM. This pin connected to 7pin SATA Connector (J20) in carrier board. (Optional)

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
33	SATA_ACT#	GPIO_SATA_ACT#(GPIO1_18)	MIPI_DSI0_GPIO0_00/BD30	I, 3.3V CMOS	This pin connected from M.2 SATA Connector (J33) for SATA Channel0 command Activity line. It's Connected with D9 Indicating LED And Optionally Connected with J31 Command Activity Line
34	GND	GND	NA	Power	Ground.
35	SATA0_RX+	PCIE_SATA0_RX0_P	PCIE_SATA0_RX0_P/ A19	I, SATA	This pin connected to M.2 SATA Connector (J33) for SATA Channel0 Receive differential pair positive.
36	SATA1_RX+	NC	NA	-	NC in i.MX8 Qseven SOM. This pin connected to 7pin SATA Connector (J20) in carrier board. (optional)
37	SATA0_RX-	PCIE_SATA0_RX0_N	PCIE_SATA0_RX0_N/ B20	I, SATA	NC in i.MX8 Qseven SOM. This pin connected to 22pin SATA Connector (J25) for SATA Channel0 Receive differential pair negative.
38	SATA1_RX-	NC	NA	NA	NC in i.MX8 Qseven SOM. This pin connected to 7pin SATA Connector (J20) in carrier board. (optional)
39	GND	GND		Power	Ground.
40	GND	GND		Power	Ground.
41	BIOS_DISABLE#/ BOOT_ALT#	NC	NA	NA	NC in i.MX8 Qseven SOM This pin is connected from Config Connecter (J12) 3rd Pin with Grounded 4th pin.
42	SDIO_CLK#	uSDHC1_CLK	USDHC1_CLK /J39	I, 3.3V CMOS	uSDHC1 Clock. This pin is connected to SD/MMC connector(J28)./Optionally Connected With (J27) Micro Sd
43	SDIO_CD#	GPIO_SDC1_CD(GPIO1_23)	MIPI_DSI1_GPIO0_01 /BK24	O, 3.3V CMOS	uSDHC1 Card Detect. This pin is connected from SD/MMC connector(J28)/Optionally Connected With (J27) Micro Sd
44	SDIO_LED	GPIO_SD1_LED(GPIO3_06)	SPI0_CS1/ BA3	I, 3.3V CMOS	This pin is connected to Power I/O Header (J3)

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
45	SDIO_CMD	uSDHC1_CMD	USDHC1_CMD /G41	IO,3.3VCMOS	uSDHC1 command. This pin is connected to SD/MMC connector(J28)./Optionally Connected With (J27) Micro Sd
46	SDIO_WP	GPIO_SDC1_WP(GPIO1_22)	MIPI_DSI1_GPIO0_00/BM24	O, 3.3V CMOS	uSDHC1 Write Protect. This pin is connected to SD/MMC connector(J28)./Optionally Connected With (J27) Micro Sd
47	SDIO_PWR#	GPIO_SDC1_PWR_EN(GPIO1_19)	MIPI_DSI0_GPIO0_01/BD28	I, 3.3V CMOS/ 10K PD	SD/MMC Interface Power Enable. This pin is used control the power input to the SD/MMC connector.(J28),Optionally Connected With (J27) Micro Sd
48	SDIO_DAT1	uSDHC1_DATA1	USDHC1_DATA1 /F38	IO, 3.3V CMOS	uSDHC1 Data1. This pin is connected to SD/MMC connector(J28).Optionally Connected With (J27) Micro Sd
49	SDIO_DAT0	uSDHC1_DATA0	USDHC1_DATA0 /E37	IO, 3.3V CMOS	uSDHC1 Data0. This pin is connected to SD/MMC connector(J28).Optionally Connected With (J27) Micro Sd
50	SDIO_DAT3	uSDHC1_DATA3	USDHC1_DATA3 /F40	IO, 3.3V CMOS	uSDHC1 Data3. This pin is connected to SD/MMC connector(J28).Optionally Connected With (J27) Micro Sd
51	SDIO_DAT2	uSDHC1_DATA2	USDHC1_DATA2 /E39	IO, 3.3V CMOS	uSDHC1 Data2. This pin is connected to SD/MMC connector(J28).Optionally Connected With (J27) Micro Sd
52	RSVD2/SDIO_DAT5	NC	NA	NA	NC in i.MX8 Qseven SOM. This pin is connected to SD/MMC connector (J28) in carrier board.
53	RSVD3/SDIO_DAT5	NC	NA	NA	NC in i.MX8 Qseven SOM. This pin is connected to SD/MMC connector (J28) in carrier board.
54	RSVD4/SDIO_DAT7	NC	NA	NA	NC in i.MX8 Qseven SOM. This pin is connected to SD/MMC connector (J28) in carrier board.
55	RSVD5/SDIO_DAT6	NC	NA	NA	NC in i.MX8 Qseven SOM. This pin is connected to SD/MMC connector (J28) in carrier board.

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
56	USB_DRIVE_VBUS	USB_OTG1_PWR(GPIO4_03)	USB_SS3_TC0/ J9	I, 3.3V CMOS	USB OTG Power enable.
57	GND	GND	NA	Power	Ground.
58	GND	GND	NA	Power	Ground.
59	HDA_SYNC/ I2S_WS	SAI1_TXFS	SAI1_TXFS/ AV2	I, 3.3V CMOS	SSI Audio transmit frame synchronization. This pin is connected to I2S audio codec.
60	SMB_CLK/ GP1_I2C_CLK	DMA_I2C1_SCL	DMA.I2C1.SCL/ AY52	I, 3.3V OD /2.2K PU	I2C1 clock. This pin is connected to Power IO Header (J24) 2nd Pin , M.2 SATA, M.2 PCIe
61	HDA_RST#/ I2S_RST#	GPIO_RESET(GPIO1_05)	LVDS0_GPIO01/ BD40	I, 3.3V CMOS/ 10K PU	This pin is connected to Capacitive Touch Connector for touch reset (J15).
62	SMB_DAT/ GP1_I2C_DAT	DMA_I2C1_SDA	DMA.I2C1.SDA/ AV52	IO, 3.3V OD	I2C1 Data. This pin is connected to Power IO Header (J24) 4th Pin ,M.2 SATA,M.2 PCIe
63	HDA_BCLK/ I2S_CLK	SAI1_TXC	SAI1_TXC / AU5	O, 3.3V CMOS	SSI Audio transmit clock. This pin is connected from I2S audio
64	SMB_ALERT#	SMBUS_ALERT(GPIO1_15)	LVDS1_I2C1_SDA/BN35	O, 3.3V CMOS	NC in i.MX8 Qseven SOM. M.2 Sata Connected(J33) /M.2 PCIe Optional (J31)
65	HDA_SDI/ I2S_SDI	SAI1_RXD	SAI1_RXD/ AV4	O, 3.3V CMOS	SSI Audio Transmit Data. This pin is connected from I2S audio codec.
66	GP0_I2C_CLK	DMA_I2C2_SCL	DMA.I2C2.SCL /BA53	I, 3.3V OD	I2C2 clock. This pin is connected to IO Expander, I2s Audio Codec, Capacitive Touch
67	HDA_SDO/ I2S_SDO	SAI1_TXD	SAI1_TXD / AU1	I, 3.3V CMOS	SSI Audio Receive Data. This pin is connected to I2S audio codec.
68	GP0_I2C_DAT	DMA_I2C2_SDA	DMA.I2C2.SDA / AY50	IO, 3.3V OD	I2C2 Data. This pin is connected to IO Expander ,I2s Audio Codec, Capacitive Touch
69	THRM#	THRM#	NA	I, 3.3V CMOS	This pin is connected from Push button (SW6) in carrier board.
70	WDTRIG#	Q7_WDTRIG_B	NA	I, 3.3V CMOS	This pin is connected to Power I/O Header (J3) 11th Pin

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
71	THRMTRIP#	GPIO_THRMTRIP_ Q7(GPIO3_05)	SPI0_CS0 /BC1	O, 3.3V CMOS	Thermal trip. This pin is connected to indication LED D14
72	WDOUT	Q7_WDOG_B	NA	O, 3.3V CMOS	This pin is connected to Power I/O Header (J3) 9th Pin
73	GND	GND	NA	Power	Ground.
74	GND	GND	NA	Power	Ground.
75	USB_P7-/ USB_SSTX0-	USB3_HUB1_TXM	NA	I, USB SS	USB3.0 Host Port0 Transmit Differential pair negative. This pin is connected to Dual stack USB3.0 Type A connector (J22A) bottom port.
76	USB_P6-/ USB_SSRX0-	USB3_HUB1_RXM	NA	O, USB SS	USB3.0 Host Port0 Receive Differential pair negative. This pin is connected to Dual stack USB3.0 Type A connector (J22A) bottom port.
77	USB_P7+/ USB_SSTX0+	USB3_HUB1_TXP	NA	I, USB SS	USB3.0 Host Port0 Transmit Differential pair positive. This pin is connected to Dual stack USB3.0 Type A connector (J23A) bottom port.
78	USB_P6+/ USB_SSRX0+	USB3_HUB1_RXP	NA	O, USB SS	USB3.0 Host Port0 Receive Differential pair positive. This pin is connected to Dual stack USB3.0 Type A connector (J22A) bottom port.
79	USB_6_7_OC#	NC	NA	NA	NC in i.MX8 Qseven SOM. Over current sense signal for USB3.0 Host Port0. This pin is connected from USB3.0 Host Port0 Over current indicator.
80	USB_4_5_OC#	NC	NA	NA	NC in i.MX8 Qseven SOM. This pin is connected to USB3.0 Host Port1 Over current indicator in carrier board.
81	USB_P5- / USB_SSTX2-	USB3_HUB3_TXM	NA	I, USB SS	This pin is connected to USB Switch For M.2 Sata ,Optionally Connected With M.2 PCIe

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
82	USB_P4- / USB_SSRX2-	USB3_HUB3_RXM	NA	O, USB SS	This pin is connected to USB Switch For M.2 SATA, Optionally Connected With M.2 PCIe
83	USB_P5+ / USB_SSTX2+	USB3_HUB3_TXP	NA	I, USB SS	This pin is connected to USB Switch For M.2 SATA, Optionally Connected With M.2 PCIe
84	USB_P4+ / USB_SSRX2+s	USB3_HUB3_RXP	NA	O, USB SS	This pin is connected to USB Switch For M.2 SATA, Optionally Connected With M.2 PCIe
85	USB_2_3_OC#	USB_HUB3_OC/USB_HUB2_OC	NA	O, 3.3V CMOS	Over current sense signal for USB Host Port2 and Port3. This pin is connected from USB Host Port2 Over current indicator.
86	USB_0_1_OC#	USB_UB1_OC/USB_OTG1_OC(GPIO0_03)	NA	O, 3.3V CMOS/ 10K PU	Over current sense signal for USB Host Port0 and OTG Port1. This pin is connected from Host Port0 and USB OTG Port1 Over current indicator.
87	USB_P3-	USB_HUB3OUT_DM	NA	IO, DIFF	This Pin Connected to USB Switch 2 For M.2 PCIe(J33) And 10.1 LVDS Touch (J32)
88	USB_P2-	USB_HUB2OUT_DM	NA	IO, DIFF	USB 2.0 Host Port2 Data negative. This pin is connected to Dual stack USB3.0 Type A connector (J22B) Top port.
89	USB_P3+	USB_HUB3OUT_DP	NA	IO, DIFF	This Pin Connected to USB Switch 2 For M.2 PCIe(J33) And 10.1 LVDS Touch (J32)
90	USB_P2+	USB_HUB2OUT_DP	NA	IO, DIFF	USB 2.0 Host Port2 Data negative. This pin is connected to Dual stack USB3.0 Type A connector (J22B) Top port.
91	USB_VBUS	VBUS_OTG1	USB_OTG1_VBUS/ A39	O, 5V Power	Reference voltage to USB controller.
92	USB_ID	USB_ID	USB_OTG1_ID/ A37	O, 3.3V CMOS	USB OTG ID. This pin is connected from Micro USB OTG connector (J1).(Optional)
93	USB_P1-	USB_OTG1_DM	USB_OTG1_DM / C39	IO, DIFF	USB 2.0 OTG Port1 Data negative. This pin is connected to Micro USB OTG connector (J1).

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
94	USB_P0-	USB_HUB1OUT_DM	NA	IO, DIFF	USB 2.0 Host Port0 Data negative. This pin is connected to USB Type A combo connector (J22A) (from the USB HUB output port1 of the I.MX8 SOM).
95	USB_P1+	USB_OTG1_DP	USB_OTG1_DP / B40	IO, DIFF	USB 2.0 OTG Port1 Data positive. This pin is connected to Micro USB OTG connector (J1).
96	USB_P0+	USB_HUB1OUT_DP	NA	IO, DIFF	USB 2.0 Host Port0 Data positive. This pin is connected to USB Type A combo connector (J22A) (from the USB HUB output port1 of the I.MX8 SOM).
97	GND	GND	NA	Power	Ground.
98	GND	GND	NA	Power	Ground.
99	eDP0_TX0+/ LVDS_A0+	LVDS1_CH0_TX0_P	LVDS1_CH0_TX0_P/ BN37	LVDS, DIFF	LVDS primary channel differential pair0 positive. This pin is connected to LVDS Receiver.
100	eDP1_TX0+/ LVDS_B0+	LVDS1_CH1_TX0_P	LVDS1_CH1_TX0_P/ BN33	LVDS, DIFF	LVDS secondary channel differential pair0 positive. This pin is connected to secondary LVDS connector (J30) in carrier board.
101	eDP0_TX0-/ LVDS_A0-	LVDS1_CH0_TX0_N	LVDS1_CH0_TX0_N/ BL37	LVDS, DIFF	LVDS primary channel differential pair0 negative. This pin is connected to LVDS Receiver.
102	eDP1_TX0-/ LVDS_B0-	LVDS1_CH1_TX0_N	LVDS1_CH1_TX0_N/ BL33	LVDS, DIFF	LVDS secondary channel differential pair0 negative. This pin is connected to secondary LVDS connector (J30) in carrier board.
103	eDP0_TX1+/ LVDS_A1+	LVDS1_CH0_TX1_P	LVDS1_CH0_TX1_P/ BM38	LVDS, DIFF	LVDS primary channel differential pair1 positive. This pin is connected to LVDS Receiver.
104	eDP1_TX1+/ LVDS_B1+	LVDS1_CH1_TX1_P	LVDS1_CH1_TX1_P/ BM32	LVDS, DIFF	LVDS secondary channel differential pair1 positive.

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
					This pin is connected to secondary LVDS connector (J30) in carrier board.
105	eDP0_TX1-/ LVDS_A1-	LVDS1_CH0_TX1_N	LVDS1_CH0_ TX1_N/ BK38	LVDS, DIFF	LVDS primary channel differential pair1 negative. This pin is connected to LVDS Receiver.
106	eDP1_TX1-/ LVDS_B1-	LVDS1_CH1_TX1_N	LVDS1_CH1_ TX1_N/ BK32	LVDS, DIFF	LVDS secondary channel differential pair1 negative. This pin is connected to secondary LVDS connector (J30) in carrier board.
107	eDP0_TX2+/ LVDS_A2+	LVDS1_CH0_TX2_P	LVDS1_CH0_ TX2_P/ BN39	LVDS, DIFF	LVDS primary channel differential pair2 positive. This pin is connected to LVDS Receiver.
108	eDP1_TX2+/ LVDS_B2+	LVDS1_CH1_TX2_P	LVDS1_CH1_ TX2_P/ BN31	LVDS, DIFF	LVDS secondary channel differential pair2 positive. This pin is connected to secondary LVDS connector (J30) in carrier board.
109	eDP0_TX2-/ LVDS_A2-	LVDS1_CH0_TX2_N	LVDS1_CH0_ TX2_N/ BL39	LVDS, DIFF	LVDS primary channel differential pair2 negative. This pin is connected to LVDS Receiver.
110	eDP1_TX2-/ LVDS_B2-	LVDS1_CH1_TX2_N	LVDS1_CH1_ TX2_N/ BL31	LVDS, DIFF	LVDS secondary channel differential pair2 negative. This pin is connected to secondary LVDS connector (J30) in carrier board.
111	LVDS_PPEN	LCD1_VDD_EN(GPIO1_14)	LVDS1_I2C1_ SCL/ BD32	I, 3.3V CMOS/ 10K PU	LCD Panel Power Enable.
112	LVDS_BLEN	LCD1_EN(GPIO1_09)	LVDS0_I2C1_ SDA/ BE35	I, 3.3V CMOS/ 10K PU	LCD Panel Backlight Enable Control.
113	eDP0_TX3+/ LVDS_A3+	LVDS1_CH0_TX3_P	LVDS1_CH0_ TX3_P/ BM40	LVDS, DIFF	LVDS primary channel differential pair3 positive. This pin is connected to LVDS Receiver.
114	eDP1_TX3+/ LVDS_B3+	LVDS1_CH1_TX3_P	LVDS1_CH1_ TX3_P/	LVDS, DIFF	LVDS secondary channel differential pair3 positive.

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
			BM30		This pin is connected to secondary LVDS connector (J30) in carrier board.
115	eDP0_TX3-/ LVDS_A3-	LVDS1_CH0_TX3_N	LVDS1_CH0_ TX3_N/ BK40	LVDS, DIFF	LVDS primary channel differential pair3 negative. This pin is connected to LVDS Receiver.
116	eDP1_TX3-/ LVDS_B3-	LVDS1_CH1_TX3_N	LVDS1_CH1_ TX3_N/ BK30	LVDS, DIFF	LVDS secondary channel differential pair3 negative. This pin is connected to secondary LVDS connector (J30) in carrier board.
117	GND	GND	NA	Power	Ground.
118	GND	GND	NA	Power	Ground.
119	eDP0_AUX+/ LVDS_A_CLK+	LVDS1_CH0_CLK_P	LVDS1_CH0_ CLK_P/ BM36	LVDS, DIFF	LVDS primary channel differential Clock positive. This pin is connected to LVDS Receiver.
120	eDP1_AUX+/ LVDS_B_CLK+	LVDS1_CH1_CLK_P	LVDS1_CH1_ CLK_P/ BM34	LVDS, DIFF	LVDS secondary channel differential Clock positive. This pin is connected to secondary LVDS connector(J30) in carrier board.
121	eDP0_AUX-/ LVDS_A_CLK-	LVDS1_CH0_CLK_N	LVDS1_CH0_ CLK_N/ BK36	LVDS, DIFF	LVDS primary channel differential Clock negative. This pin is connected to LVDS Receiver.
122	eDP1_AUX-/ LVDS_B_CLK-	LVDS1_CH1_CLK_N	LVDS1_CH1_ CLK_N/ BK34	LVDS, DIFF	LVDS secondary channel differential Clock negative. This pin is connected to secondary LVDS connector (J30) in carrier board.
123	LVDS_BLT_CTRL /GP_PWM_OUT 0	LCD1_BL_PWM(GP IO1_10) [1]	LVDS1_GPIO 00/ BD34	I, 3.3V CMOS/ 10K PU	RGB & LVDS LCD Panel Backlight Control.
124	GP_1-Wire_Bus	HDMI_TX0_CEC	HDMI_TX0_C EC/ BJ1	O, 3.3V CMOS	This pin is connected to HDMI connector (J25) in carrier board.
125	GP2_I2C_DAT/L VDS_DID_DAT	LVDS1_I2C0_SDA	LVDS1_I2C0_ SDA/E33	IO, 3.3V OD/	I2C3 Data.

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
					This pin is directly connected to Power I/O Header 1 (J24) 1st pin
126	eDP0_HPD# /LVDS_BLC_DAT	NC	NA	NA	NC in i.MX8 Qseven SOM. This pin is directly connected to. Power I/O Header 1 (J24) 11th pin
127	GP2_I2C_CLK /LVDS_DID_CLK	LVDS1_I2C0_SCL	LVDS1_I2C0_ SCL/BL35	I, 3.3V OD	I2C3 Clock. This pin is directly connected to Power I/O Header 1 (J24) 3st pin.
128	eDP1_HPD# /LVDS_BLC_CLK	NC	NA	NA	NC in i.MX8 Qseven SOM. This pin is directly connected to. Power I/O Header 1 (J24) 9th pin
129	CAN0_TX	FLEXCAN0_TX	FLEXCAN0_T X/H6	I, 3.3V CMOS	Transmit input for CAN0 bus. This pin is connected to CAN0 Transceiver.
130	CAN0_RX	FLEXCAN0_RX	FLEXCAN0_R X/C5	O, 3.3V CMOS	Receive output for CAN0 bus. This pin is connected from CAN0 Transceiver.
131	DP_LANE3+/ TMDS_CLK+	HDMI_TX0_CLK_P/ EDP3_P	HDMI_TX0_C LK_EDP3_P/B L3	I, HDMI or EDP	HDMI differential data lane clock positive. This pin is connected to Switch For DP/HDMI Function
132	USB_SSTX1-	USB3_HUB2_TXM	NA	I, USB SS	USB3.0 Host Port3 Transmit Differential pair negative. This pin is connected to Dual stack USB3.0 Type connector (J22B) Top port 1.
133	DP_LANE3-/ TMDS_CLK-	HDMI_TX0_CLK_N/ EDP3_N	HDMI_TX0_C LK_EDP3_N/ BK2	I, HDMI or EDP	HDMI differential data clock negative. This pin is connected to Switch For DP/HDMI Function
134	USB_SSTX1+	USB3_HUB2_TXP	NA	I, USB SS	USB3.0 Host Port3 Transmit Differential pair Positive. This pin is connected to Dual stack USB3.0 Type connector (J22B) Top port 1.
135	GND	GND	NA	Power	Ground.
136	GND	GND	NA	Power	Ground.
137	DP_LANE1+/ TMDS_LANE1+	HDMI_TX0_DATA1 _P/EDP1_P	HDMI_TX0_D ATA1_EDP1_ P /BL7	I, HDMI or EDP	HDMI differential data lane 1 positive. This pin is connected to Switch For DP/HDMI Function

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
138	DP_AUX+	EDP_AUX_P	HDMI_TX0_AUX_P / BH2	I, EDP	Connected To Display Port Aux Positive (J23)
139	DP_LANE1-/ TMDS_LANE1-	HDMI_TX0_DATA1_N/EDP1_N	HDMI_TX0_DATA1_EDP1_N /BM6	I, HDMI or EDP	HDMI differential data lane 1 negative. This pin is connected to Switch For DP/HDMI Function.
140	DP_AUX-	EDP_AUX_N	HDMI_TX0_AUX_N / BG3	I, EDP	Connected To Display Port Aux Negative (J23)
141	GND	GND	NA	Power	Ground.
142	GND	GND	NA	Power	Ground.
143	DP_LANE2+/ TMDS_LANE0+	HDMI_TX0_DATA0_P/EDP2_P	HDMI_TX0_DATA0_EDP2_P /BL5	I, HDMI or EDP	HDMI differential data lane 0 positive. This pin is connected to Switch For DP/HDMI Function.
144	USB_SSRX1-	USB3_HUB2_RXM	NA	O, USB SS	USB3.0 Host Port3 Transmit Differential pair Negative. This pin is connected to Dual stack USB3.0 Type connector (J22B) Top port 1.
145	DP_LANE2-/ TMDS_LANE0-	HDMI_TX0_DATA0_N/EDP2_N	HDMI_TX0_DATA0_EDP2_N /BM4	I, HDMI or EDP	HDMI differential data lane 0 negative. This pin is connected to Switch For DP/HDMI Function.
146	USB_SSRX1+	USB3_HUB2_RXP	NA	O, USB SS	USB3.0 Host Port3 Transmit Differential pair Positive. This pin is connected to Dual stack USB3.0 Type connector (J22B) Top port 1
147	GND	GND	NA	Power	Ground.
148	GND	GND	NA	Power	Ground.
149	DP_LANE0+/ TMDS_LANE2+	HDMI_TX0_DATA2_P/EDP0_P	HDMI_TX0_DATA2_EDP0_P /BL9	I, HDMI or EDP	HDMI differential data lane 2 positive. This pin is connected to Switch For DP/HDMI Function.
150	HDMI_CTRL_DAT	HDMI_TX0_CTRL_DAT	HDMI_TX0_DDC_SDA/ BN5	IO, 3.3V CMOS	HDMI I2C Data. This pin is connected to HDMI connector (J25) in carrier board.
151	DP_LANE0-/ TMDS_LANE2-	HDMI_TX0_DATA2_N/EDP0_N	HDMI_TX0_DATA2_EDP0_N /BM8	I, HDMI or EDP	HDMI differential data lane 2 negative. This pin is connected to Switch For DP/HDMI Function.

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
152	HDMI_CTRL_CLK	HDMI_TX0_CTRL_CLK	HDMI_TX0_DDC_SCL/ BG1	I, 3.3V CMOS	HDMI I2C Clock. This pin is connected to HDMI connector (J25) in carrier board.
153	DP_HDMI_HPD#	HDMI_TX_HPD	HDMI_TX0_HPD / BH8	O, 3.3V CMOS	HDMI hot plug detect. This pin is connected to HDMI connector (J25) in carrier board.
154	DP_HPD#	DP_HPD	DP_HPD(GPIO0_02)	I ,3.3 V	Display Port hot plug detect. This pin is connected to HDMI connector (J23) in carrier board.
155	PCIE_CLK_REF+	PCIE_A_REFCLK_P	NA	I, PCIe	PCIe differential reference clock positive. This pin is connected to M.2 Pcie(J31)
156	PCIE_WAKE#	PCIE_A_WAKE_B(GPIO4_28)	PCIE_CTRL0_WAKE_B/ A15	O, 3.3V CMOS/ 10K PU	PCIe wake event. This pin is connected to M.2 Pcie(J31)
157	PCIE_CLK_REF-	PCIE_A_REFCLK_N	NA	I, PCIe	PCIe differential reference clock negative. This pin is connected to M.2 Pcie(J31).
158	PCIE_RST#	PCIE_A_RST_B(GPIO4_29) [1]	PCIE_CTRL0_PERST_B/ D20	I, 3.3V CMOS	PCIe reset. This pin is connected to M.2 Pcie(J31)
159	GND	GND	NA	Power	Ground.
160	GND	GND	NA	Power	Ground.
161	PCIE3_TX+	NC	NA	NA	NC in i.MX8 Qseven SOM. This pin is connected to M.2 Pcie(J31).(Optional)
162	PCIE3_RX+	NC	NA	NA	NC in i.MX8 Qseven SOM. This pin is connected to M.2 Pcie(J31).(Optional)
163	PCIE3_TX-	NC	NA	NA	NC in i.MX8 Qseven SOM. This pin is connected to M.2 Pcie(J31).(Optional)
164	PCIE3_RX-	NC	NA	NA	NC in i.MX8 Qseven SOM. This pin is connected to M.2 Pcie(J31).(Optional)
165	GND	GND	NA	Power	Ground.
166	GND	GND	NA	Power	Ground.
167	PCIE2_TX+	NC	NA	NA	NC in i.MX8 Qseven SOM.

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
					This pin is connected to M.2 Pcie(J31).(Optional)
168	PCIE2_RX+	NC	NA	NA	NC in i.MX8 Qseven SOM. This pin is connected to M.2 Pcie(J31).(Optional)
169	PCIE2_TX-	NC	NA	NA	NC in i.MX8 Qseven SOM. This pin is connected to M.2 Pcie(J31).(Optional)
170	PCIE2_RX-	NC	NA	NA	NC in i.MX8 Qseven SOM. This pin is connected to M.2 Pcie(J31).(Optional)
171	UART0_TX	UART0_TX	UART0_TX /AV48	I, 3.3V CMOS	SCIFB2 interface serial data transmitter. This pin is connected to Data UART Header (J6) 05th Pin. Optinaly Connect with M.2 PCIe
172	UART0_ RTS#	UART0_RTS_B	UART0_RTS_ B /AU45	I, 3.3V CMOS	SCIFB2 interface ready to receive handshake signal. This pin is connected to Data UART Header (J6) 02th Pin.
173	PCIE1_TX+	PCIE1_B_TX0_P	PCIE1_TX0_P /B24	I, PCIe	This pin is connected to M.2 PCIe connector (J31) in carrier board.
174	PCIE1_RX+	PCIE1_B_RX0_P	PCIE1_RX0_P /A21	O, PCIe	This pin is connected to M.2 PCIe connector (J31) in carrier board
175	PCIE1_TX-	PCIE1_B_TX0_N	PCIE1_TX0_N /C25	I, PCIe	This pin is connected to M.2 PCIe connector (J31) in carrier board
176	PCIE1_RX-	PCIE1_B_RX0_N	PCIE1_RX0_N /B22	O, PCIe	This pin is connected to M.2 PCIe connector (J31) in carrier board
177	UART0_RX	UART0_RX	UART0_RX /AV50	O, 3.3V CMOS	SCIFB2 interface serial data receiver. This pin is connected from Data UART Header (J6) 04th Pin.
178	UART0_CTS#	UART0_CTS_B	UART0_CTS_ B /AW49	O, 3.3V CMOS	SCIFB2 interface ready to send handshake signal. This pin is connected from Data UART Header (J6) 02nd Pin.
179	PCIE0_TX+	PCIE0_A_TX0_P	PCIE0_TX0_P /B26	I, DIFF	PCIe Channel0 Transmit data output positive. This pin is connected to M.2 PCIe connector (J31) in carrier board.

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
180	PCIE0_RX+	PCIE0_A_RX0_P	PCIE0_RX0_P /A29	O, DIFF	PCIe Channel0 Receive data input positive. This pin is connected to M.2 PCIe connector (J31) in carrier board.
181	PCIE0_TX-	PCIE0_A_TX0_N	PCIE0_TX0_N /C27	I, DIFF	PCIe Channel0 Transmit data output negative. This pin is connected to M.2 PCIe connector (J31) in carrier board.
182	PCIE0_RX-	PCIE0_A_RX0_N	PCIE0_RX0_N /B30	O, DIFF	PCIe Channel0 Receive data input negative. This pin is connected to M.2 PCIe connector (J31) in carrier board.
183	GND	GND	NA	Power	Ground.
184	GND	GND	NA	Power	Ground.
185	LPC_AD0/ GPIO0	Q7_GPIO_0(GPIO3_12)	SAI1_RXC/AV6	IO,3.3VCMOS/ 10K PU	General purpose Input/Output0. This Pin is Connected From Capacitive Touch (J15) For RGB Display
186	LPC_AD1/ GPIO1	Q7_GPIO_1(GPIO3_02)	SPI0_SCK/BB4	IO,3.3VCMOS/ 10K PU	General purpose Input/Output1. This pin is connected to M.2 PCIe and M.2 Sata
187	LPC_AD2 / GPIO2	Q7_GPIO_2(GPIO3_14)	SAI1_RXFS/AU3	IO,3.3VCMOS/ 10K PU	General purpose Input/Output2. This GPIO is used for Mic Input Detect and connected from Audio IN Jack. (J8)
188	LPC_AD3/ GPIO3	Q7_GPIO_3(GPIO3_11)	SPI2_CS1/AY2	IO,3.3VCMOS/ 10K PU	General purpose Input/Output3. This GPIO is used for Headphone Detect and connected from Audio Out Jack.*(J7)*
189	LPC_CLK/ GPIO4	Q7_GPIO_4(GPIO1_08)	LVDS0_I2C1_SCL/BE37	IO, 3.3V CMOS	General purpose Input/Output4. This GPIO is used for CAN0 Transceiver Power down control and connected to CAN transceiver.
190	LPC_FRAME#/ GPIO5	Q7_GPIO_5(GPIO1_11)	LVDS1_GPIO01/BH36	IO,3.3VCMOS/ 10K PU	M.2 Pcie Reset Control. Optionally connect With M.2 Sata
191	SERIRQ / GPIO6	Q7_GPIO_6(GPIO5_00)	PCIE_CTRL1_PERST_B/G25	IO,3.3VCMOS/ 10K PU	Connected With LVDS LCD Panel Power Enable.
192	LPC_LDRQ#/ GPIO7	Q7_GPIO_7(GPIO0_00)	LSIO.GPIO0.IO00/AL45	IO, 3.3V CMOS	M.2 Host Wake Connected With M.2 SATA Optionally Connected With M.2 PCIe

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
193	VCC_RTC	VDD_RTC	NA	O, 3V Power	3V backup coin cell input for RTC.
194	SPKR/ GP_PWM_OUT2	PWM2(GPIO0_19) [1]	LSIO.GPIO0.IO19/ BA51	I, 3.3V CMOS	Buzzer control PWM input. This pin is connected to buzzer in carrier board. *Note: Also, this pin is used as a GPIO for LVDS LCD Backlight control through resistor and default populated.*
195	FAN_TACHOIN/ GP_TIMER_IN	Q7_FAN_TECHOIN(GPIO0_01)	LSIO.GPIO0.IO01/AP48	I, 3.3V CMOS	This pin is connected to Fan Header (J26) 04th Pin in carrier board.
196	FAN_PWMOUT/ GP_PWM_OUT1	PWM3(GPIO0_16) [1]	PWM3(GPIO0_16)/ AW53	I, 3.3V CMOS	Fan Control PWM input. This pin is connected to Fan Header (J26) 2nd Pin.
197	GND	GND	NA	Power	Ground.
198	GND	GND	NA	Power	Ground.
199	SPI_MOSI	SPI3_MOSI [1]	SPI3_MOSI/ BF2	I, 3.3V CMOS	SPI Master Out Slave In. Connected With SPI Flash /Power I/O Header (J3) 3rd Pin
200	SPI_CS0#	SPI3_CS0	SPI3_CS0/BG5	I, 3.3V CMOS/ 10K PU	SPI Chip Select1. This Pin is connected to SPI Flash.
201	SPI_MISO	SPI3_MISO	SPI3_MISO/BE5	O, 3.3V CMOS	SPI Master In Slave Out. Connected With SPI Flash /Power I/O Header (J3) 1rd Pin
202	SPI_CS1#	SPI3_CS1 [1]	SPI3_CS1/BD8	I, 3.3V CMOS	SPI Chip Select2. Connected With SPI Flash /Power I/O Header (J3) 2nd Pin.
203	SPI_SCK	SPI3_SCLK	SPI3_SCLK/BF6	I, 3.3V CMOS	SPI Clock. This Pin is connected to SPI Flash. /Power I/O Header (J3) 6rd Pin.
204	MFG_NC4	NC	NA	NA	NC in i.MX8 Qseven SOM. JTAG Test Reset. This pin is connected from Debug to USB Conversion Section. And Controlled with Dip Switch sw4 4th pin
205	VCC_5V_SB1	NC	NA	NA	NC in i.MX8 Qseven SOM. This pin is connected to 5V standby power supply in carrier board.
206	VCC_5V_SB2	NC	NA	NA	NC in i.MX8 Qseven SOM. This pin is connected to 5V standby power supply in carrier board.

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
207	MFG_NC0	JTAG_TCK	JTAG_TCK/ BC51	O, 3.3V CMOS/ 10K PD	JTAG Test Clock. This pin is connected from JTAG Header (J16) 09th Pin through buffer.
208	MFG_NC2	UART4_RX/JTAG_TDI	DMA.UART4.RX/AR47 or JTAG_TDI/ BE51	O, 3.3V CMOS	SCIFA2 serial data receiver. This pin is connected from Serial to USB converter for Debug console. And Connected With JTAG
209	MFG_NC1	UART4_TX/JTDO_UTX	DMA.UART4.TX/AU53 or JTAG_TDO/BD52	I, 3.3V CMOS	SCIFA2 serial data transmitter. This pin is connected to Serial to USB converter for Debug console. *This pin is also connected to JTAG Header.*
210	MFG_NC3	JTAG_TMS	JTAG_TMS/BA49	O, 3.3V CMOS/ 10K PU	JTAG Test Mode Select. This pin is connected from JTAG Header.
211	VCC	NC	NA	O, 5V Power	Supply Voltage.
212	VCC	NC	NA	O, 5V Power	Supply Voltage.
213	VCC	NC	NA	O, 5V Power	Supply Voltage.
214	VCC	NC	NA	O, 5V Power	Supply Voltage.
215	VCC	NC	NA	O, 5V Power	Supply Voltage.
216	VCC	NC	NA	O, 5V Power	Supply Voltage.
217	VCC	NC	NA	O, 5V Power	Supply Voltage.
218	VCC	NC	NA	O, 5V Power	Supply Voltage.
219	VCC	VCC_5V	NA	O, 5V Power	Supply Voltage.
220	VCC	VCC_5V	NA	O, 5V Power	Supply Voltage.
221	VCC	VCC_5V	NA	O, 5V Power	Supply Voltage.
222	VCC	VCC_5V	NA	O, 5V Power	Supply Voltage.
223	VCC	VCC_5V	NA	O, 5V Power	Supply Voltage.
224	VCC	VCC_5V	NA	O, 5V Power	Supply Voltage.
225	VCC	VCC_5V	NA	O, 5V Power	Supply Voltage.
226	VCC	VCC_5V	NA	O, 5V Power	Supply Voltage.
227	VCC	VCC_5V	NA	O, 5V Power	Supply Voltage.
228	VCC	VCC_5V	NA	O, 5V Power	Supply Voltage.
229	VCC	VCC_5V	NA	O, 5V Power	Supply Voltage.
230	VCC	VCC_5V	NA	O, 5V Power	Supply Voltage.

2.4 Serial Interface Features

2.4.1 Debug UART Interface

The i.MX 8 QM/QP Qseven development board supports debug interface through i.MX8 CPU's UART4 interface. This UART4 signals from Qseven MXM connector is connected to UART to USB Convertor "FT232RQ" and connected to USB Micro AB Connector (J2). This USB Micro AB Connector can be used for Debug purpose which is physically located at the top of the board as shown below.

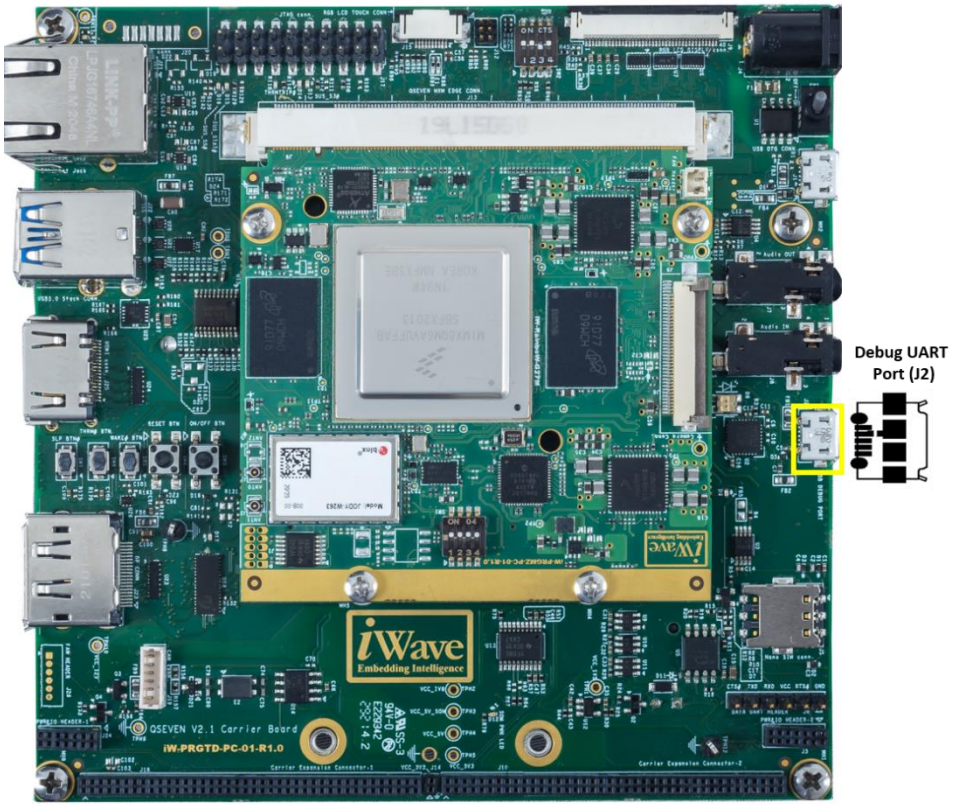


Figure 3: Debug UART Port

2.4.2 Data UART Interface

The i.MX 8 QM/QP Qseven carrier board supports full functional Data UART interface through i.MX8 CPU's UART0 interface. This UART0 signals from Qseven MXM connector is connected to 6pin Header (J6) for easy accessibilty. This Data UART header is physically located at the top of the board as shown below.

Number of Pins : 6

Connector Part number : 5-146280-6 from TE Connectivity

Mating Connector : 534237-4 from TE Connectivity

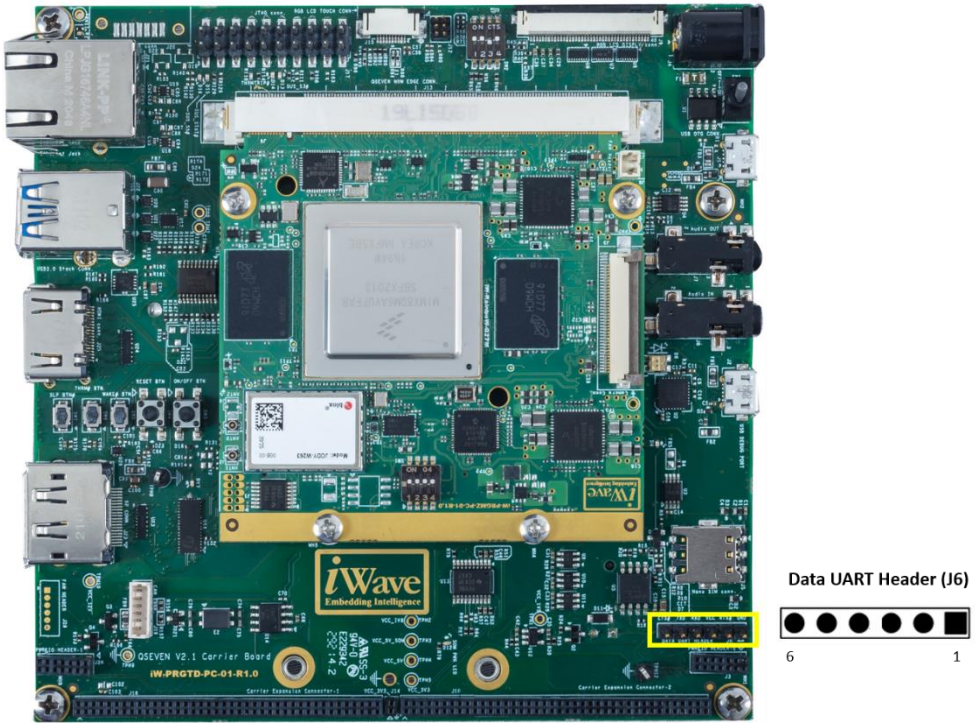


Figure 4: Data UART Header

Table 4: Data UART Header Pinout

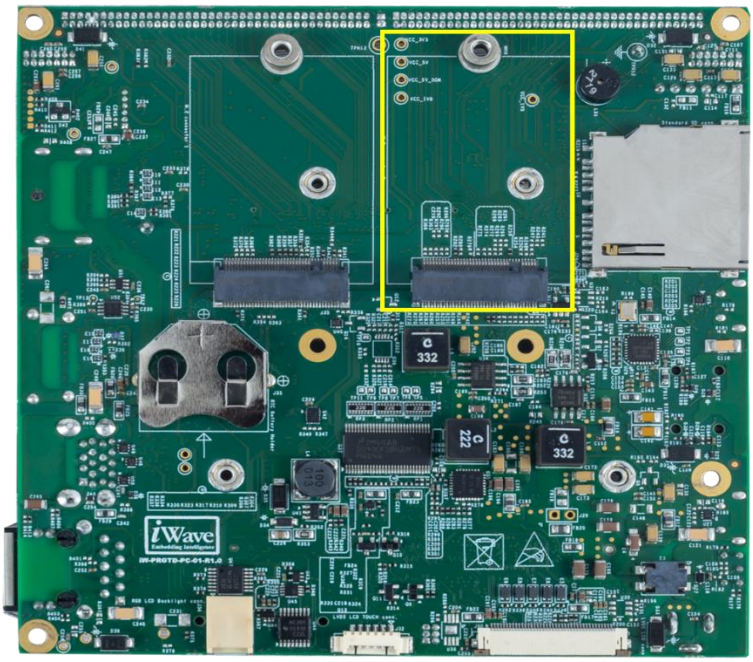
Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	GND	GND	Power	Ground.
2	CTS#	UART0_RTS#	O, 3.3V CMOS	UART0 interface Clear to Send signal.
3	VCC	VCC_UART	O, 3.3V Power	3.3V Supply Voltage. (optional)
4	TXD	UART0_RXD	I, 3.3V CMOS	UART0 interface Receive signal.
5	RXD	UART0_TXD	O, 3.3V CMOS	UART0 interface Transmit signal.
6	RTS#	UART0_CTS#s	I, 3.3V CMOS	UART0 interface Ready to Send signal.

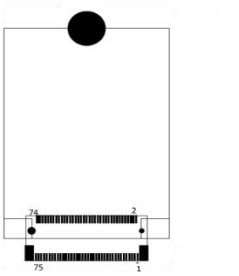
2.5 High Speed Interface Features

2.5.1 PCIe Interface

The i.MX 8 QM/QP Qseven Development platform by default supports two PCIe Lanes PCIe0 and PCIe1. PCIe0 lane supported through i.MX8 CPU's PCIe0 Interface and other PCIe1 lane supported through i.MX8 CPU's PCIe1 Interface.

Both PCIe0 and PCIe1 lanes from Qseven MXM connector are connected to PCIe lane0 PCIe lane1 of M.2 connecter respectively. M.2 PCIe connector (J31) is physically located at the bottom of the board as shown below.





M.2 Key-B/Key-M Connector (J31)

Figure 5: M.2 PCIe Connector

Table 5: M.2 PCIe Connector Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	CONFIG_3	M.2_1_CONFIG_3	3V3 ,10K PU	M.2 Configuration pin 3
2	3.3 V1	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
3	GND1	GND	Power	Ground.
4	3.3 V2	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
5	PERn3	GND	Power	Ground.
6	N/A1	M.2_PWR_OFF#	O, 3.3V CMOS 10K PU	M.2 Full card Power off Signal.
7	PERp3	NC	NC	NC
8	N/A2	Q7_GPIO_1(GPIO3_02)	O, 3.3V CMOS 10K PU	M.2 Wireless Disable Signal
9	GND2	USBP3-	IO, USB	USB2.0 Port3 Data Minus.
10	DAS/DSS	GPIO_SATA_ACT#(GPIO1_18)	O, 3.3V CMOS	Provide status indicators via LED.(D9) *Note: GPIO1_18 Connected Optionally.*

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
11	PETn3	GND	Power	Ground.
12	3.3 V3	NC	NC	NC.
13	PETp3	NC	NC	NC.
14	3.3 V4	NC	NC	NC.
15	GND3	NC	NC	NC.
16	3.3V5	NC	NC	NC.
17	PERn2	NC	NC	NC.
18	3.3 V6	NC	NC	NC.
19	PERp2	NC	NC	NC.
20	N/A3	NC	NC	NC
21	CONFIG_0	M.2_CONFIG_0	I, 1.8V CMOS 10K PU	M.2 Configuration Pin 0.
22	N/A4	NC	NC	NC
23	PETn2	PCIE2_TX-	NC	NC-on SOM Its Not Connected
24	N/A5	NC	NC	NC-on SOM Its Not Connected
25	PETp2	PCIE2_TX+	O, 1.8V CMOS	M.2 Dynamic Power Reduction Signal. *Note: GPIO1_29 Connected Optionally.*
26	N/A6	GNSS_DISABLE_2#	NC	Optional
27	GND4	GND	Power	Ground
28	N/A7	NC	NA	NC
29	PERn1	PCIE1_B_RX0_N	O, PCIe	PCIe Port1 Receive Pair Negative
30	N/A8	SIM_RST	O, SIM	This Pin Optionally Connect with Sim Reset
31	PERp1	PCIE1_RX0_P	O, PCIe	PCIe Port1 Receive Pair Positive
32	N/A9	SIM_CLK	I, SIM	This Pin Optionally Connect with Sim Clock
33	GND5	GND	Power	Ground
34	N/A10	SIM_DAT	IO, SIM	This Pin Optionally Connect with Sim Data
35	PETn1	PCIE1_B_TX0_N	I, PCIe	PCIe Port1 Transferring Pair Negative
36	N/A11	M2_UIM_PWR	O, SIM Power	This Pin is Connected for Sim Power
37	PETp1	PCIE1_B_TX0_P	I, PCIe	PCIe Port1 Transferring Pair Positive
38	DEVSLP	NC	NA	Optionally Connect With 3.3V PU/PD
39	GND6	GND	Power	Ground
40	SMB_CLK	DMA_I2C1_SCL	O,1.8 V CMOS	I2C Clock
41	SATA-B+/PERn0	PCIE0_A_RX0_N	I, PCIe	PCIe Port0 Receiving Pair Negative
42	SMB_DATA	DMA_I2C1_SDA	I0,1.8 V CMOS	I2C Data
43	SATA-B-/PERp0	PCIE0_A_RX0_P	O, PCIe	PCIe Port0 Receiving Pair Positive
44	ALERT#	SMBUS_ALERT(GPIO1_15)	I/O 1.8V CMOS	General Purpose input Output
45	GND7	GND	Power	Ground
46	N/A15	NC	NA	NC
47	SATA-A-/PETn0	PCIE_SATA0_TX0_N	I, PCIe	PCIe Channel A/B Receive Positive
48	N/A16	NC	NA	NC
49	SATA-A+/PETp0	PCIE_SATA0_TX0_P	I, PCIe	PCIe Channel A/B Receive Positive
50	PERST#	NC	NA	NC
51	GND8	GND	Power	Ground

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
52	CLKREQ#	NC	NA	NC
53	REFCLKN	PCIE_A_REFCLK_N	O, PCIe	PCIE Channel Clock Negative
54	PEWAKE#	NC	NA	NC
55	REFCLKP	PCIE_A_REFCLK_P	O, PCIe	PCIE Channel Clock Positive
56	MFG1(DATA)	NC	NA	NC
57	GND9	GND	Power	Ground
58	MFG2(CLOCK)	NC	NA	NC
59	M1	NC	NA	NC
60	M2	Q7_GPIO_5(GPIO1_11)	O,1.8V CMOS	M.2 Reset Signal Note: This signal is connected Optionally
61	M3	NC	NA	NC
62	M4	UART0_TX	O,1.8 CMOS	NC. UART0_TX It's Connected Optionally
63	M5	NC	NA	NC
64	M6	UART0_RX	O,1.8 CMOS	NC. UART0_RX It's Connected Optionally
65	M7	NC	NA	NC
66	M8	M.2_SIM_DETECT_2	NC	Optionally Connect With 10K PU/PD
67	N/A17	Q7_GPIO_5(GPIO1_11)	I,1.8V CMOS 10K PU	M.2 Reset Signal Note: This signal is connected Optionally
68	SUSCLK	M.2_2_SUSCLK	I,3.3V CMOS 33E Series	Optionally Connect 32.768 KHz Clock oscillator
69	CONFIG_1	M.2_2_CONFIG_1	I,1.8V CMOS 10K PU	M.2 Configuration Pin 1.
70	3.3 V7	VCC_3V3	O,3.3 V Power	3.3V Supply Voltage
71	GND10	GND	Power	Ground
72	3.3 V8	VCC_3V3	O,3.3 V Power	3.3V Supply Voltage
73	GND11	GND	Power	Ground
74	3.3 V9	VCC_3V3	O,3.3 V Power	3.3V Supply Voltage
75	CONFIG_2	M.2_2_CONFIG_2	I,1.8V CMOS 10K PU	m.2 Configuration PIN 2

2.5.2 M.2 SATA Interface

The i.MX 8 QM/QP Qseven carrier board supports M.2 SATA interface from PCIE_SATA0 of i.MX 8 QM/QP processor using M.2 SATA connector (J33). The Qseven carrier board also supports SATA activity LED (D17) on Top side of the board for SATA activity indication. This M.2 SATA Connecter is physically located at the top of the board.

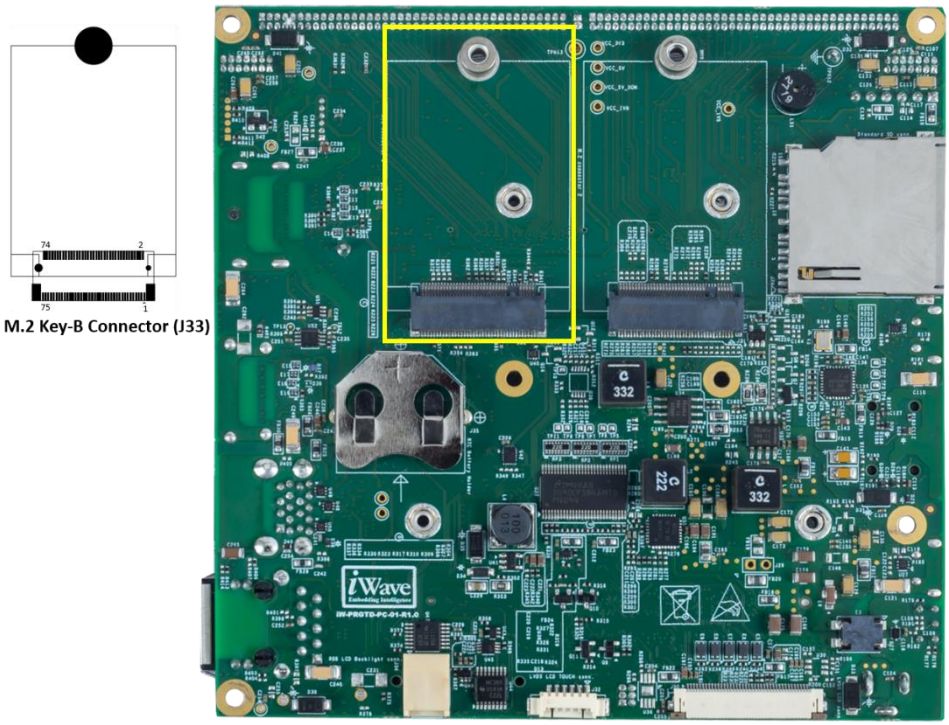


Figure 6: M.2 SATA Connector

Refer below table for the pinout is listed of M.2 SATA connector.

Table 6: M.2 SATA Connector Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	CONFIG_3	M.2_1_CONFIG_3	I, 3.3V CMOS 10K PU	M.2 Configuration Pin 3.
2	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
3	GND	GND	Power	Ground.
4	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
5	GND	GND	Power	Ground.
6	FULL_CARD_POWER _OFF# (O)(0/1.8V_3.3V)	M.2_PWR_OFF#	O, 3.3V CMOS 10K PU	M.2 Full card Power off Signal.
7	USB_D+	USB_HUB3OUT_DP	IO, USB	USB2.0 Host Port3 Data Plus.
8	W_DISABLE1# (O)(0/3.3V)	M.2_W_DISABLE1#	O, 3.3V CMOS	M.2 Wireless Disable Signal
9	USB_D-	USB_HUB3OUT_DM	IO, USB	USB2.0 Host Port3 Data Minus.
10	GPIO9(LED1#/DAS_D SS#)(I)(0/3.3V)	M.2_LED_1	O, 3.3V CMOS	Provide status indicators via LED
11	GND	GND	Power	Ground.
12	B1	NC	NC	NC.
13	B2	NC	NC	NC.
14	B3	NC	NC	NC.
15	B4	NC	NC	NC.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
16	B5	NC	NC	NC.
17	B6	NC	NC	NC.
18	B7	NC	NC	NC.
19	B8	NC	NC	NC.
20	GPIO5(AUDIO0/I2S_CLK(I/O)(0/1.8V)	NC	NC	NC.
21	CONFIG_0	M.2_CONFIG_0	I, 3.3V CMOS 10K PU	M.2 Configuration Pin 0.
22	GPIO6_(AUDIO1/I2S_RX) (I/O)(0/1.8V)	NC	NC	NC.
23	GPIO11(WOWWAN#/HSIC_DATA(1.2V))(I/O) (0/1.8V)	Q7_GPIO_7(GPIO0_00)	3.3V CMOS	M.2 Host Wake
24	GPIO7(AUDIO2/I2S_TX) (I/O)(0/1.8V)	NC	NC	NC.
25	DPR (O) (0/1.8V)	M.2_DPR	O, 1.8V CMOS 10K PU	M.2 Dynamic Power Reduction Signal.
26	GPIO10_(W_DISABLE_2#/HSIC_STROBE(1.2V)) (I/O)(0/1.8V)	NC	NA 10K PU	NC.
27	GND	GND	Power	Ground.
28	GPIO8(AUDIO3/I2S_WS)(I/O)(0/1.8V)	NC	NC	NC.
29	PERN1/USB30_RX-/SSIC_RX-	USB3_HUB3_RXM	I,O USB	USB 3.0 Receiving Data Negative
30	UIM-RESET (I)	M2_UIM_RST	O, SIM	SIM Card Reset Signal.
31	PERP1/USB30_RX+/SSIC_RX+	NC	NC	USB 3.0 Receiving Data Positive
32	UIM-CLK (I)	M2_UIM_CLK	I, SIM	SIM Card Clock Signal.
33	GND	GND	Power	Ground.
34	UIM-DATA (I/O)	M2_UIM_DAT	IO, SIM	SIM Card Data IO Signal.
35	PETN1/USB3.1-TX-/SSIC-TXN	NC	NC	USB 3.0 Transferring Data Negative
36	UIM-PWR (I)	M2_UIM_PWR	O, SIM Power	SIM Card Power.
37	PETP1/USB3.1-TX+/SSIC-TXP	NC	NC	USB 3.0 Transferring Data Positive
38	DEVSLP (O)	NC	NC	NC.
39	GND	GND	Power	Ground.
40	GPIO0(SMB_CLK/GNSS_SCL/SIM_DET2)(I/O)(0/1.8V)	DMA_I2C1_SCL	O, 1.8V CMOS	I2C CLK.
41	PERN0/SATA_B+	PCIE_SATA0_RX0_P	I,PCIe/SATA	PCIe Port 0 Receive Lane Positive.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
42	GPIO1(SMB_DATA/GNSS_SDA/UIM_DAT2)(I/O)/(0/1.8V)	DMA_I2C1_SDA	IO, 1.8V CMOS	I2C Data.
43	PERP0/SATA_B-	PCIE_SATA0_RX0_N	I,PCIe/SATA	PCIe Port 0 Receive Lane Negative.
44	GPIO2_(ALERT#/GNSS_IRQ/UIM_CLK2)(I)/(0/1.8V)	SMBUS_ALERT(GPIO1_15)	IO, 1.8V CMOS	General Purpose Input Output.
45	GND	GND	Power	Ground.
46	GPIO3(SYSCLK/GNSS_0/UIM_RST2)(I/O)(0/1.8V)	NC	NC	NC
47	PETN0/SATA_A-	PCIE_SATA0_TX0_N	O,PCIe/SATA	PCIe Transmit Lane Negative.
48	GPIO4(TX_BLK/GNSS_1/UIM_PWR2)(I/O)(0/1.8V)	NC	NC	NC
49	PETP0/SATA_A+	PCIE_SATA0_TX0_P	O,PCIe/SATA	PCIe Transmit pair Negative.
50	PERST# (O)(0/3.3V)	NC	-	NC
51	GND	GND	Power	Ground.
52	CLKREQ# (I/O)(0/3.3V)	NC	-	NC
53	REFCLKN	NC	NA	NC
54	PEWAKE# (I/O)(0/3.3V)	NC	-	NC
55	REFCLKP	NC	NA	NC
56	MFG_DATA	NC	NA	NC
57	GND	GND	Power	Ground.
58	MFG_CLOCK	I2C2_SCL	O, 3.3V CMOS	NC. *Optionally connected I2C Clock.*
59	ANTCTL0 (I)(0/1.8 V)	NC	NC	NC.
60	COEX3 (I/O)(0/1.8V)	Q7_GPIO_5(GPIO1_11)	I,O 3.3V CMOS	M.2 Reset Signel
61	ANTCTL1 (I)(0/1.8 V)	NC	NC	NC.
62	COEX_TXD (O)(0/1.8V)	UART0_TX	I,O 3.3V CMOS	UART Receiving signal Is Connected
63	ANTCTL2 (I)(0/1.8 V)	NC	NC	NC.
64	COEX_RXD (I)(0/1.8V)	UART0_RX	I,O 3.3V CMOS	UART Receiving signal Is Connected
65	ANTCTL3 (I)(0/1.8 V)	NC	NC	NC.
66	SIM_DETECT (I)	M.2_SIM_DETECT_1	10K PU with 3.3V	This pin is connect With Sim Detect Pin
67	RESET# (O)(0/1.8V)	Q7_GPIO_5(GPIO1_11)	I,O 3.3V CMOS	M.2 Reset Signal (OPTIONAL)

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
68	SUSCLK(32KHZ) (O)(0/3.3V)	M.2_2_SUSCLK	I, 32.768kHz Clock Supply	*Note: Optionally connected 32.768kHz Clock output*
69	CONFIG_1	M.2_CONFIG_1	I, 3.3V CMOS 10K PU	M.2 Configuration Pin 1.
70	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
71	GND	GND	Power	Ground.
72	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
73	GND	GND	Power	Ground.
74	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
75	CONFIG_2	M.2_CONFIG_2	I, 3.3V CMOS 10K PU	M.2 Configuration Pin 2.

2.5.3 Nano SIM Connecter: -

The i.MX 8 QM/QP Qseven carrier board supports Nano SIM connector to support the WWAN M.2 Modules. The Nano SIM connector (J5) is physically located on the top of the board

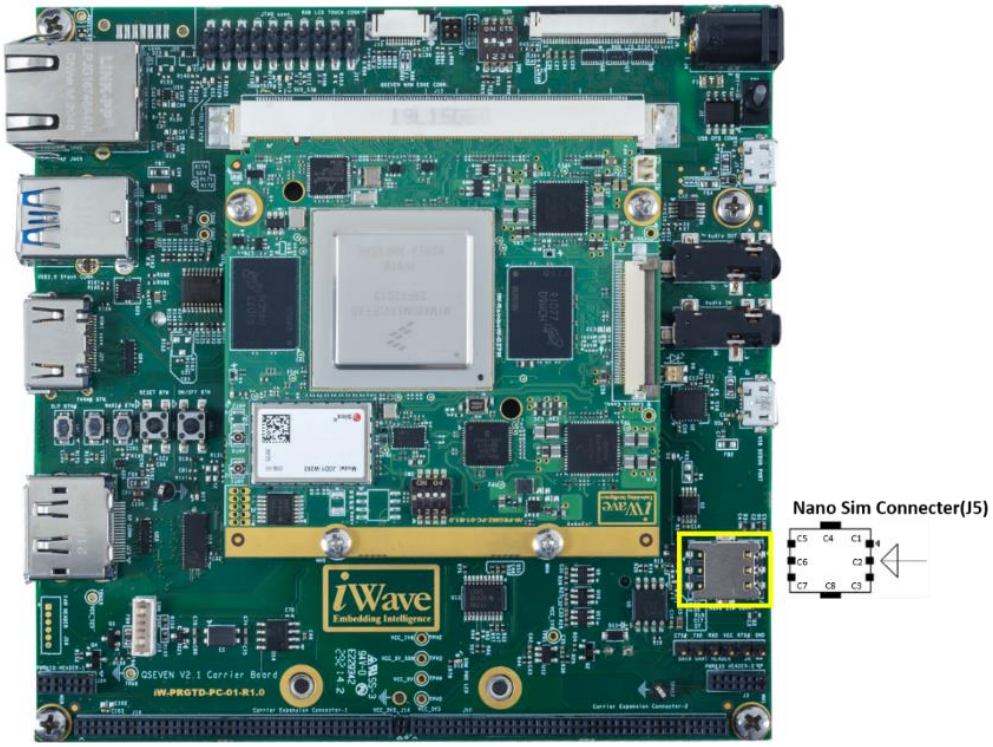


Figure 7: Nano Sim Connector

Table 7: Nano sim connector Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
C1	VCC	M2_UIM_PWR	Power	Sim Card Power Connect with M.2 Sata (optionally connect with M.2 PCIe)
C2	RST	SIM_RST	O, Signal	Sim Card Reset Signal Connect with M.2 Sata (optionally connect with M.2 PCIe)
C3	CLK	SIM_CLK	O, Signal	Sim Card Clock Signal Connect with M.2 SATA (optionally connect with M.2 PCIe)
C4	MH1	GND	Power	Ground
C5	GND	GND	Power	Ground
C6	VPP	NC	NA	Optionally Connected with M2_UIM_PWR
C7	IO	SIM_DAT	O, Signal	Sim Card data Signal Connect with M.2 Sata (optionally connect with M.2 PCIe)
C8	MH2	GND	Power	Ground

2.5.4 USB3.0 Host Interface

The i.MX 8 QM/QP Qseven carrier board supports Super Speed USB3.0 Host interface through on SOM USB3.0 Hub. This USB3.0 Both signals of Qseven MXM connector is directly connected to bottom port and Top of dual stack USB3.0 Type A connector (J22). Also, USB2.0 Port2 signals of Qseven MXM connector is connected to this connector for USB2.0 host interface from 3.0 USB Hub used on SOM.

The VBUS power of this USB3.0 connector is connected through current limit power switch and limit is set as 900mA. If connected USB3.0 device takes more than 900mA current, this power switch limits the current to constant mode and sends the over current indication signal to the over current indicator pin of Qseven MXM connector USB port 6 & 7. This USB3.0 connector (J22) is physically located at the top of the board as shown below.

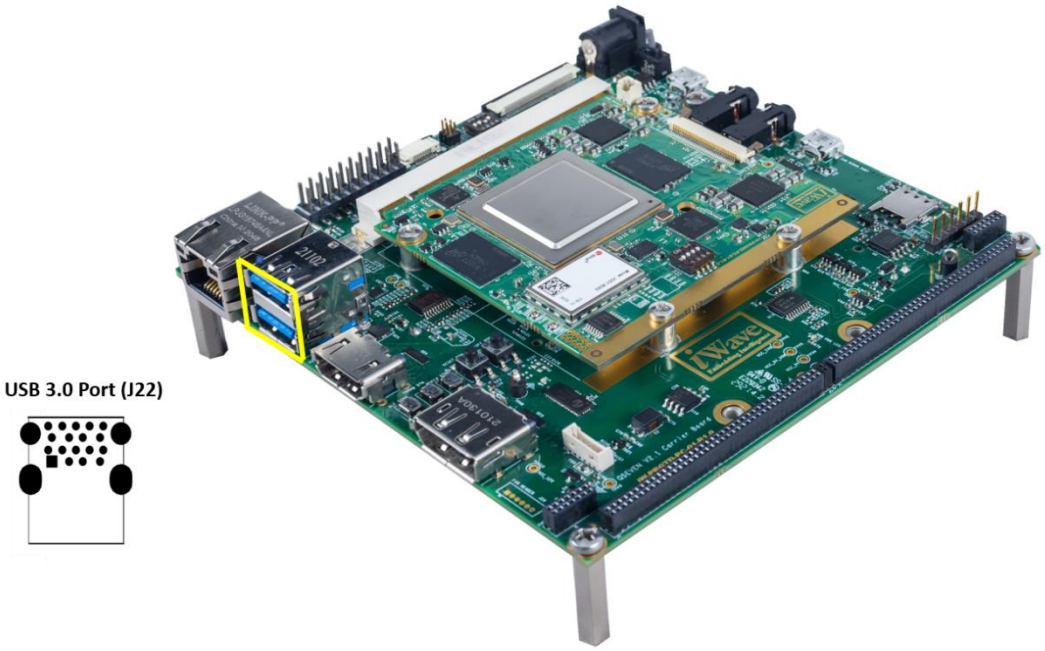


Figure 8: USB3.0 Host

2.6 Communication Interface Features

2.6.1 Gigabit Ethernet Interface

The i.MX 8 QM/QP Qseven development board supports Ethernet Port interface through on SOM Ethernet PHY which supports 10/100/1000Mbps Ethernet. The Ethernet PHY output signals from Qseven MXM connector GBE0 is directly connected to RJ45 Magjack (J21). Also, it supports Speed (Yellow) and Link/Activity (Green) LED indications on RJ45 Magjack. This RJ45 Magjack combo connector is physically located at the top of the board as shown below.

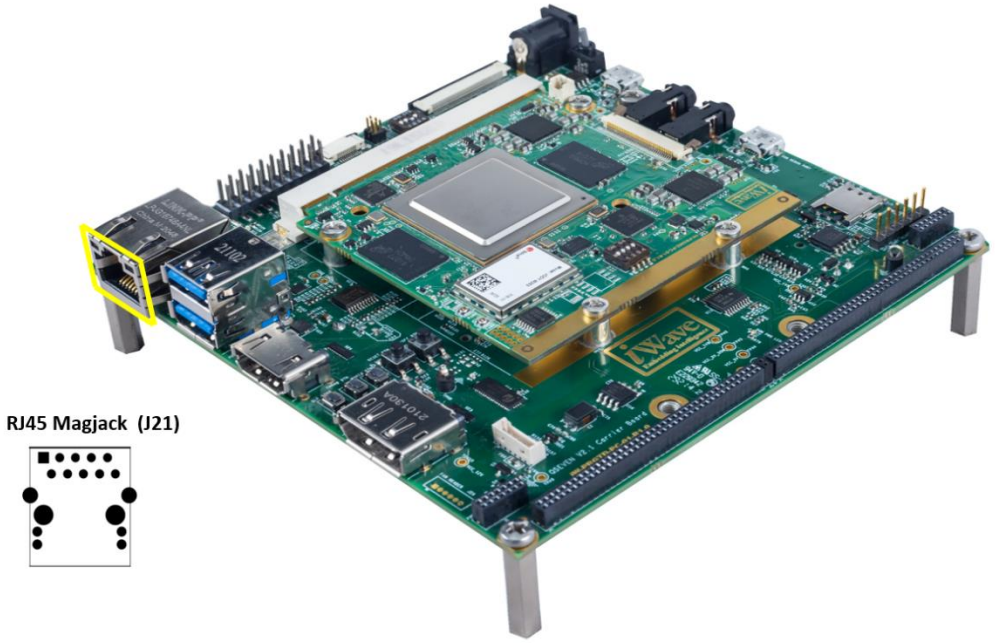


Figure 9: RJ45 Magjack

2.6.2 USB2.0 OTG Interface

The i.MX 8 QM/QP Qseven carrier Board supports USB2.0 High Speed OTG interface through i.MX8 CPU's USB_OTG1 interface. This USB2.0 Port1 signals of Qseven MXM connector is directly connected to USB2.0 Micro AB connector (J1)

This USB2.0 OTG connector is physically located at the top of the board as shown below.

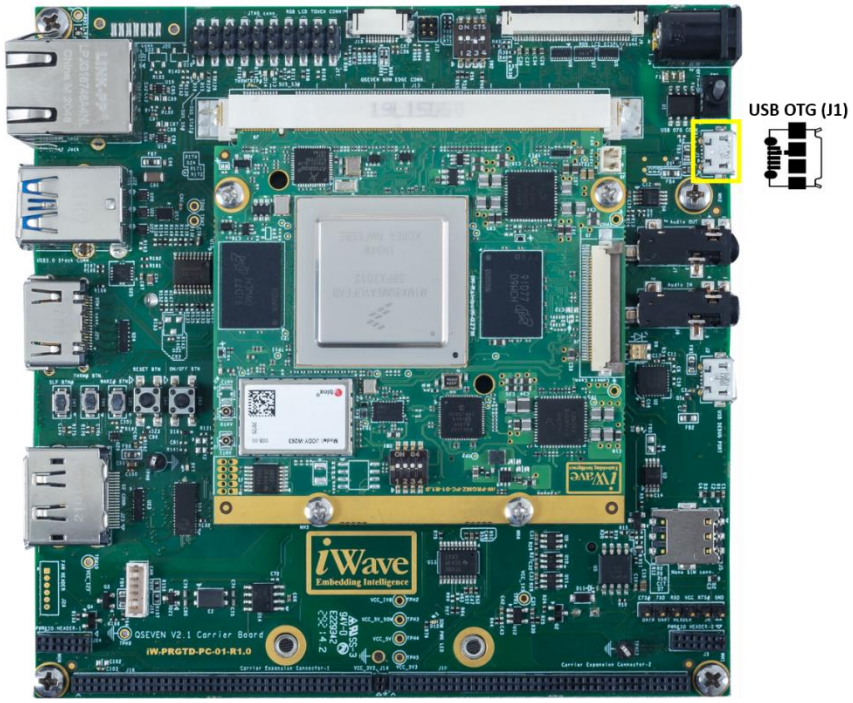


Figure 10: USB2.0 OTG

2.6.3 SDIO Interface

The i.MX 8 QM/QP Carrier Board supports SDIO interface through CPU's uSDHC1 interface. This uSDHC1 signals from Qseven MXM connector is connected to SD/MMC connector (J28) to support Standard SD interface. This connector supports up to 4-bit data transfer with card detect and write protect.

The main power to SD/MMC connector is 3.3V and it is connected through power switch to support power enable/disable feature. This power enable/disable is controlled from the SDIO_PWR# pin of Qseven MXM connector This SD/MMC connector (J28) is physically located at the bottom of the board as shown below.

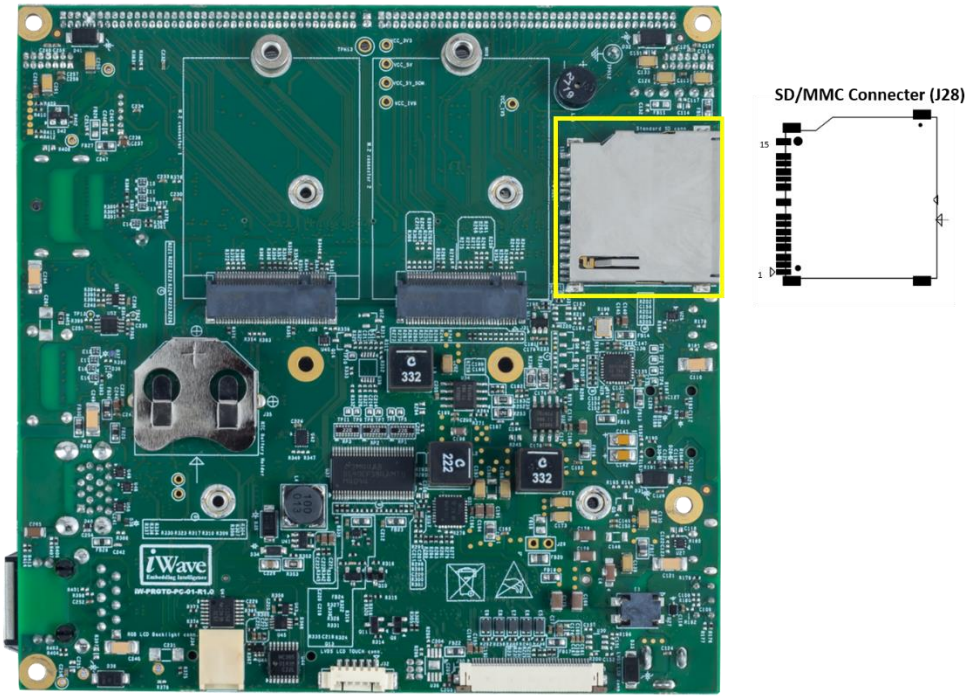


Figure 11:Standard SD Connector

2.6.4 CAN Interface

The i.MX 8 QM/QP Qseven Carrier Board supports CAN interface through i.MX 8 QM/QP CAN interface. This CAN1 interface signals from Qseven MXM connector (pins 129th & 130th) is connected to CAN Bus transceiver "MCP2562FD-E/SN" and to 6pin custom CAN header (J19. This CAN header is physically located at the top of the board as shown below.

Number of Pins : 6

Connector Part number : 53047-0610 from Molex

Mating Connector : 0510210600 from Molex with crimping pins

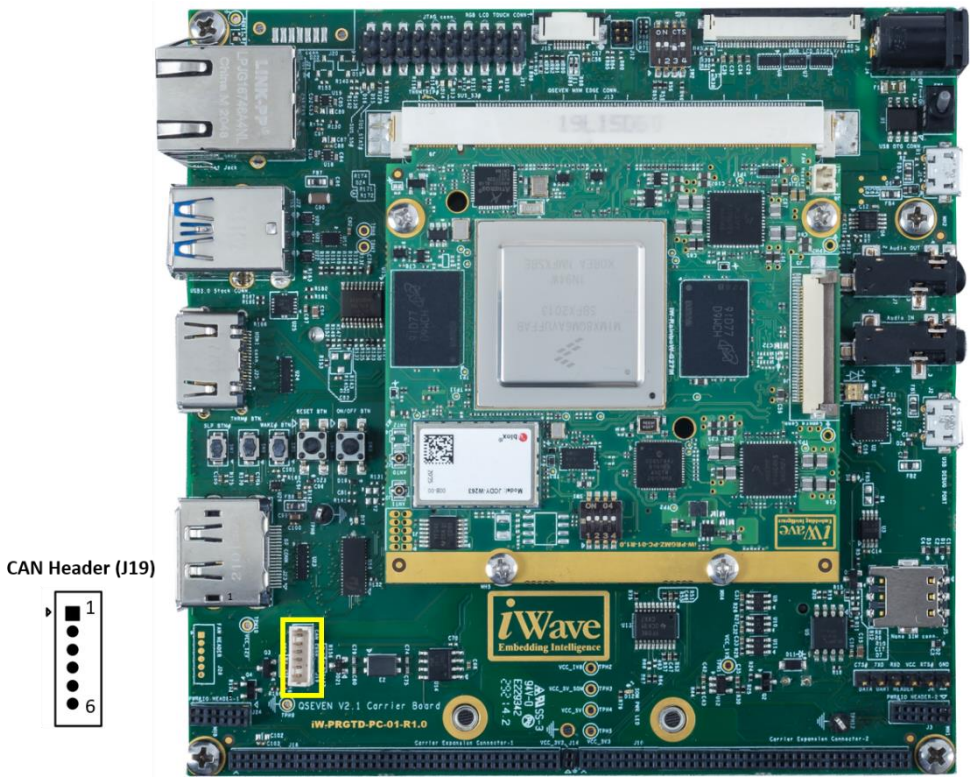


Figure 12: CAN Header

Table 8: CAN Header Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	VCC_5V	VCC_5V	O, 5V Power	5V Supply Voltage.
2	VCC_12V	NC	NA	*Note: Optionally connected to 12V supply Voltage.*
3	CANL	FLEXCAN0_TX	IO, DIFF	CAN0 Low-Level Voltage I/O
4	GND	GND	Power	Ground.
5	CANH	FLEXCAN0_RX	IO, DIFF	CAN0 High-Level Voltage I/O
6	GND	GND	Power	Ground.

2.7 Audio/Video Features

2.7.1 HDMI Interface

The i.MX 8 QM/QP CPU supports HDMI 2.0 audio/video out. HDMI Signals from the Qseven MXM connector along with HDMI DDC clock & data is connected to Standard HDMI Type-A connector with ESD protection circuitry.

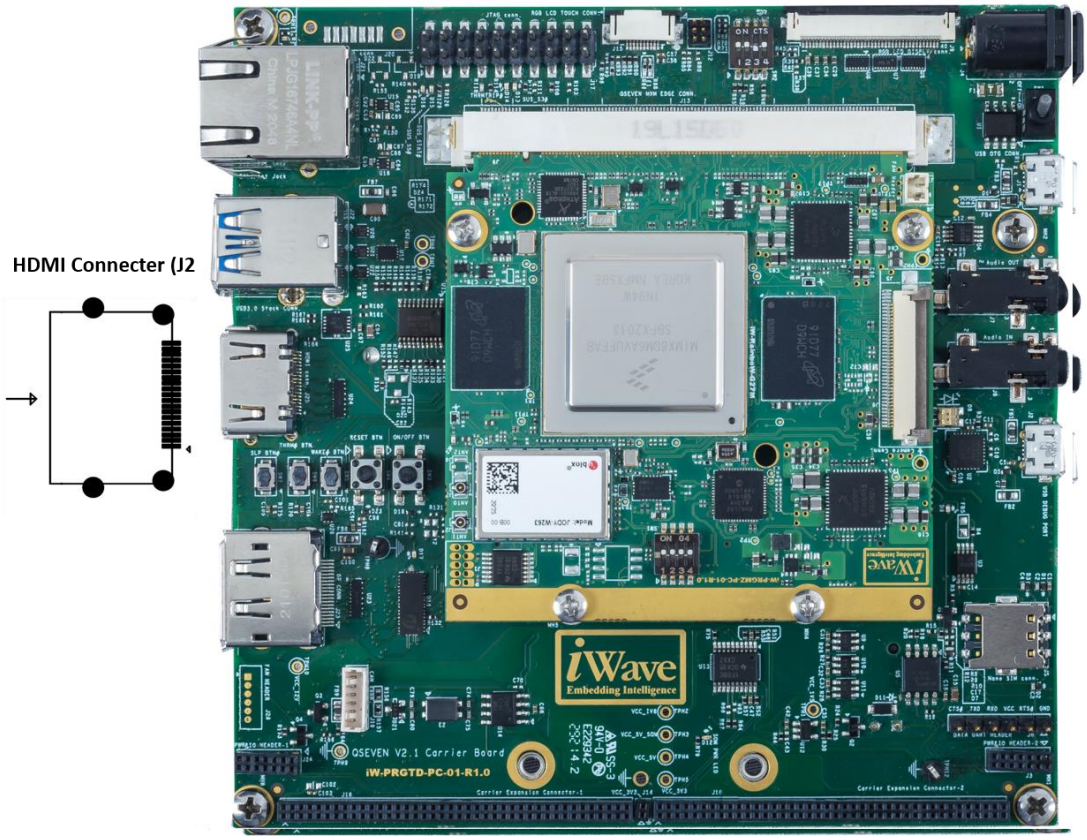


Figure 13: HDMI Output

2.7.2 Display Port Interface

The i.MX 8 QM/QP CPU supports Display Port (J23) Optional Feature On SOM, the i.MX 8 QM/QP CPU supports Either HDMI or DP. Contact iWave Technical Support team for display port supported SOM. In The Development Platform Through Switch (Refer 2.9.3 Switch) the data lines can shared from HDMI to DP. Display Port (J23) Connecter is physically placed on top.

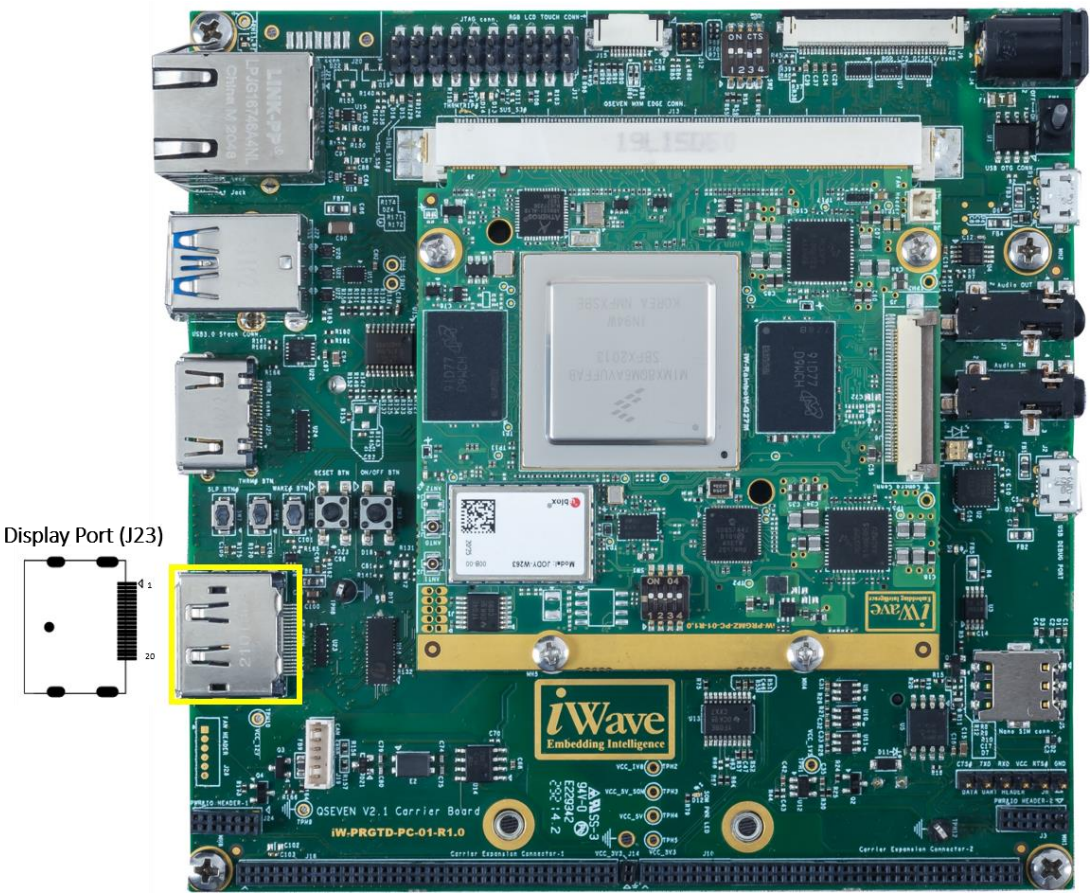


Figure 14: Display port

2.7.3 I2S Audio Interface

The i.MX 8 QM/QP Qseven carrier board supports Audio in and out through CPU's SAI1 interface which can support I2S format. This four wire I2S signals from Qseven MXM connector is connected to I2S Audio Codec "SGTL5000" to support Headphone Stereo output and Mono Mic input which is supported through 3.5mm Jack J7 and J8 correspondingly. Also, Headphone detect and Mic detect is supported through Qseven MXM connector pins GPIO3 (188th Pin) & GPIO2 (187th Pin) correspondingly. These Audio Jacks are physically located at the top of the board as shown below.

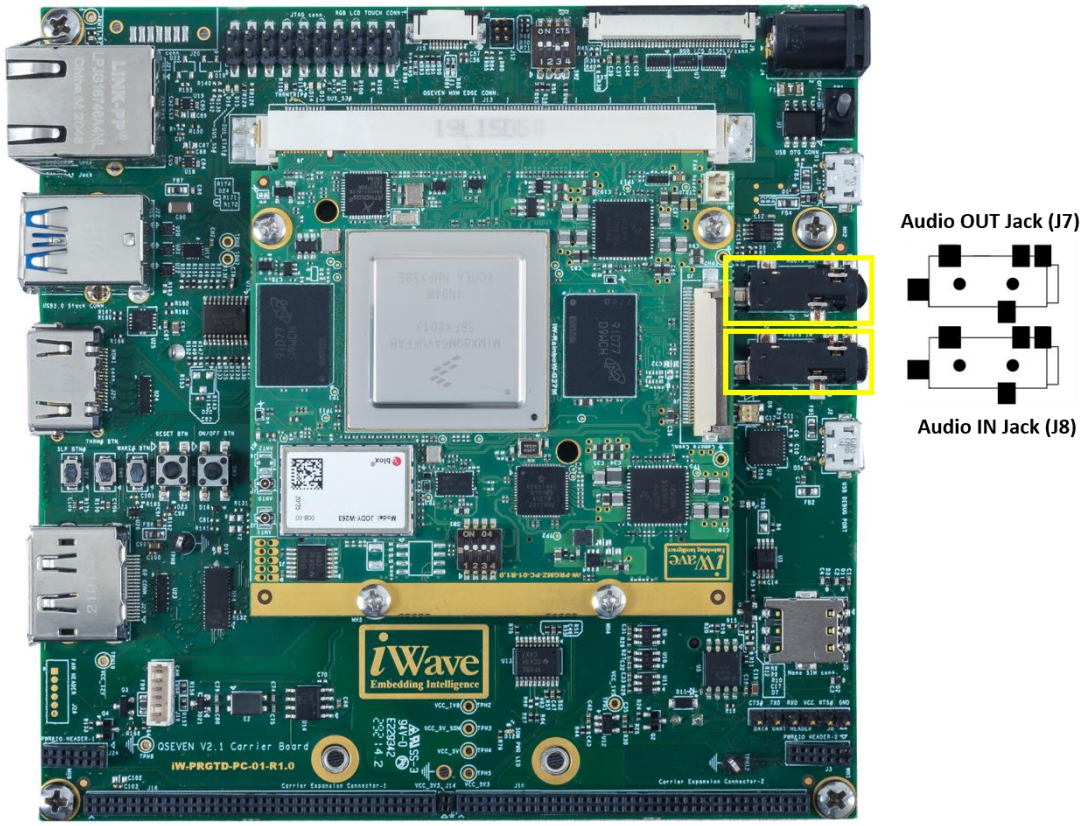


Figure 15: Audio Jack

2.7.4 7” LCD with Capacitive Touch

The i.MX 8 QM/QP Qseven carrier board supports 7inch, 18bpp RGB LCD “ETM070001ADH6” from Emerging Display Technologies Corporation (EDT) with capacitive touch panel. i.MX 8 CPU’s LVDS1_CH0 port is connected to primary LVDS channel of Qseven MXM connector. This primary LVDS interface signals are directly connected to LVDS transmitter (DS90CF384A) in carrier board which converts LVDS Interface signals to RGB and connects to RGB LCD connector (J9). This RGB LCD connector (J9) is physically located at the top of board as shown below.

This RGB LCD’s power enable and backlight enable is connected from LVDS_PPEN (111th pin) & LVDS_BLEN (112th pin) of Qseven MXM connector which is i.MX 8 CPU’s GPIO pins “GPIO01_14” and “GPIO01_09” respectively. Also, RGB LCD’s brightness is controlled from LVDS_BLT_CTRL (123rd pin) of Qseven MXM connector which is i.MX 8 CPU’s PWM(GPIOS_22).

Note: In i.MX 8 QM/QP carrier board, LVDS brightness control GPIO from Qseven MXM connector (123rd Pin) is shared to both primary & secondary LCD’s brightness control.

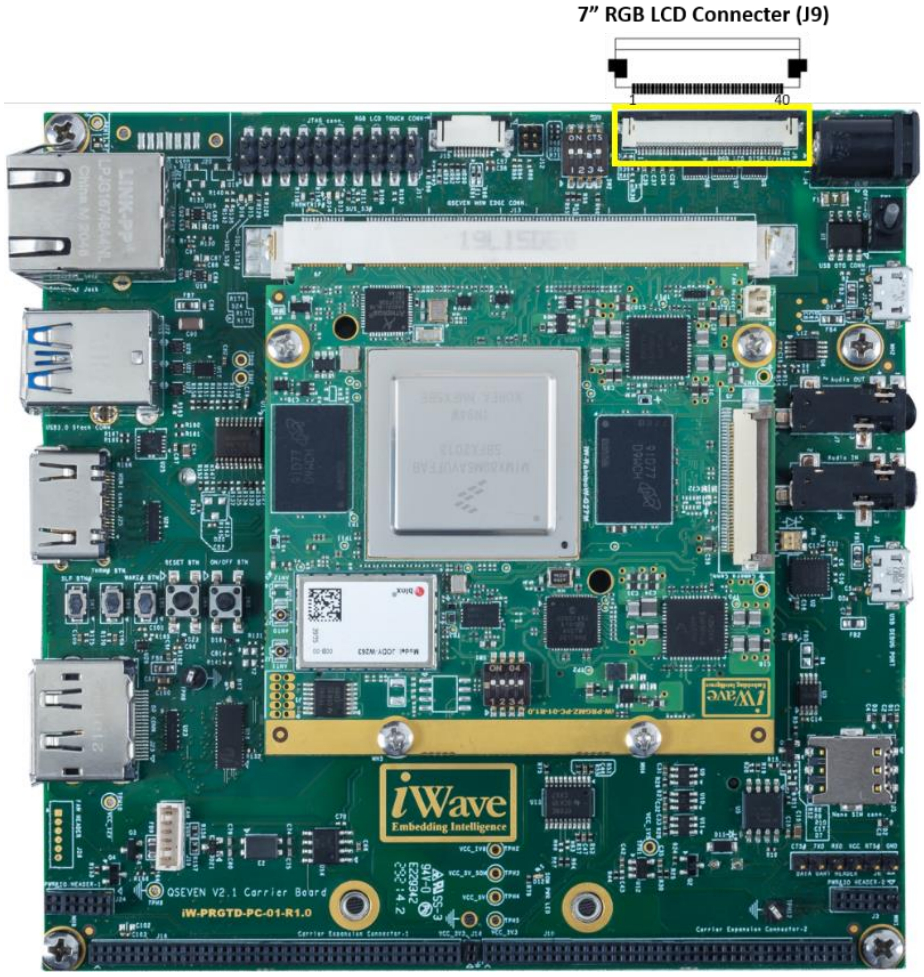


Figure 16: 7” RGB LCD Connector

Table 9: 7" RGB LCD Connector Pinouts

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	U/D	U/D	O, 3.3V CMOS	Up or Down Scanning Direction.
2	L/R	L/R	O, 3.3V CMOS	Left or Right Scanning Direction.
3	NC1	NC	-	-
4	VCC1	VCC1	O, 3.3V Power	3.3V Supply voltage for LED Driver Circuit.
5	VCC2	VCC2	O, 3.3V Power	3.3V Supply voltage for LED Driver Circuit.
6	VCC3	VCC3	O, 3.3V Power	3.3V Supply voltage for LED Driver Circuit.
7	VCC4	VCC4	O, 3.3V Power	3.3V Supply voltage for LED Driver Circuit.
8	NC2	NC	-	-
9	DE	DIS_DE	O, 3.3V CMOS	Data Enable Output.
10	VSS1	GND	Power	Ground.
11	VSS2	GND	Power	Ground.
12	VSS3	GND	Power	Ground.
13	B5	DIS_B7	O, 3.3V CMOS	Display Blue Data 7(MSB).
14	B4	DIS_B6	O, 3.3V CMOS	Display Blue Data 6.
15	B3	DIS_B5	O, 3.3V CMOS	Display Blue Data 5.
16	VSS4	GND	Power	Ground.
17	B2	DIS_B4	O, 3.3V CMOS	Display Blue Data 4.
18	B1	DIS_B3	O, 3.3V CMOS	Display Blue Data 3.
19	B0	DIS_B2	O, 3.3V CMOS	Display Blue Data 2(LSB).
20	VSS5	GND	Power	Ground.
21	G5	DIS_G7	O, 3.3V CMOS	Display Green Data 7(MSB).
22	G4	DIS_G6	O, 3.3V CMOS	Display Green Data 6.
23	G3	DIS_G5	O, 3.3V CMOS	Display Green Data 5.
24	VSS6	GND	Power	Ground.
25	G2	DIS_G4	O, 3.3V CMOS	Display Green Data 4.
26	G1	DIS_G3	O, 3.3V CMOS	Display Green Data 3.
27	G0	DIS_G2	O, 3.3V CMOS	Display Green Data 2(LSB).
28	VSS7	GND	Power	Ground.
29	R5	DIS_R7	O, 3.3V CMOS	Display Red Data 7(MSB).
30	R4	DIS_R6	O, 3.3V CMOS	Display Red Data 6.
31	R3	DIS_R5	O, 3.3V CMOS	Display Red Data 5.
32	VSS8	GND	Power	Ground.
33	R2	DIS_R4	O, 3.3V CMOS	Display Red Data 4.
34	R1	DIS_R3	O, 3.3V CMOS	Display Red Data 3.
35	R0	DIS_R2	O, 3.3V CMOS	Display Red Data 2(LSB).
36	VSS9	GND	Power	Ground.
37	NC3	NC	-	-
38	DCLK	DIS_CLK	O, 3.3V CMOS	DOT Data Clock.
39	HSYNC	DIS_HSYNC	O, 3.3V CMOS	Horizontal SYNC Output.
40	VSYNC	DIS_VSYNC	O, 3.3V CMOS	Vertical SYNC Output.

The below image shows capacitive touch connector located at the top of the carrier board.

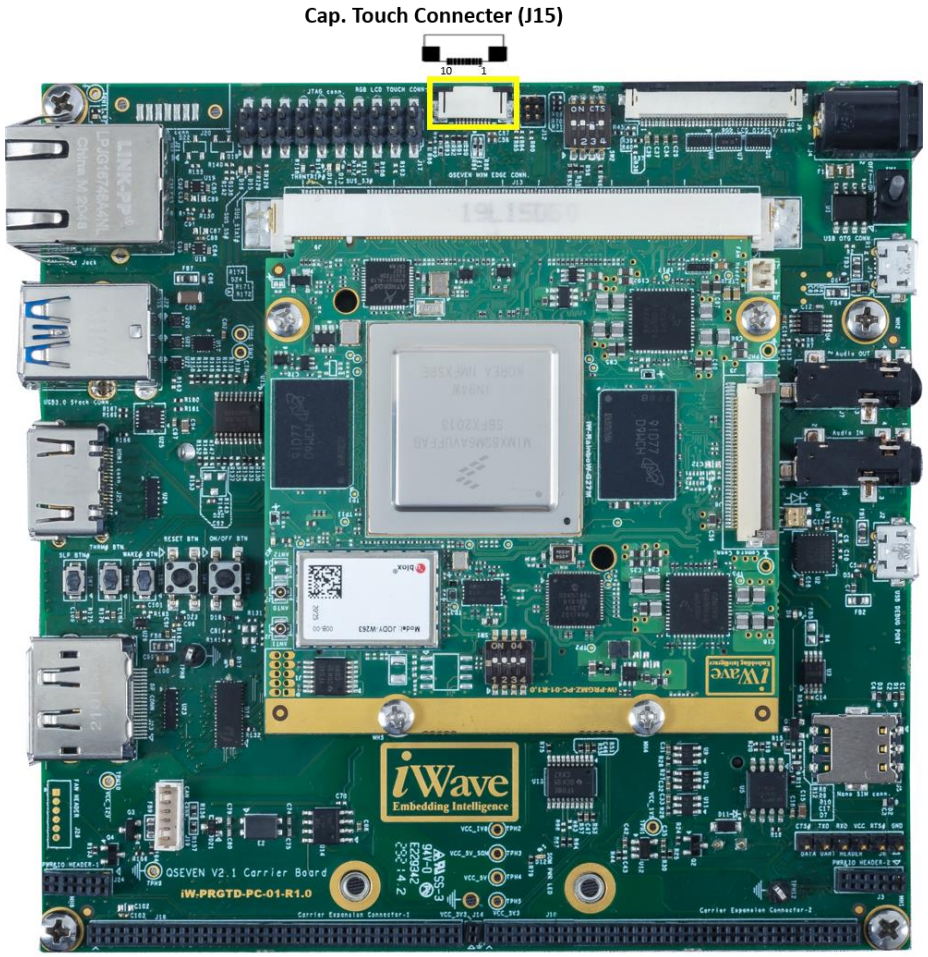


Figure 17: Capacitive touch connector

Table 10: Capacitive touch connector Pinouts

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	VSS1	GND	Power	Ground Signal
2	VDD	VCC_3V3_TFT1	0,3.3V Power	3.3 V Supply voltage.
3	SCL	DMA_I2C2_SCL	O, 3.3V OD	I2C2 Clock Signal
4	NC1	NC	-	-
5	SDA	DMA_I2C2_SDA	IO,3.3V OD	I2C2 Data Signal
6	NC2	NC	-	-
7	RST#	GPIO_RESET(GPIO1_05)	O,3.3V CMOS /10K PU	Touch Controller Reset
8	WAKE#	CAP_WAKE#	O,3.3V CMOS/10K PU	Wake interrupt.
9	INT#	Q7_GPIO_0(GPIO3_12)	I,3.3 V CMOS/10K PU	Touch Controller Interrupt
10	VSS1	GND	Power	Ground

2.7.5 LVDS Port with Resistive Touch

The i.MX 8 QM/QP Qseven carrier board can support 10.1-inch LVDS LCD interface through i.MX 8 QM/QP CPU's LVDS1_CH1 display port. These LVDS signals from Qseven MXM connector is directly connected to 40pin LVDS connector (J30). This LVDS LCD connector (J30) is physically located at the bottom of board as shown below.

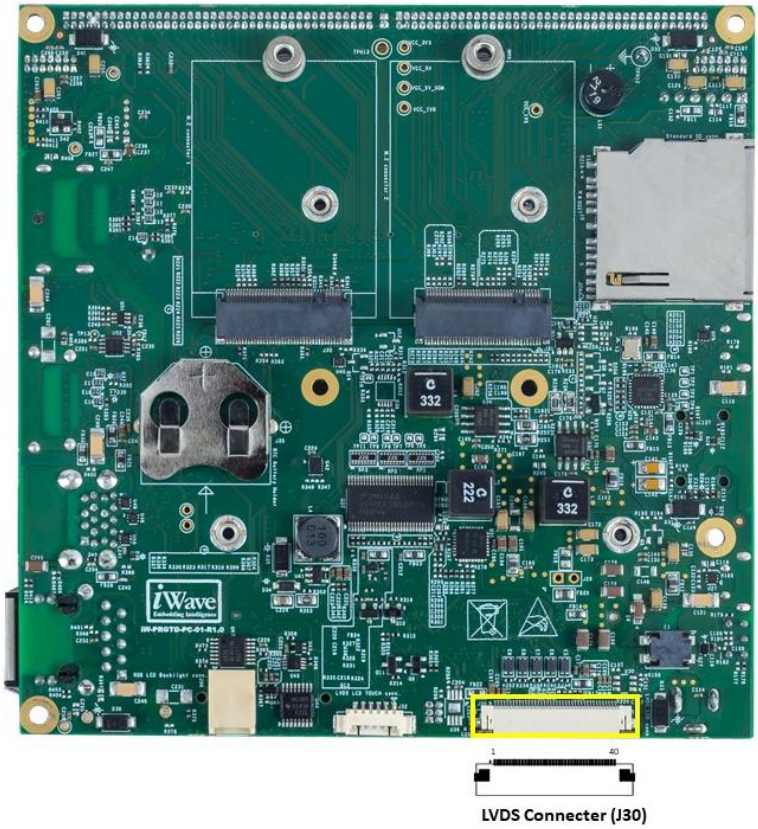


Figure 18: LVDS Display Connector

Table 11: LVDS Connector Pinout

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	VDD1	VCC_3V3_TFT0	Power	3.3V Supply voltage
2	VDD2	VCC_3V3_TFT0	Power	3.3V Supply voltage
3	GND1	GND	Power	Ground
4	GND2	GND	Power	Ground
5	RIN0-	LVDS1_CH1_TX0_N	I, LVDS	LVDS channel differential pair0 negative
6	RIN0+	LVDS1_CH1_TX0_P	I, LVDS	LVDS channel differential pair0 positive
7	GND3	GND	Power	Ground
8	RIN1-	LVDS1_CH1_TX1_N	I, LVDS	LVDS channel differential pair1 negative
9	RIN1+	LVDS1_CH1_TX1_P	I, LVDS	LVDS channel differential pair1 positive
10	GND4	GND	Power	Ground
11	RIN2-	LVDS1_CH1_TX2_N	I, LVDS	LVDS channel differential pair2 negative
12	RIN2+	LVDS1_CH1_TX2_P	I, LVDS	LVDS channel differential pair2 positive
13	GND5	GND	Power	Ground

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
14	CLKIN-	LVDS1_CH1_CLK_N	I, LVDS	LVDS channel differential Clock negative
15	CLKIN+	LVDS1_CH1_CLK_P	I, LVDS	LVDS channel differential Clock positive
16	GND6	GND	Power	Ground
17	RIN3-	LVDS1_CH1_TX3_N	I, LVDS	LVDS channel differential pair3 negative
18	RIN3+	LVDS1_CH1_TX3_P	I, LVDS	LVDS channel differential pair3 positive
19	GND7	GND	Power	Ground
20	GND8	GND	Power	Ground

2.8 Additional Features

2.8.1 SPI Flash

The i.MX 8 QM/QP Qseven development board supports SPI Flash(U5) through i.MX8 CPU's SPI3 interface. This SPI interface signals from MXM connector is connected to SPI Flash "SST25VF016B-50" and operating at 3.3V Level.

2.8.2 RTC Coin Cell Holder

The i.MX 8 QM/QP Qseven carrier board supports Coin Cell Holder to connect "2032" series coin cell. This coin cell voltage is connected to Qseven MXM connector VDD_RTC pin (193th) for RTC back up voltage when VCC main power is off. This Coin Cell Holder (J35) is physically located at the top of the board as shown below.

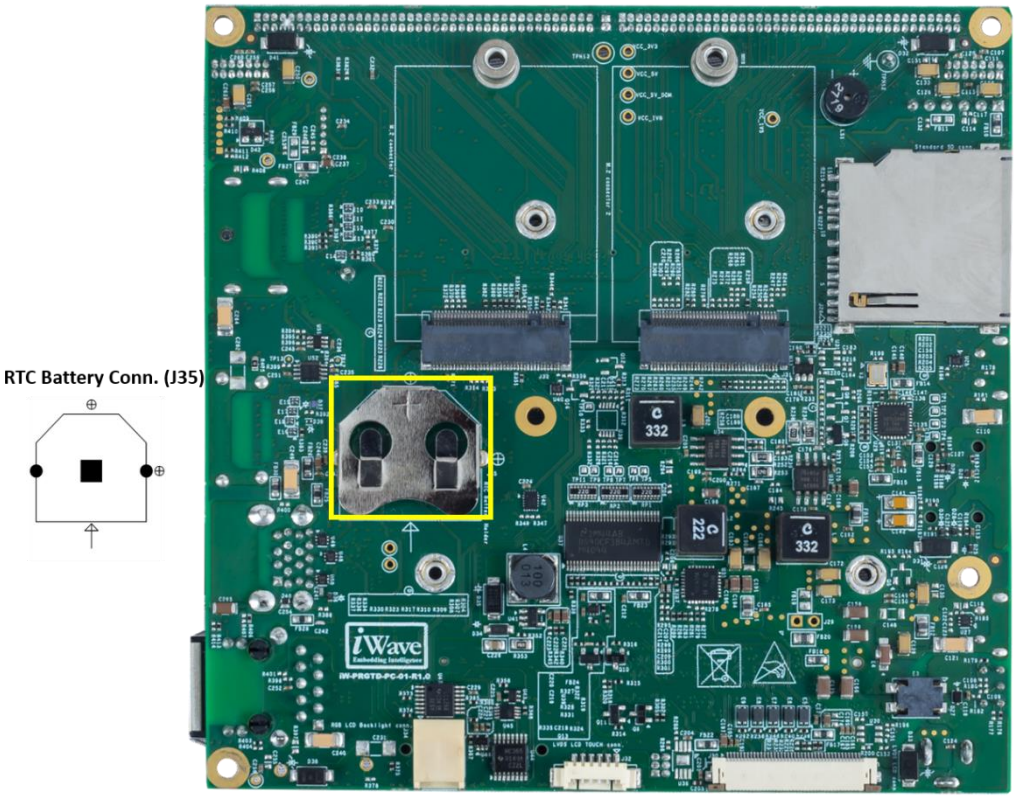


Figure 19: RTC Battery Holder

2.8.3 Fan Header

The i.MX 8 QM/QP Qseven carrier board supports 6pin Fan Header (J26) to connect the Fan if required. The "FAN_PWMOUT" signal of Qseven MXM connector is connected to Fan header to control the speed of the Fan. The i.MX 8M/QP CPU's PWM3 interface is used for Fan speed control PWM. This Fan Header (J26) is physically located at the top of the board as shown below.

Number of Pins : 6

Connector Part number : 53047-0610 from Molex

Mating Connector : 0510210600 from Molex with crimping pins

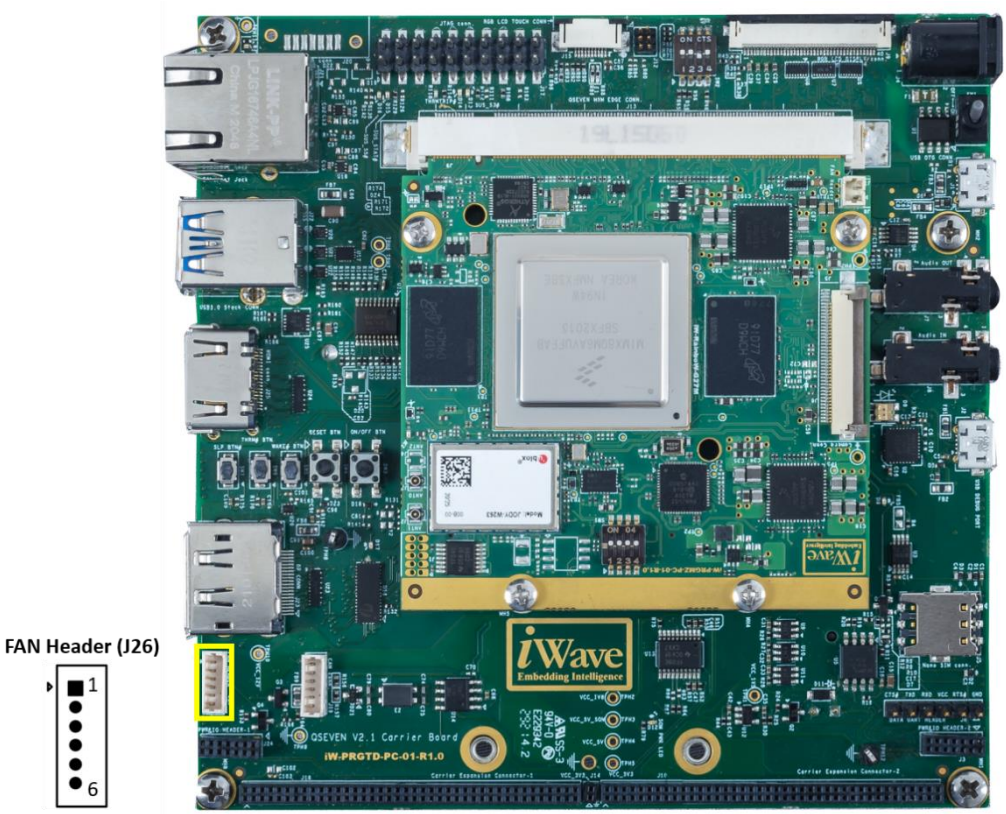


Figure 20: Fan Header

Table 12: Fan Header Pin Out

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	VCC	VCC_12V	O, 12V Power	12V Supply Voltage.
2	PWM	PWM3(GPIO0_16)	O, 3.3 CMOS	Fan Speed control.
3	GND	GND	Power	Ground.
4	TACHO	FAN_TACHOIN	I, 3.3 CMOS	Fan tachometer input
5	SPWR	VCC_FAN	O, Power	Fan Power Control.
6	GND	GND	Power	Ground.

2.8.4 JTAG Header (Optional)

A Standard 20-pin ARM JTAG Header is available in i.MX 8 QM/QP Qseven carrier board for debug purpose. JTAG signals from Qseven MXM connector is connected to JTAG Header (J17) through 3.3V level Buffer. This JTAG Header (J17) is physically located at the top of the board as shown below.

As per Qseven specification version 2.1, Debug UART and JTAG interfaces share the same pins in Qseven Edge connector. Hence either debug UART or JTAG interface can be used at a time. By default, Debug UART (UART4) is supported in the i.MX 8M/QP Qseven SOM and hence JTAG connector on i.MX 8 QM/QP Qseven carrier board cannot be used for debugging.

Number of Pins : 20
Connector Part number : 0015912200 from Molex
Mating Connector : 0015445820 from Molex

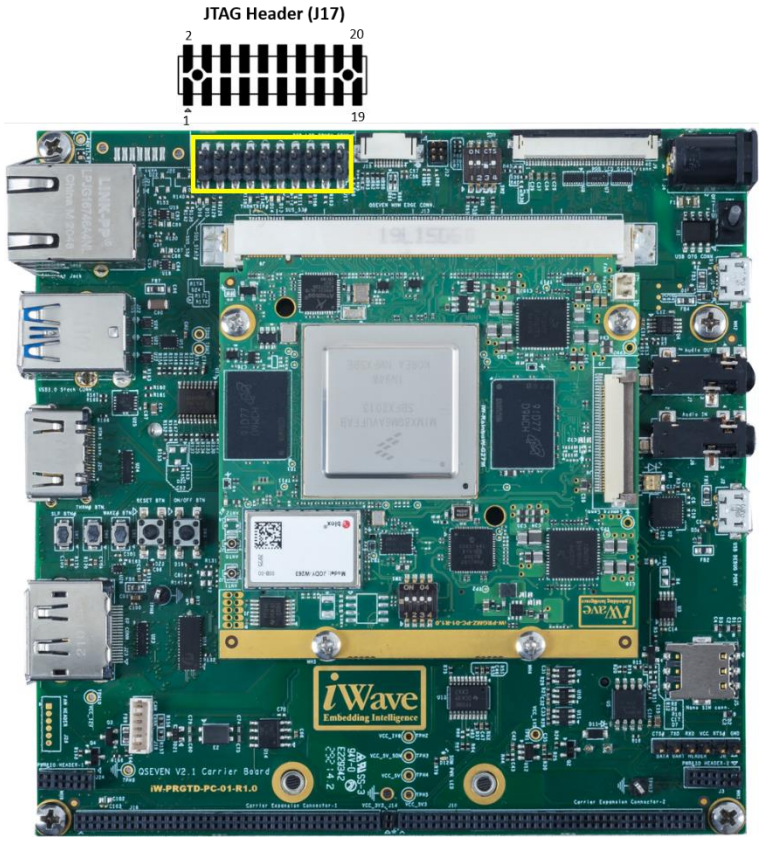


Figure 21: JTAG Header

2.8.5 USB2.0 Header

The i.MX 8 Qseven development board supports a 6-pin USB Header (J32) which is placed at bottom side of the board. This connector can be used as general-purpose touch connector using USB interface.

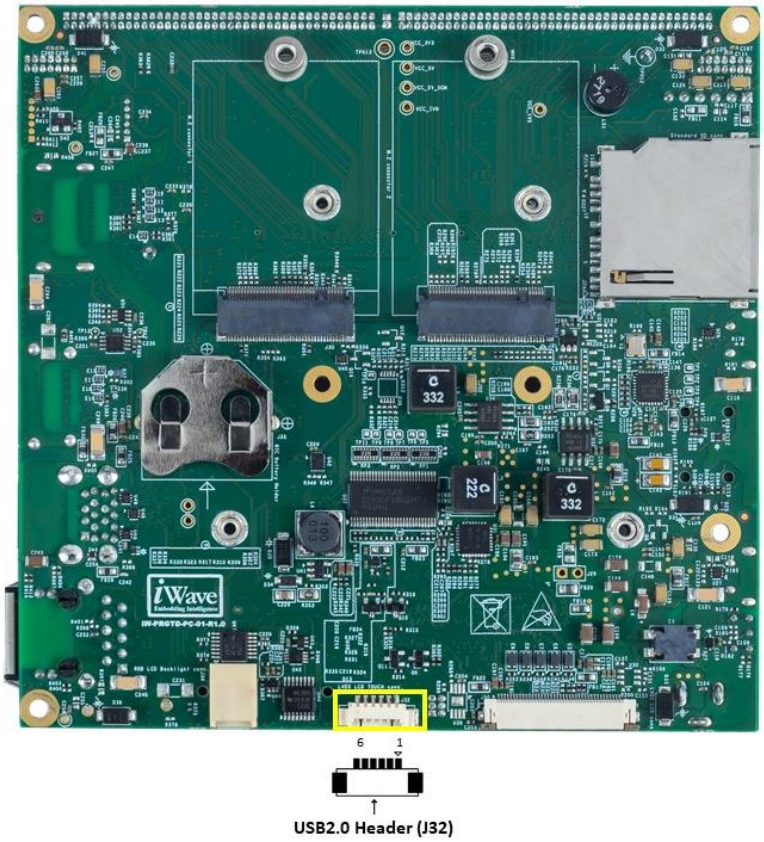


Figure 22: USB2.0 Header

Table 13: USB2.0 Header

Pin No	Signal Name	Signal Type / Termination	Description
1	VBUS_HOST_TP	Power	Supply Voltage 5V
2	USB_HUBOUT3_DM	Power	USB Data Negative
3	USB_HUBOUT3_DP	I, 3.3V CMOS	USB Data Positive
4	NC1	NA	NC
5	GND	Power	Ground
6	NC2	NA	NC

2.9 On Board Switches

2.9.1 Power ON/OFF Switch

The i.MX 8 QM/QP Qseven carrier board has power ON/OFF switch (SW1) to control the Main Power Input On/Off functionality. This power ON/OFF switch is physically located at the top of the board as shown below.

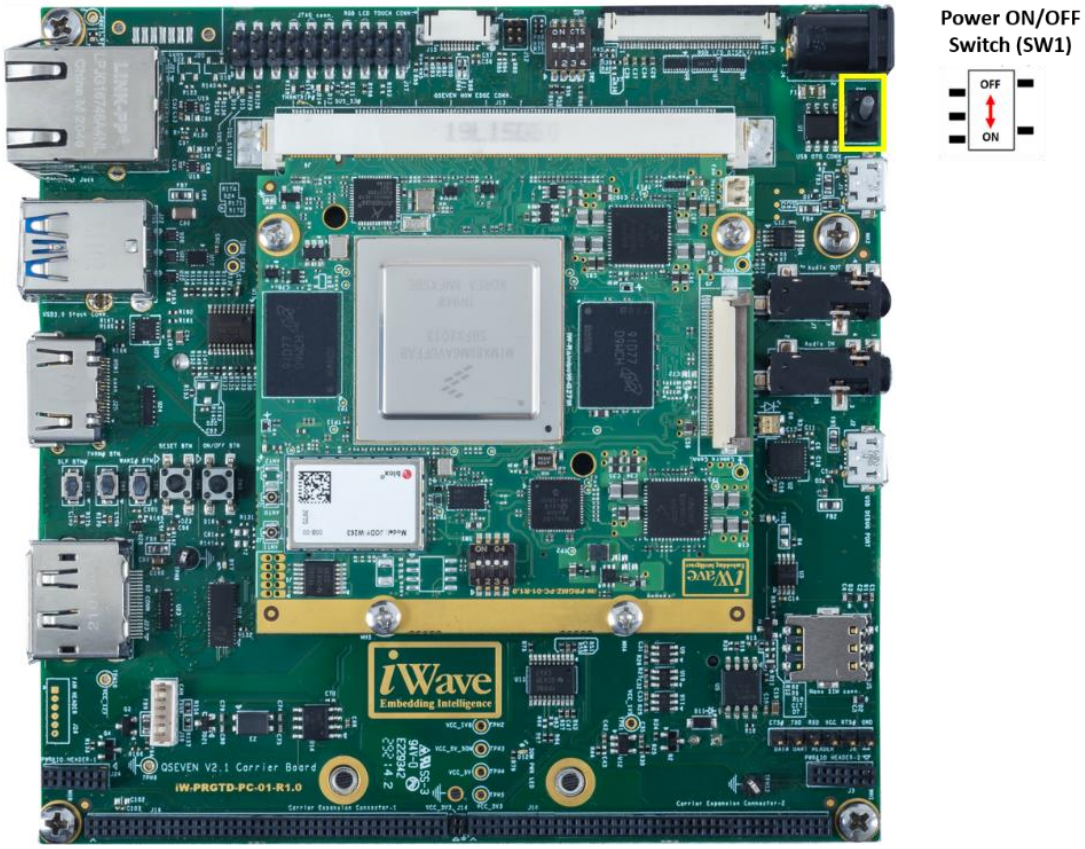


Figure 23: Power ON/OFF Switch

2.9.2 Reset Switch

The i.MX 8 QM/QP Qseven carrier board supports Push button switch (SW4) to reset the i.MX 8M/QP CPU. “RSTBTN” signal of Qseven MXM connector is directly connected from Reset Push button switch. This Reset Push button switch (SW4) is physically located at the top of the board as shown below.

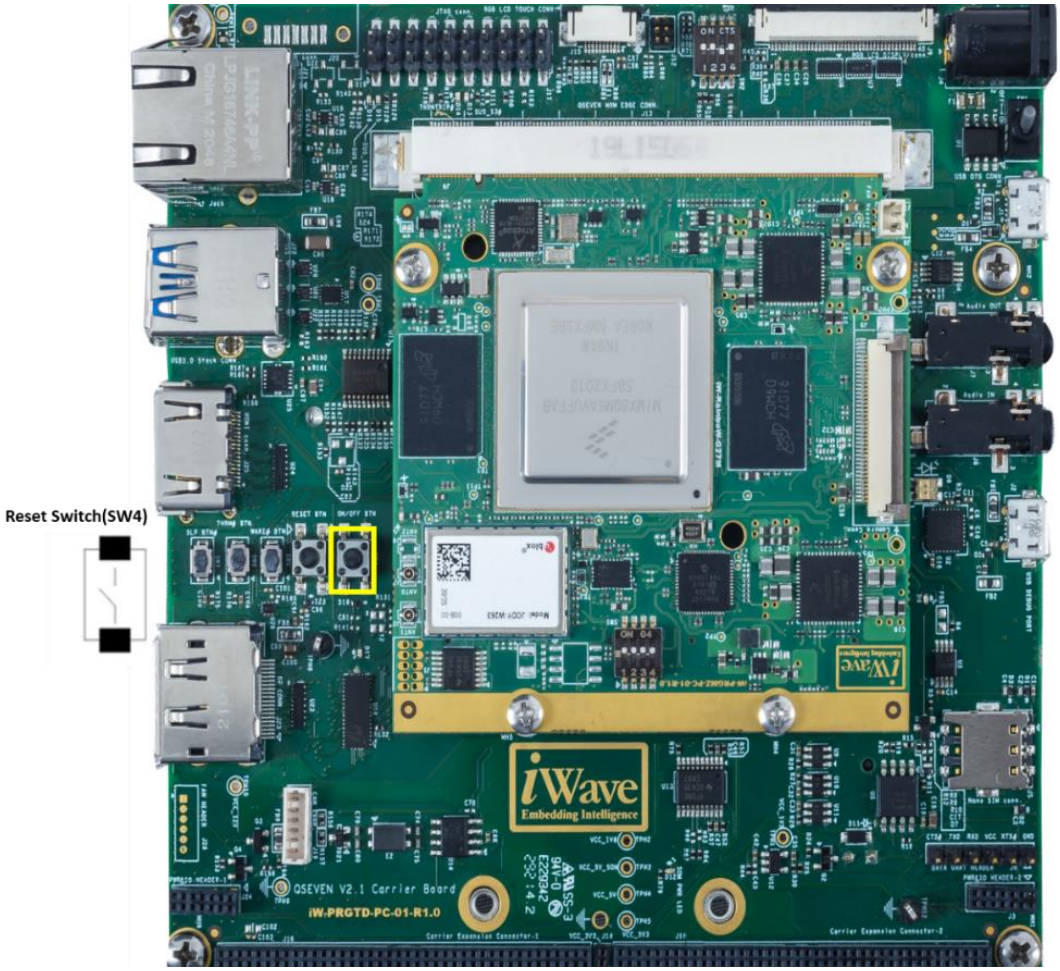


Figure 24: Reset Switch

2.9.3 Board Configuration Switch

The i.MX 8 QM/QP Qseven carrier board has one 8bit Board configuration switch (SW2) to configure board specific feature setting. Each bit of this switch is used to select the different features or modes. This Board configuration switch is physically located at the top of the board as shown below.

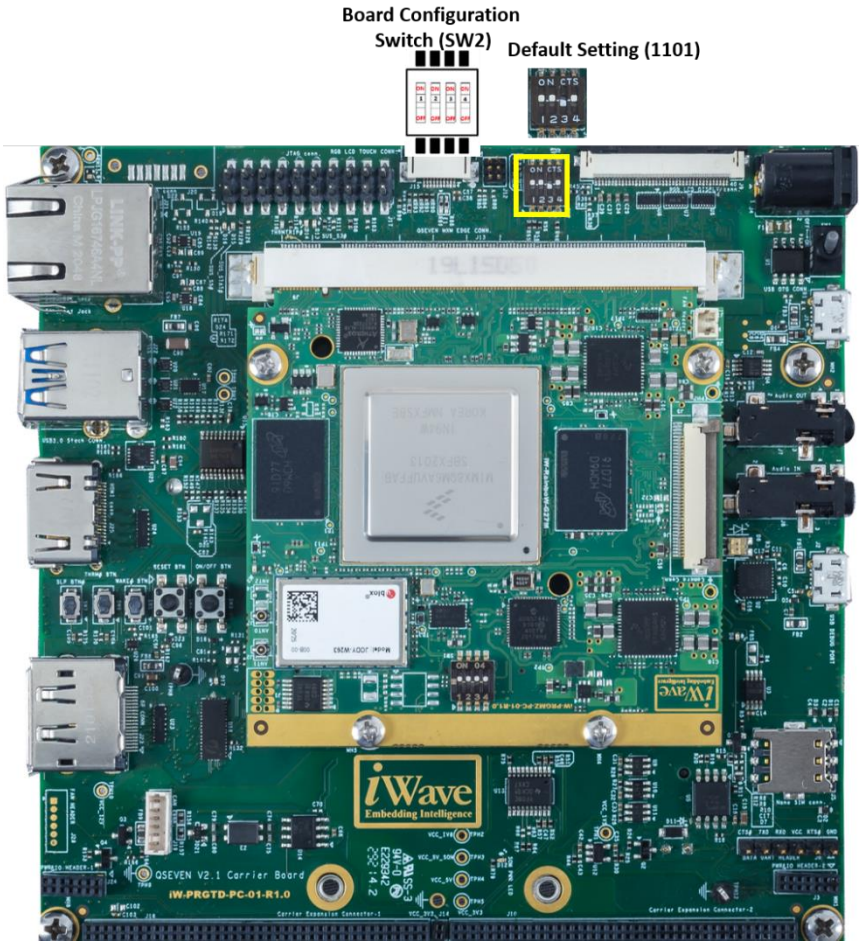


Figure 25: Board Configuration Switch

The functionality of Board configuration switch (SW2) in i.MX 8M/QP Qseven carrier board is explained in the following table. All the bits of Board configuration switch are not used in i.MX 8 QM/QP Qseven carrier board and so only the required bits are explained with default setting highlighted.

Table 14: Board Configuration Switch

SW2 Bits	SW2 Bit Name	Description	
		ON	OFF
1	M.2/LCS_SEL	M.2	LCD touch
2	USB_SEL	USB 2.0	USB 3.0
3	GPU_SEL	HDMI	DP
4	MFG4_JTAG_TRST#	UART	JTAG
Configuration Connecter			
5	LID_BTN# (GPII_0(GPIO3_03)	LID Open	LID Close
6	BIOS_DSIABLE#	BIOS enable *(ON Som Its Not Connected)*	BIOS Disable *(ON Som Its Not Connected)*
7	BATLOW# (GPII_2(GPIO0_05)	Battery-OK	Battery-LOW

2.1 SOM Expansion Connectors

The i.MX 8 QM/QP Qseven carrier board has two 80pin Expansion Connectors for mating with i.MX 8 QM/QP Qseven SOM. This SOM Expansion connector 1 & 2 (J16 & J11) pins are one to one directly connected to Carrier board Expansion connector 1 & 2 (J18 & J10) pins in i.MX 8 QM/QP Qseven carrier board.

These Expansion connectors J16 & J11 are physically located at the top of the board as shown below.

Connectors Part number : DF17(2.0)-80DP-0.5V(57) from Hirose

Mating Connector : DF17(3.0)-80DS-0.5V(57) from Hirose

Note: For SOM expansion connector pinout, refer the i.MX 8 QM/QP Qseven SOM Hardware User Guide.

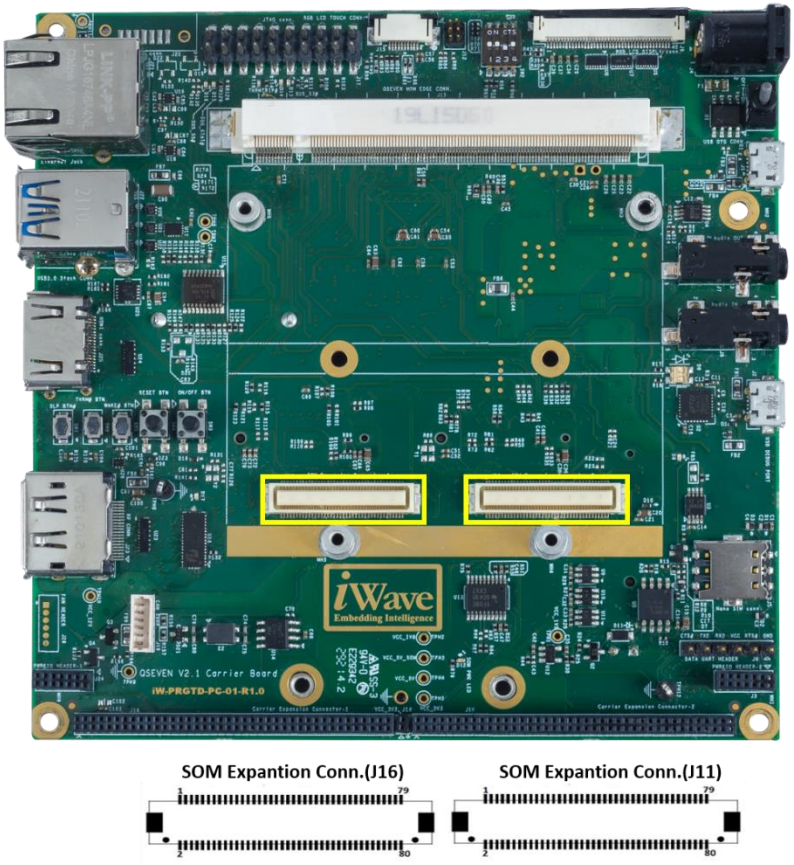
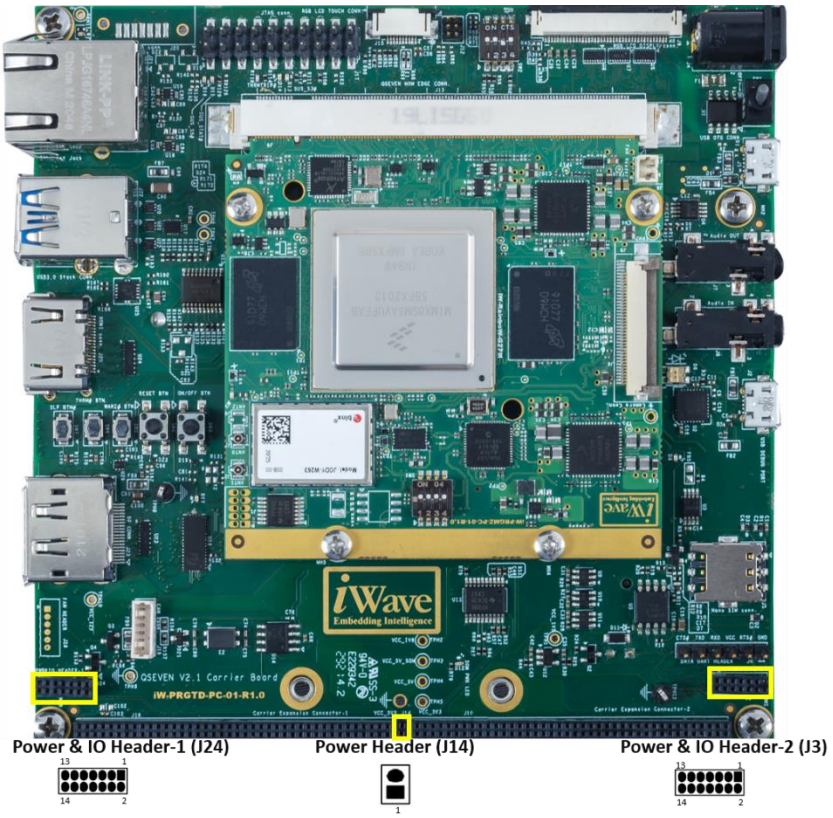


Figure 26: SOM Expansion Connectors

2.2 Power and IO Headers

The i.MX 8 QM/QP Qseven carrier board supports two Power and IO Headers (J3 and J24) which is 14 pins each. Also the board 2pin Power header(J14) which is optional.



Power Header (J4)			
Pin No	**Signal Name**	**Signal Type /Termination**	**Description**
1	GND	O,Power	This pin is connected with Ground
2	VCC_3V3	O,Power 3.3V	This pin is connected with Power
Power & IO Header-1 (J3)			
1	LVDS1_I2C0_SDA	O,3.3V OD	I2C0 Data line
2	DMA_I2C1_SCL	I, 3.3V OD /2.2K PU	I2C1 Clock
3	LVDS1_I2C0_SCL	I, 3.3V OD	I2C0 Clock
4	DMA_I2C1_SDA	I, 3.3V OD /2.2K PU	I2C1 Data
5	VCC_12V	O,12V Power	12V Supply Voltage
6	VCC_5V	O,5V Power	5V Supply Voltage
7	VCC_12V	O,12V Power	12V Supply Voltage
8	VCC_5V	O,5V Power	5V Supply Voltage
9	LVDS_BLC_CLK	NA	On SOM In this pin is Not Connected
10	VCC_3V3	O,3.3V Power	3.3 V Supply Voltage
11	LVDS_BLC_DAT	NA	On SOM In this pin is Not Connected
12	VCC_3V3	Power, O 3.3V Power	3.3V Supply Voltage
13	GND	Power	Ground
14	GND	Power	Ground

Power & IO Header-2 (J24)			
1	SPI_MISO	O, 3.3V CMOS	SPI Master In Slave Out. Connected With SPI Flash
2	SPI_CS1#	I, 3.3V CMOS	SPI Chip Select2. Connected With SPI Flash.
3	SPI_MOSI	I, 3.3V CMOS	SPI Master Out Slave In. Connected With SPI Flash
4	GND	Power	Ground
5	VCC_3V3	3.3V Power, O	3.3V Supply Voltage
6	SPI_SCK	I, 3.3V CMOS	SPI Clock. This Pin is connected to SPI Flash.
7	VCC_3V3	3.3V Power, O	3.3V Supply Voltage
`8	VCC_1V8	1.8V Power, O	1.8V Supply Voltage
9	WDOUT	NA	NC
10	RSVD1	I, 3.3V CMOS	This Pin is connected with GPIO(GPIO_SD1_LED(GPIO3_06))
11	WDTRIG#	I, 3.3V CMOS	This pin is connected with PMIC Control
12	VCC_1V5	1.5V Power, O	1.5V Supply Voltage
13	GND	Power	Ground
14	GND	Power	Ground

2.3 Carrier Board Expansion Connectors

The i.MX 8M/QP Qseven carrier board has two 80pin Expansion Connectors for expansion purpose. These two connector 1 & 2 (J18 & J10) pins are one to one directly connected from SOM Expansion connector 1 & 2 (J16 & J11) pins in i.MX 8M/QP Qseven carrier board.

These Expansion connectors are physically located at the top of the board as shown below.

Connectors Part number: 20021311-00080T4LF Amphenol ICC

Mating Connector: 20021111-00080T4LF from Amphenol ICC

Important Note: Since carrier board Expansion connector 1 & 2 pins are one to one directly connected from i.MX 8 QM/QP Qseven SOM Expansion connector 1 & 2 pins, these connectors pinout information are not included in this document. Refer i.MX 8 QM/QP Qseven SOM hardware user guide for Expansion connector 1 & 2 pinout details.

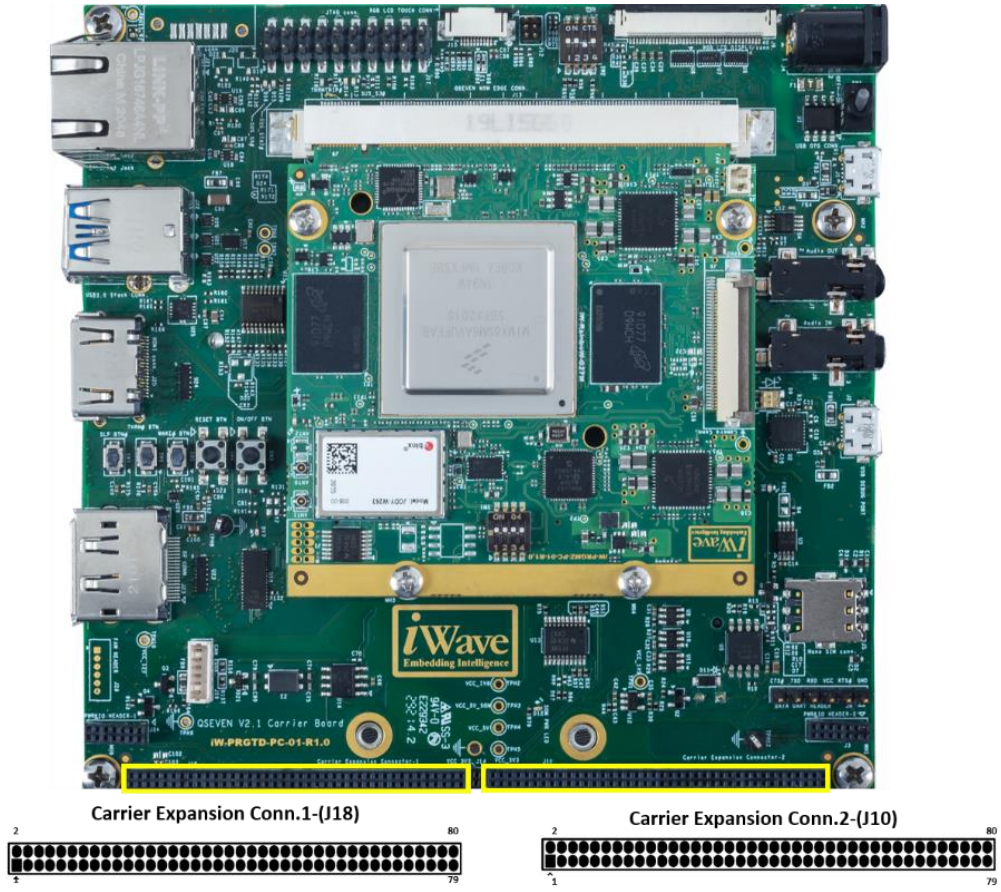


Figure 27: Carrier Board Expansion Connectors

Table 15:Carrier Expansion Connector1 Pin Out

Pin No	Signal Name	Signal Name	Signal Type / Termination	Description
1	MIPI_DSI0_CLK_P	MIPI_DSI0_CLK_P/ BL27	I, DIFF	MIPI_DSI0 Differential Clock Positive
2	MIPI_DSI1_CLK_P	MIPI_DSI1_CLK_P/ BG31	I, DIFF	MIPI_DSI1 Differential Clock Positive
3	MIPI_DSI0_CLK_N	MIPI_DSI0_CLK_N/ BN27	I, DIFF	MIPI_DSI0 Differential Clock Negative
4	MIPI_DSI1_CLK_N	MIPI_DSI1_CLK_N/ BH39	I, DIFF	MIPI_DSI1 Differential Clock Negative
5	GND	NA	Power	Ground
6	GND	NA	Power	Ground
7	MIPI_DSI0_DATA0_P	MIPI_DSI0_DATA0 _P/BK28	I, DIFF	MIPI_DSI1 Differential Data Lane 0 Positive
8	MIPI_DSI1_DATA0_P	MIPI_DSI1_DATA0 _P/BG33	I, DIFF	MIPI_DSI0 Differential Data Lane 0 Positive
9	MIPI_DSI0_DATA0_N	MIPI_DSI0_DATA0 _N/BM28	I, DIFF	MIPI_DSI0 Differential Data Lane 0 Negative

Pin No	Signal Name	Signal Name	Signal Type / Termination	Description
10	MIPI_DSI1_DATA0_N	MIPI_DSI1_DATA0_N/BH32	I, DIFF	MIPI_DSI1 Differential Data Lane 0 Negative
11	GND	NA	Power	Ground
12	GND	NA	Power	Ground
13	MIPI_DSI0_DATA1_P	MIPI_DSI0_DATA1_P/BK26	I,DIFF	MIPI_DSI1 Differential Data Lane 1 Positive
14	MIPI_DSI1_DATA1_P	MIPI_DSI1_DATA1_P/BG29	I,DIFF	MIPI_DSI1 Differential Data Lane 1 Positive
15	MIPI_DSI0_DATA1_N	MIPI_DSI0_DATA1_N/BM26	I,DIFF	MIPI_DSI0 Differential Data Lane 1 Negative
16	MIPI_DSI1_DATA1_N	MIPI_DSI1_DATA1_N/BH28	I,DIFF	MIPI_DSI1 Differential Data Lane 1 Negative
17	GND	NA	Power	Ground
18	GND	NA	Power	Ground
19	MIPI_DSI0_DATA2_P	MIPI_DSI0_DATA2_P/BL29	I,DIFF	MIPI_DSI0 Differential Data Lane 2 Positive
20	MIPI_DSI1_DATA2_P	MIPI_DSI1_DATA2_P/BG35	I,DIFF	MIPI_DSI1 Differential Data Lane 2 Positive
21	MIPI_DSI0_DATA2_N	MIPI_DSI0_DATA2_N/BN29	I,DIFF	MIPI_DSI0 Differential Data Lane 2 Negative
22	MIPI_DSI1_DATA2_N	MIPI_DSI1_DATA2_N/BH34	I,DIFF	MIPI_DSI1 Differential Data Lane 2 Negative
23	GND	NA	Power	Ground
24	GND	NA	Power	Ground
25	MIPI_DSI0_DATA3_P	MIPI_DSI0_DATA3_P/BL25	I,DIFF	MIPI_DSI0 Differential Data Lane 3 Positive
26	MIPI_DSI1_DATA3_P	MIPI_DSI1_DATA3_P/BG27	I,DIFF	MIPI_DSI1 Differential Data Lane 2 Positive
27	MIPI_DSI0_DATA3_N	MIPI_DSI0_DATA3_N/BN25	I,DIFF	MIPI_DSI0 Differential Data Lane 3 Negative
28	MIPI_DSI1_DATA3_N	MIPI_DSI1_DATA3_N/BH26	I,DIFF	MIPI_DSI1 Differential Data Lane 2 Negative
29	GND	NA	Power	Ground
30	GND	NA	Power	Ground
31	HDMI_RX0_CLK_N	HDMI_RX0_CLK_N/BL11	I,DIFF	HDMI_RX0 Clock Negative
32	MIPI_DSI0_I2C_SDA	MIPI_DSI0_I2C_SDA/BE31	I,DIFF	MIPI_DSI I2C0 Data
33	HDMI_RX0_CLK_P	HDMI_RX0_CLK_P/BM12	I,DIFF	HDMI_RX0 Clock Negative
34	MIPI_DSI0_I2C_SCL	MIPI_DSI0_I2C_SCL/BE29	I,DIFF	MIPI_DSI I2C0 Clock

Pin No	Signal Name	Signal Name	Signal Type / Termination	Description
35	GND	NA	Power	Ground
36	FLEXCAN1_RX	FLEXCAN1_RX/E5	I,1.8V CMOS	Can1 Receiver
37	HDMI_RX0_ARC_N	HDMI_RX0_ARC_N /BL13	I,TMDS	HDMI RX0 differential audio Return channel negative
38	FLEXCAN1_TX	FLEXCAN1_TX/G7	O,1.8V CMOS	CAN1 Transmitter
39	HDMI_RX0_ARC_P	HDMI_RX0_ARC_P /BM14	I,TMDS	HDMI RX0 differential audio Return channel Positive
40	FLEXCAN2_RX	FLEXCAN2_RX/C3	I,1.8V CMOS	CAN1 Receiver
41	GND	NA	Power	Ground
42	FLEXCAN2_TX	FLEXCAN2_TX/E7	O,1.8V CMOS	Can1 Transmitter
43	HDMI_RX0_DATA0_N	HDMI_RX0_DATA0 _N/BL15	I,TDMS	HDMI_RX0 Differential Data Lane 0 Negative
44	GND	NA	Power	Ground
45	HDMI_RX0_DATA0_P	HDMI_RX0_DATA0 _P/BM16	I,TDMS	HDMI_RX0 Differential Data Lane 0 Positive
46	HDMI_RX0_CEC	HDMI_RX0_CEC/BJ 19	IO,3.3V CMOS	HDMI Consumer Electronics Control
47	GND	NA	Power	Ground
48	HDMI_RX_HPD	HDMI_RX_HPD/BF 14	O,5V CMOS	HDMI RX Hot plug detect
49	HDMI_RX0_DATA1_N	HDMI_RX0_DATA1 _N/BL17	I,TDMS	HDMI_RX0 Differential Data Lane 1 Negative
50	HDMI_RX0_DDC_SDA	HDMI_RX0_DDC_S DA/BE13	IO,5V CMOS	HDMI RX0 DDC Data
51	HDMI_RX0_DATA1_P	HDMI_RX0_DATA1 _P	I,TDMS	HDMI_RX0 Differential Data Lane 1 Positive
52	HDMI_RX0_DDC_SCL	HDMI_RX0_DDC_S CL/BH10	IO,5V CMOS	HDMI RX0 DDC Clock
53	GND	GND	Power	Ground
54	VHDMI_RX_5V	VHDMI_RX_5V/BN 11	Power	HDMI RX0 Reference Voltage
55	HDMI_RX0_DATA2_N	HDMI_RX0_DATA2 _N/BL19	I,TDMS	HDMI_RX0 Differential Data Lane 2 Negative
56	GND	NA	Power	Ground
57	HDMI_RX0_DATA2_P	HDMI_RX0_DATA2 _P/BM20	I,TDMS	HDMI_RX0 Differential Data Lane 2 Positive
58	ADC_IN4(GPIO3_22)	ADC_IN4(GPIO3_2 2)/AN9	I, 1.8V CMOS	ADC Input 4 *(Note: Optionally UART3_RX)*
59	GND	NA	Power	Ground

Pin No	Signal Name	Signal Name	Signal Type / Termination	Description
60	ADC_IN5(GPIO3_23)	ADC_IN5(GPIO3_23)/AR7	I, 1.8V CMOS	ADC Input 5 *(Note: Optionally UART3_TX)*
61	ENET1_RGMII_TXC	ENET1_RGMII_TXC/D46	O, 3.3V CMOS/ 33E Series	ENET1 transmit clock.
62	VDD_ENET1	VDD_ENET1/T38	Power	ENET1 reference voltage
63	ENET1_RGMII_TX_CTL	ENET1_RGMII_TX_CTL/B48	O, 3.3V CMOS/ 33E Series	ENET1 data Control line.
64	MIPI_DSI1_I2C_SCL(GPIO1_20)	MIPI_DSI1_I2C_SCL(GPIO1_20)/BE27	O, 3.3V OD/ 2.2K PU	MIPI_DSI1 Serial clock.
65	ENET1_RGMII_TXD0	ENET1_RGMII_TXD0/A49	O, 3.3V CMOS/ 33E Series	ENET1 transmit data0.
66	MIPI_DSI1_I2C_SDA(GPIO1_21)	MIPI_DSI1_I2C_SDA(GPIO1_21)/BG25	IO, 3.3V OD/ 2.2K PU	MIPI_DSI1 Serial Data.
67	ENET1_RGMII_TXD1	ENET1_RGMII_TXD1/C47	O, 3.3V CMOS/ 33E Series	ENET1 transmit data1.
68	GND	NA	Power	Ground
69	ENET1_RGMII_TXD2	ENET1_RGMII_TXD2/G47	O, 3.3V CMOS/ 33E Series	ENET1 transmit data2.
70	ENET1_RGMII_RXC	ENET1_RGMII_RXC/B50	I, 3.3V CMOS	ENET1 receive clock.
71	ENET1_RGMII_TXD3	ENET1_RGMII_TXD3/D48	O, 3.3V CMOS/ 33E Series	ENET1 transmit data3.
72	ENET1_RGMII_RX_CTL	ENET1_RGMII_RX_CTL/E49	I, 3.3V CMOS	ENET1 receive Control line.
73	GND	NA	Power	Ground
74	ENET1_RGMII_RXD0	ENET1_RGMII_RXD0/E51	I, 3.3V CMOS	ENET1 receive data0.
75	ENET1_REFCLK_125M_25M	ENET1_REFCLK_125M_25M/A11	I, 3.3V CMOS	Synchronous Ethernet reference clock.
76	ENET1_RGMII_RXD1	ENET1_RGMII_RXD1/C51	I, 3.3V CMOS	ENET1 receive data1.
77	ENET1_MDIO	ENET1_MDIO/C13	IO,3.3V CMOS	Management data.
78	ENET1_RGMII_RXD2	ENET1_RGMII_RXD2/D52	I, 3.3V CMOS	ENET1 receive data2.
79	ENET1_MDC	ENET1_MDC/A13	O,3.3V	Management data clock.
80	ENET1_RGMII_RXD3	ENET1_RGMII_RXD3	I, 3.3V CMOS	ENET1 receive data3.

Table 16: Carrier Expansion Connector 1 Pin Out

Pin No	Signal Name	Signal Name	Signal Type / Termination	Description
1	LVDS0_CH1_CLK_N	LVDS0_CH1_CLK_N / BG45	O, LVDS	LVDS0 Channel1 Clock negative.
2	LVDS0_CH0_CLK_P	LVDS0_CH0_CLK_P	LVDS0_CH0 _CLK_P/ BN41	O, LVDS
3	LVDS0_CH1_CLK_P	LVDS0_CH1_CLK_P / BH46	O, LVDS	LVDS0 Channel1 Clock positive.
4	LVDS0_CH0_CLK_N	LVDS0_CH0_CLK_N / BL41	O, LVDS	LVDS0 Channel0 Clock negative.
5	GND	NA	Power	Ground
6	GND	NA	Power	Ground
7	LVDS0_CH1_TX0_P	LVDS0_CH1_TX0_P / BH44	O, LVDS	LVDS0 Channel1 Transmit Lane 0 positive.
8	LVDS0_CH0_TX0_P	LVDS0_CH0_TX0_P / BM42	O, LVDS	LVDS0 Channel0 Transmit Lane 0 positive.
9	LVDS0_CH1_TX0_N	LVDS0_CH1_TX0_N	LVDS0_CH1 _TX0_N/ BG43	O, LVDS
10	LVDS0_CH0_TX0_N	LVDS0_CH0_TX0_N / BK42	O, LVDS	LVDS0 Channel0 Transmit Lane 0 negative.
11	GND	NA	Power	Ground
12	GND	NA	Power	Ground
13	LVDS0_CH1_TX1_N	LVDS0_CH1_TX1_N / BG41	O, LVDS	LVDS0 Channel1 Transmit Lane 1 negative.
14	LVDS0_CH0_TX1_P	LVDS0_CH0_TX1_P / BN43	O, LVDS	LVDS0 Channel0 Transmit Lane 1 positive.
15	LVDS0_CH1_TX1_P	LVDS1_CH1_TX1_P / BH42	O, LVDS	LVDS0 Channel1 Transmit Lane 1 positive.
16	LVDS0_CH0_TX1_N	LVDS0_CH0_TX1_N / BL43	O, LVDS	LVDS0 Channel0 Transmit Lane 1 negative.
17	GND	NA	Power	Ground
18	GND	NA	Power	Ground
19	LVDS0_CH1_TX2_N	LVDS0_CH1_TX2_N / BG39	O, LVDS	LVDS0 Channel1 Transmit Lane 2 negative.
20	LVDS0_CH0_TX2_P	LVDS0_CH0_TX2_P / BM44	O, LVDS	LVDS0 Channel0 Transmit Lane 2 positive.
21	LVDS0_CH1_TX2_P	LVDS0_CH1_TX2_P / BH40	O, LVDS	LVDS0 Channel1 Transmit Lane 2 positive.

Pin No	Signal Name	Signal Name	Signal Type / Termination	Description
22	LVDS0_CH0_TX2_N	LVDS0_CH0_TX2_N / BK44	O, LVDS	LVDS0 Channel0 Transmit Lane 2 negative.
23	GND	NA	Power	Ground
24	GND	NA	Power	Ground
25	LVDS0_CH1_TX3_N	LVDS0_CH1_TX3_N / BG37	O, LVDS	LVDS0 Channel1 Transmit Lane 3 negative.
26	LVDS0_CH0_TX3_P	LVDS0_CH0_TX3_P / BN45	O, LVDS	LVDS0 Channel0 Transmit Lane 3 positive.
27	LVDS0_CH1_TX3_P	LVDS0_CH1_TX3_P / BH38	O, LVDS	LVDS0 Channel1 Transmit Lane 3 positive.
28	LVDS0_CH0_TX3_N	LVDS0_CH0_TX3_N / BL45	O, LVDS	LVDS0 Channel0 Transmit Lane 3 negative.
29	GND	NA	Power	Ground
30	GND	NA	Power	Ground
31	LVDS0_I2C0_SDA	LVDS0_I2C0_SDA/BD36	IO, 3.3V CMOS/ 2.2K PU	LVDS0 Serial Data.
32	SNVS_TAMPER_OUT0	SNVS_TAMPER_OUT0/BD46	O,1.8V CMOS	Tamper out pin 0
33	LVDS0_I2C0_SCL	LVDS0_I2C0_SCL/BD38	O, 3.3V CMOS/ 2.2K PU	LVDS0 Serial Clock.
34	SNVS_TAMPER_IN0	SNVS_TAMPER_IN0 / BE41	I,1.8V CMOS	Tamper In pin 0
35	SPDIF_RX	SPDIF_RX/BC7	I,3.3V CMOS	Sony/Philips Digital Interface Receive.
36	SNVS_TAMPER_IN1	SNVS_TAMPER_IN1 /BE43	I,1.8V CMOS	Tamper In pin 1
37	SPDIF_ETX_CLK	SPDIF_ETX_CLK/ BD6	O,3.3V CMOS	Sony/Philips Digital Interface Clock. *Note: Optionally connected to USB_HUB4_OC*
38	SNVS_TAMPER_OUT1	SNVS_TAMPER_OUT1/BD42	O,1.8V CMOS	Temper out pin 1
39	SPDIF_TX	SPDIF_TX/BC9	O,3.3V CMOS	Sony/Philips Digital Interface Transmit. *Note: Optionally connected to VDD_SNVS*
40	GND	NA	Power	Ground
41	MLB_DATA	MLB_DATA/ E3	IO,1.8V CMOS	Media Local Bus Data.
42	MLB_DATA_P	MLB_DATA_P/ F34	IO, MLB	Media Local Bus DATA positive.
43	MLB_CLK	MLB_CLK/ D2	O,1.8V CMOS	Media Local Bus Clock.

Pin No	Signal Name	Signal Name	Signal Type / Termination	Description
44	MLB_DATA_N	MLB_DATA_N/ E35	IO, MLB	Media Local Bus DATA negative.
45	MLB_DATA	MLB_SIG/E1	O,1.8V CMOS	Media Local Bus Signal.
46	GND	NA	Power	Ground
47	MLB_CLK	ESAI1_SCKR/ BD12	I,3.3V CMOS	ESAI1 Clock Input.
48	MLB_CLK_P	MLB_CLK_P/ D32	O, MLB	Media Local Bus Clock positive.
49	MLB_SIG	ESAI1_FSR/ BE11	I,3.3V CMOS	ESAI1 Frame Sync Input.
50	MLB_CLK_N	MLB_CLK_N/ E33	O, MLB	Media Local Bus Clock negative.
51	ESAI1_SCKR	ESAI1_TX0/ BF10	O,3.3V CMOS	ESAI1 Transmit 0.
52	GND	NA	Power	Ground
53	ESAI1_FSR	ESAI1_TX2_RX3/ AU11	IO,3.3V CMOS	ESAI1 Transmit 2 or Receive 3.
54	MLB_SIG_P	MLB_SIG_P/ D30	O, MLB	Media Local Bus Signal positive.
55	ESAI1_TX0	ESAI1_TX3_RX2/ AV10	IO,3.3V CMOS	ESAI1 Transmit 3 or Receive 2.
56	MLB_SIG_N	MLB_SIG_N/ E31	O, MLB	Media Local Bus Signal negative.
57	ESAI1_TX2_RX3	ESAI1_TX4_RX1/ AY12	IO,3.3V CMOS	ESAI1 Transmit 4 or Receive 1.
58	GND	NA	Power	Ground
59	ESAI1_TX3_RX2	ESAI1_TX5_RX0/ AT10	IO,3.3V CMOS	ESAI1 Transmit 5 or Receive 0.
60	GND	NA	Power	Ground
61	GND	NA	Power	Ground
62	SPI2_SCLK	SPI2_SCK/ AW5	O, 1.8V CMOS/ 33E Series	SPI2 Clock
63	QSPI1A_SCLK	QSPI1A_SCLK / F10	O, 1.8V CMOS/ 33E Series	QSPI Clock Output.
64	SPI2_CS0	SPI2_CS0/ AW1	O,3.3V CMOS	SPI2 Chip Select 0.
65	QSPI1A_SS0	QSPI1A_SS0_B/ J11	O,1.8V CMOS	QSPI Chip select.

Pin No	Signal Name	Signal Name	Signal Type / Termination	Description
66	SPI2_MISO	SPI2_SDI/ AY4	I,3.3V CMOS	SPI2 Master In Slave Out.
67	QSPI1A_DATA0	QSPI1A_DATA0/ D12	IO,1.8V CMOS	QSPI Data 0.
68	SPI2_MOSI	SPI2_SDO/ BA1	O,3.3V CMOS	SPI2 Master Out Slave In
69	QSPI1A_DATA1	QSPI1A_DATA1/ D14	IO,1.8V CMOS	QSPI Data 1.
70	GND	NA	Power	Ground
71	QSPI1A_DATA2	QSPI1A_DATA2/ E13	IO,1.8V CMOS	QSPI Data 2.
72	USB3_HUB4_RXP	NA	I, USB SS	USB3.0 Hub Receive channel 4 Plus.
73	QSPI1A_DATA3	QSPI1A_DATA3/ E11	IO,1.8V CMOS	QSPI Data 3.
74	USB3_HUB4_RXM	NA	I, USB SS	USB3.0 Hub Receive channel 4 Minus.
75	GND	NA	Power	Ground
76	GND	NA	Power	Ground
77	USB_HUB4OUT_DP	NA	I, USB HS	USB2.0 Hub Receive channel 1 Plus.
78	USB3_HUB4_TXP	NA	O, USB SS	USB3.0 Hub Transmit channel 4 Plus.
79	USB_HUB4OUT_DM	NA	I, USB HS	USB2.0 Hub Receive channel 1 Minus.
80	USB3_HUB4_TXM	NA	O, USB SS	USB3.0 Hub Transmit channel 4 Minus.

3. TECHNICAL SPECIFICATION

This section provides detailed information about the i.MX 8 QM/QP Qseven Development Platform technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Power Input Requirement

The i.MX 8 QM/QP Qseven Carrier Board is designed to work with a +12V external power and uses on board voltage regulators for internal power management. 12V power input from an external power supply is connected to the Qseven Carrier Board through Power Jack (J4). This 2.5mm x 6.5mm barrel connector Jack should fit standard DC Plugs with an inner dimension of 2.5mm and an outer dimension of 5.5mm (DC Plug Centre Pin is Positive). This connector is physically placed at the top of the board as shown below.

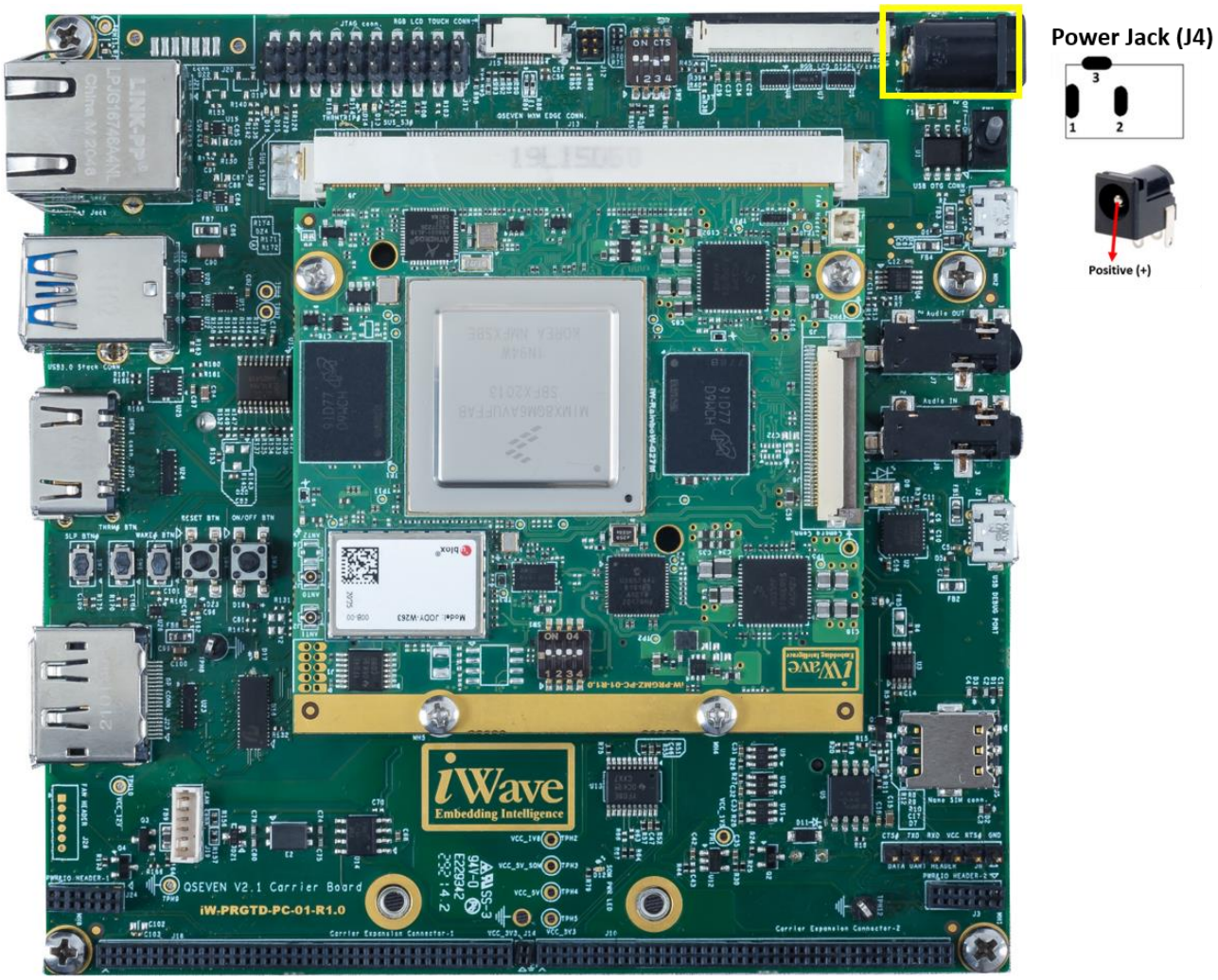


Figure 28: Power Jack

Table 17: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC_12V[1]	11.75V	12V	12.25V	±50mV
2	VRTC_3V0[2]	2.8V	3V	3.3V	±20mV

[1] Qseven Carrier Board is designed to work with 12V, 2A input power from external Power adapter.

[2] This voltage is from Coin cell holder and used as backup power source to RTC circuit of i.MX 8 QM/QP Qseven SOM when SOM VCC is off. This is an optional power and required only if RTC functionality is used.

Important Note: All carrier board power supplies should be powered ON only after the i.MX 8 QM/QP CPU is powered ON completely in the i.MX 8 QM/QP Qseven SOM. This is to ensure that there is no back voltage (leakage) from any supply on the board towards the i.MX 8 QM/QP CPU IO pins.

3.2 Power Output Specification

The i.MX 8 QM/QP Qseven Carrier Board has dedicated power regulator to provide +5V power to Qseven SOM for VCC power supply. Also +3V RTC power from coin cell holder is provided to Qseven SOM for Real time clock support.

Table 18: Power Output Specification

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Output Current (mA)
Power to Qseven SOM (through Qseven MXM connector)					
1	VCC_5V_SOM	4.85V	5V	5.15V	4000mA
2	VRTC_3V0	2.8V	3V	3.3V	-
Power to Add-On Module (through Expansion connector3)					
2	VCC_5V	4.85V	5V	5.15V	1500mA
3	VCC_3V3	3.15	3.3	3.45	1000mA
4	VCC_1V5	1.35	1.5	1.65	500mA

3.3 Environmental Characteristics

3.3.1 Environmental Specification

The below table provides the Environment specification of i.MX8 Qseven Development Platform.

Table 19: Environmental Specification

Parameters	Min	Max
Operating temperature range[1]	0°C	60°C

[1] *iWave guarantees the component selection for the given operating temperature.*

3.3.2 RoHS Compliance

iWave's i.MX 8 QM/QP Qseven Development Platform is designed by using RoHS3 compliant components and manufactured on lead free production process.

3.3.3 Electrostatic Discharge

iWave's i.MX 8 QM/QP Qseven Development Platform is sensitive to electrostatic discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the Development Platform except at an electrostatic free workstation.

3.4 Mechanical Characteristics

3.4.1 i.MX 8 QM/QP Qseven Carrier Board Mechanical Dimensions

i.MX 8 QM/QP Qseven Development Platform PCB size is 120 mm x 120 mm x 1.6mm. Qseven carrier card mechanical dimensions is shown below. (All dimensions are shown in mm)

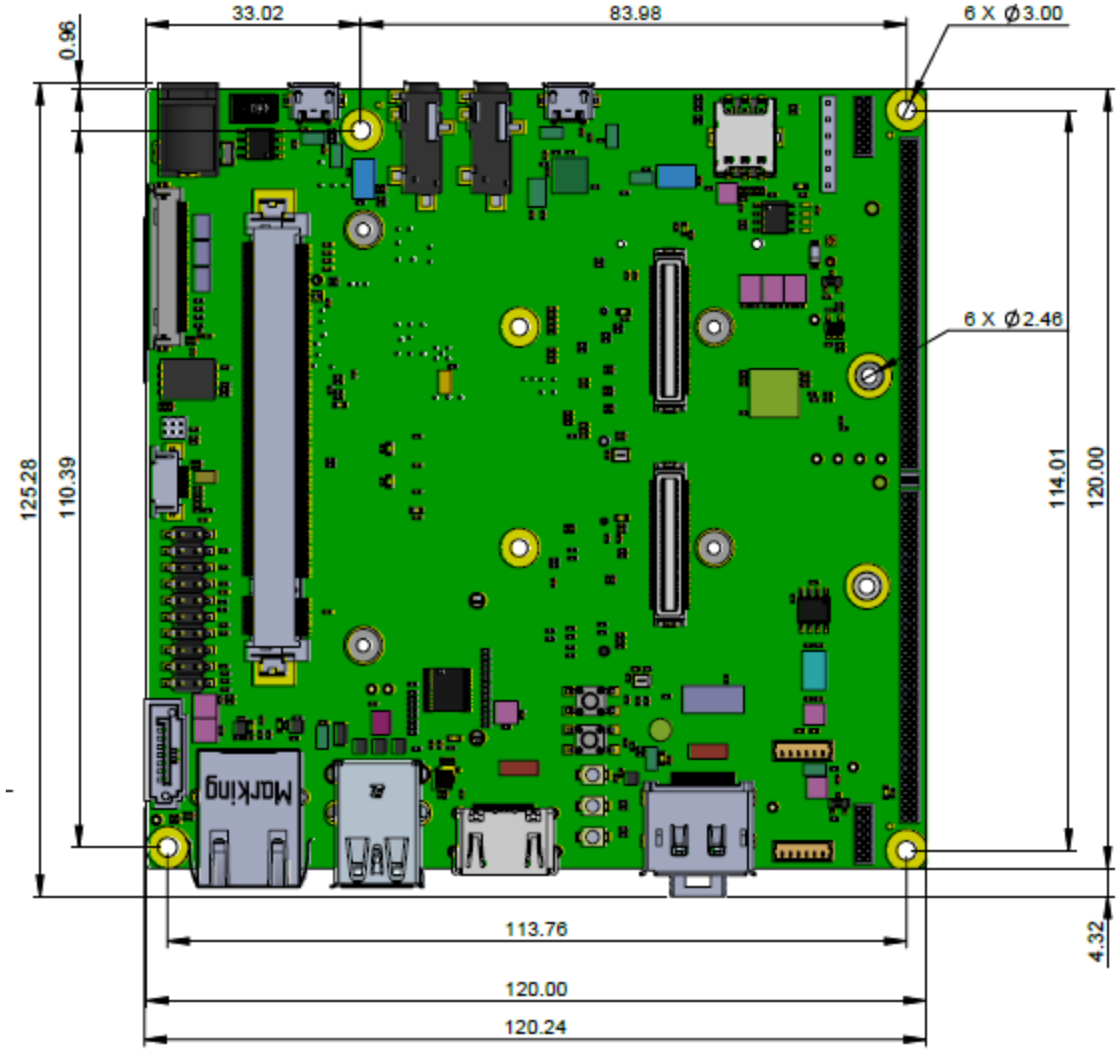


Figure 29: Mechanical dimensions of i.MX 8 QM/QP Qseven Carrier Board- Top View

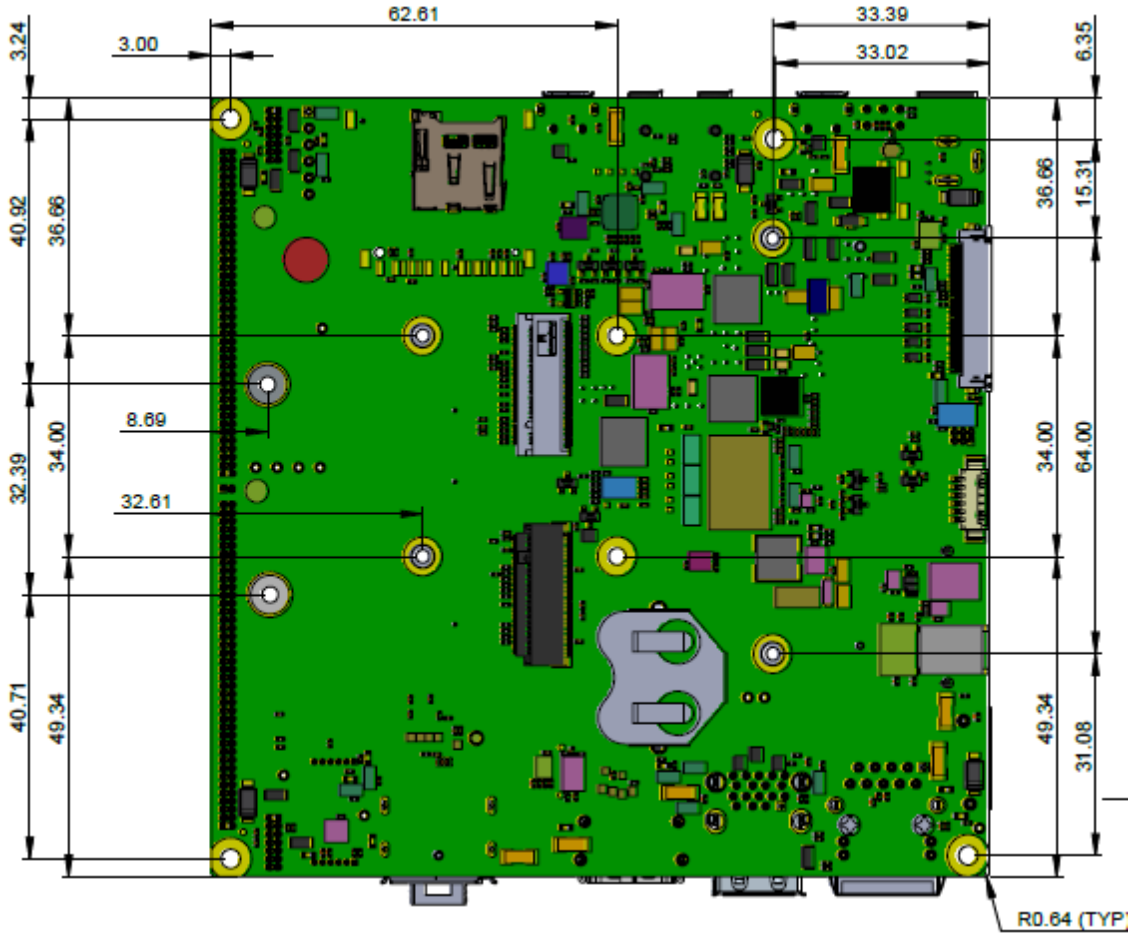
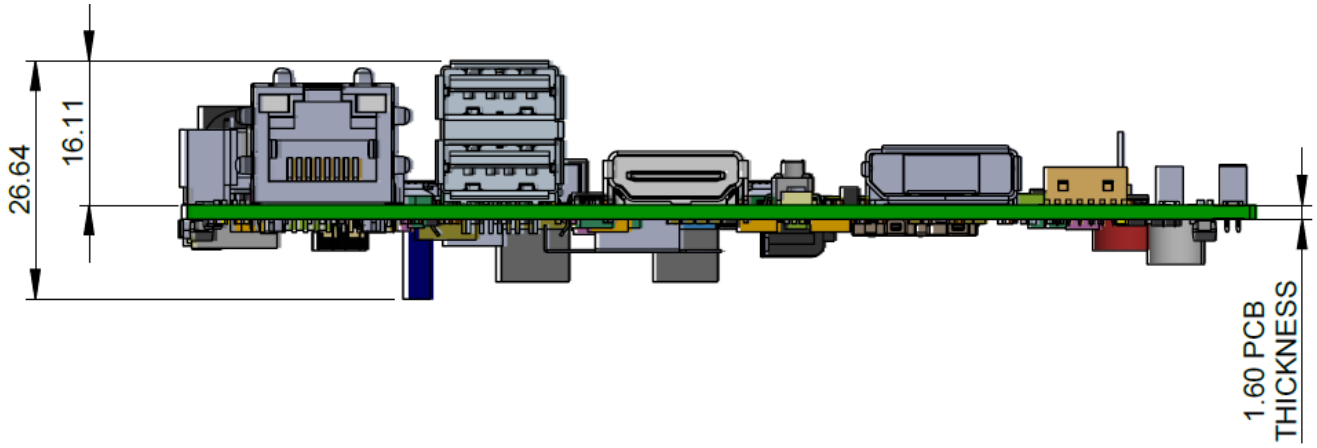


Figure 30: Mechanical dimensions of i.MX 8 QM/QP Qseven Carrier Board- Bottom View

i.MX 8 QM/QP Qseven Development Platform PCB thickness is 1.6mm±0.16mm, top side maximum height component is connector USB 3.0 Connector J22 (16.11mm) and bottom side maximum height component Ground Test Points. Please refer the below figure which gives height details of the i.MX 8 QM/QP Qseven Development kit.



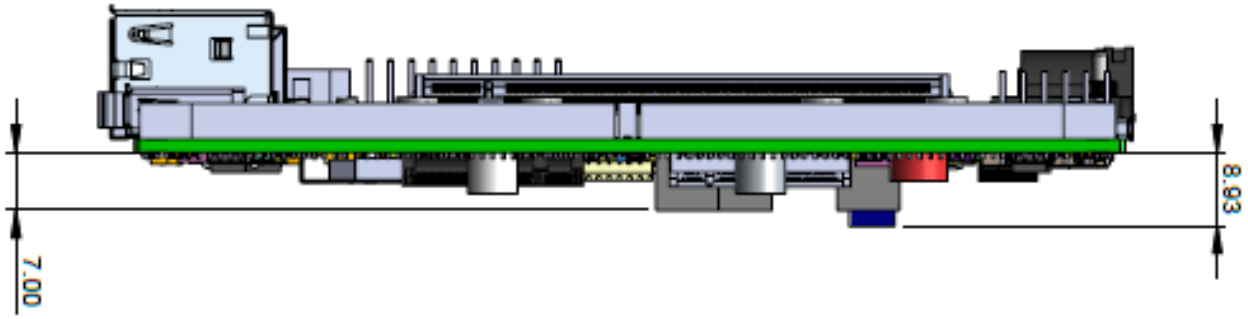


Figure 31: Mechanical dimensions of i.MX 8 QM/QP Qseven Carrier Board - Side View

3.4.2 Guidelines to insert the Qseven SOM into Carrier Board

- Make sure that power is not provided to the carrier board.
- Insert the Qseven module in to the MXM connector at an angle of 30° as shown in below image.
- Check the Notch position of Qseven module is proper while inserting.
- Once the Qseven module is inserted to the MXM connector properly, press the board vertically down as shown below, such that the board is fixed firmly into the expansion connectors and fix the board by screwing.

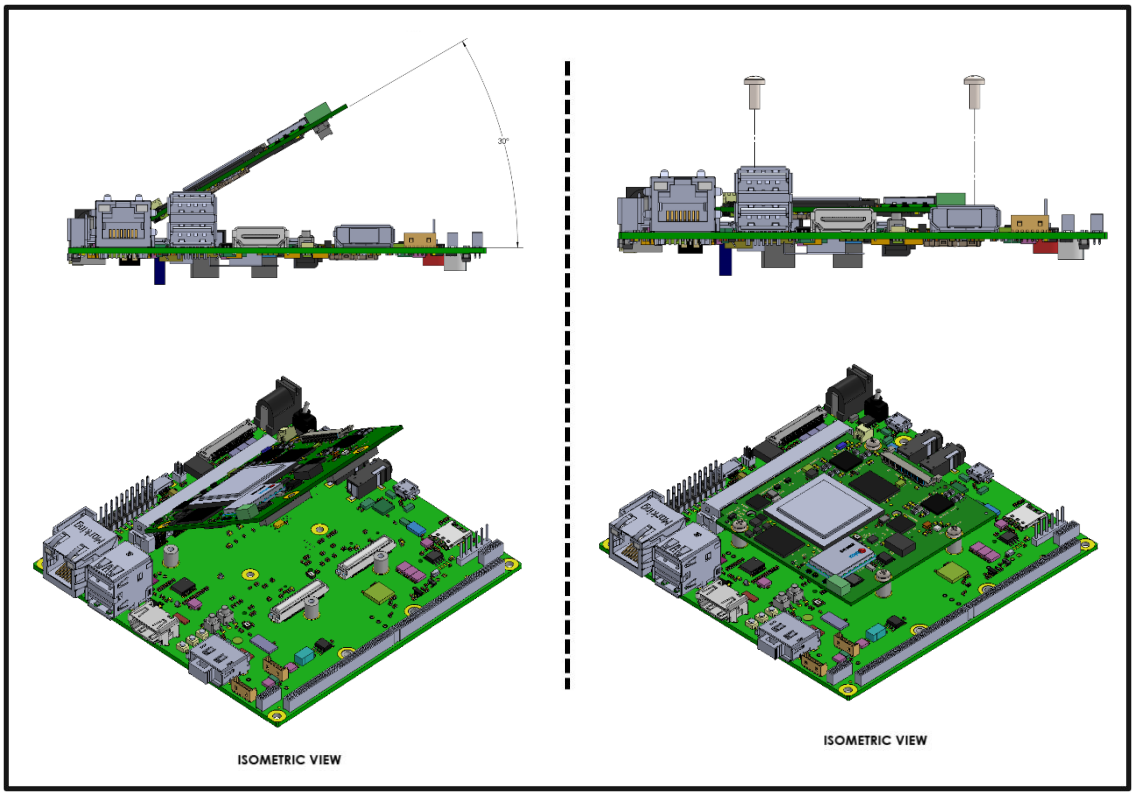


Figure 32: SOM Insertion Guideline

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for different i.MX8 QM/QP Qseven Development Platform which includes i.MX8 QM/QP Qseven SOM and Qseven carrier board.

Table 20: Orderable Product Part Numbers

Product Part Number	Description	Temperature
iW-G27D-Q7QM-4L004G-E016G-LCB	i.MX8 Quad Max, 4GB LPDDR4, 16GB eMMC flash Linux Kit without LCD display	0°C to 60°C
iW-G27D-Q7QM-4L004G-E016G-ACB	i.MX8 Quad Max, 4GB LPDDR4, 16GB eMMC flash Android Kit without LCD display	0°C to 60°C
iW-G27D-Q7QM-4L008G-E032G-LCB	i.MX8 Quad Max, 8GB LPDDR4, 32GB eMMC flash Linux Kit without LCD display	0°C to 60°C
iW-G27D-Q7QM-4L008G-E032G-ACB	i.MX8 Quad Max, 8GB LPDDR4, 32GB eMMC flash Android Kit withouts LCD display	0°C to 60°C

Note: For Development platform identification purpose, Product part number is pasted as Label with Barcode readable format.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