

Vishay Siliconix

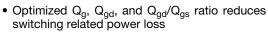
Dual N-Channel 60-V (D-S) MOSFET

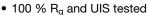


PRODUCT SUMMARY				
V _{DS} (V)	60			
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10 \text{ V}$	0.031			
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5 \text{ V}$	0.0448			
Q _g typ. (nC)	3.3			
I _D (A) ^a	6			
Configuration	Dual			

FEATURES

- TrenchFET® Gen IV power MOSFET
- Fully lead (Pb)-free device





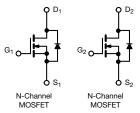
• Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT

HALOGEN FREE

APPLICATIONS

- Synchronous rectification
- · Load switch
- · Motor drive control
- · Battery management



ORDERING INFORMATION	
Package	PowerPAK 1212-8
Lead (Pb)-free and halogen-free	SiS9634LDN-T1-GE3

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	60	V
Gate-source voltage		V _{GS}	± 20	V
Continuous drain current (T _J = 150 °C)	T _C = 25 °C		6 ^a	
	T _C = 70 °C	1 . [6 ^a	
	T _A = 25 °C	l _D	6 b, f	
	T _A = 70 °C	1	5.4 b	
Pulsed drain current (t = 100 μs)		I _{DM}	24	Α
Continuous source-drain diode current	T _C = 25 °C		6 ^a	
	T _A = 25 °C	l _S	2.1 b	
Single pulse avalanche current	1 0.1 ml l	I _{AS}	10	
Single pulse avalanche energy	L = 0.1 mH	E _{AS}	5	mJ
Maximum power dissipation	T _C = 25 °C		17.9	
	T _C = 70 °C	1 5	11.4	14/
	T _A = 25 °C	P _D	2.5 ^{b, f}	W
	T _A =70 °C	1	1.6 ^{b, f}	
Operating junction and storage temperature range		T _J , T _{stq}	-55 to +150	°C
Soldering recommendations (peak temperature) c			260	- °C

THERMAL RESISTANCE RATINGS						
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT	
Maximum junction-to-ambient b, e	t ≤ 10 s	R_{thJA}	38	50	°C/W	
Maximum junction-to-case (drain)	Steady state	R_{thJC}	5.6	7	C/VV	

Notes

- a. Package limited
- b. Surface mounted on 1" x 1" FR4 board
- See solder profile (www.vishay.com/doc?73257). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components Maximum under steady state conditions is 94 $^{\circ}\text{C}$ / W t = 10 s



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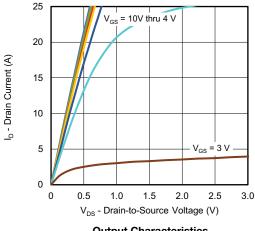
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static			•		•		
Drain-source breakdown voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	60	-	-	V	
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	I _D = 250 μA	-	33	-		
V _{GS(th)} temperature coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA	-	-4.8	-	mV/°C	
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1	-	3	V	
Gate-source leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20$	-	-	100	nA	
Zero gate voltage drain current		$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	1		
	I _{DSS}	$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 70 ^{\circ}\text{C}$	-	-	15	μA	
Drain-source on-state resistance ^a	В	V _{GS} = 10 V, I _D = 5 A	-	0.024	0.031	Ω	
	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 4 A	-	0.033	0.0448		
Forward transconductance ^a	9 _{fs}	V _{DS} = 10 V, I _D = 10 A	-	23	-	S	
Dynamic ^b							
Input capacitance	C _{iss}	V _{DS} = 30 V, V _{GS} = 0 V, f = 1 MHz -	-	420	-	pF	
Output capacitance	C _{oss}		_	92	-		
Reverse transfer capacitance	C _{rss}		4	-	1		
Total gate shares	0	$V_{DS} = 30 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 5 \text{ A}$ $V_{DS} = 30 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 5 \text{ A}$	-	7.1	11	nC	
Total gate charge	Qg		-	3.3	5		
Gate-source charge	Q _{gs}		-	1.7	-		
Gate-drain charge	Q_{gd}		-	0.9	-		
Gate resistance	R_g	f = 1 MHz	0.3	1.6	3.2	Ω	
Turn-on delay time	t _{d(on)}	V_{DD} = 30 V, R_L = 6 Ω , I_D \cong 5 A, V_{GEN} = 10 V, R_g = 1 Ω	-	10	20		
Rise time	t _r		-	5	10		
Turn-off delay time	t _{d(off)}		-	15	30		
Fall time	t _f		-	5	10	no	
Turn-on delay time	t _{d(on)}		-	12	25	ns	
Rise time	t _r	$\begin{aligned} V_{DD} &= 30 \text{ V}, \text{ R}_L = 6 \Omega, \text{ I}_D \cong 5 \text{ A}, \\ V_{GEN} &= 4.5 \text{ V}, \text{ R}_g = 1 \Omega \end{aligned}$	-	16	35		
Turn-off delay time	t _{d(off)}		-	11	25		
Fall time	t _f		-	5	10		
Drain-Source Body Diode Characterist	ics						
Continuous source-drain diode current	I _S	$T_C = 25 ^{\circ}C$	-	-	6	A	
Pulse diode forward current	I _{SM}		-	-	24		
Body diode voltage	V _{SD}	$I_S = 2 A, V_{GS} = 0 V$	-	0.8	1.2	V	
Body diode reverse recovery time	t _{rr}	I _F = 5 A, dl/dt = 100 A/μs, T _{.I} = 25 °C	-	14	30	ns	
Body diode reverse recovery charge	Q _{rr}		-	10	20	nC	
Reverse recovery fall time	t _a	1 _F = 5 Λ, αι/αι = 100 Λ/μs, 1 _J = 25 °C	-	8	-	ns	
Reverse recovery rise time	t _b		-	6	-	113	

Notes

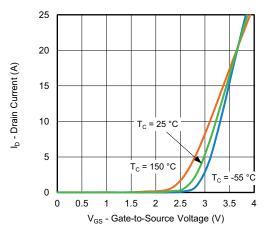
- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

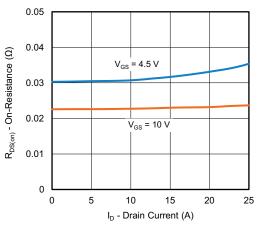




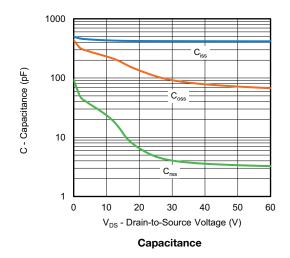
Output Characteristics

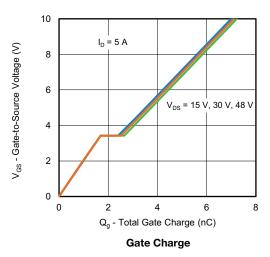


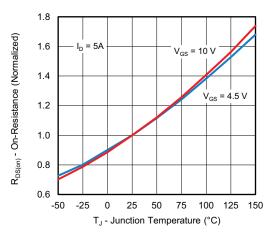
Transfer Characteristics



On-Resistance vs. Drain Current and Gate Voltage

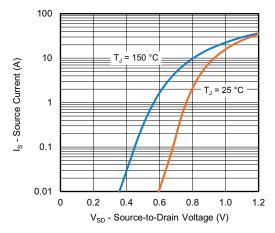




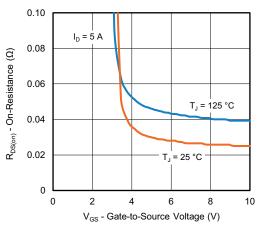


On-Resistance vs. Junction Temperature

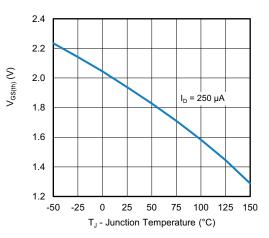




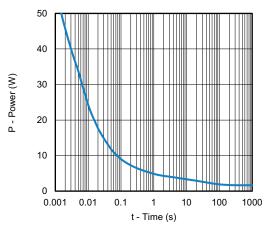
Source-Drain Diode Forward Voltage



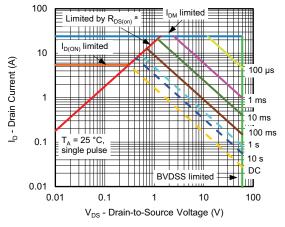
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



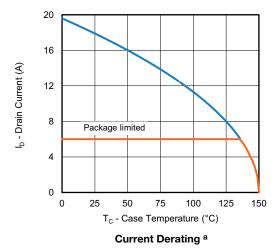
Single Pulse Power, Junction-to-Ambient

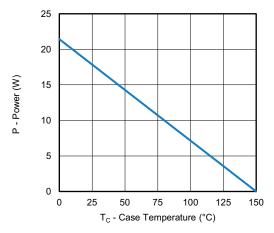


Safe Operating Area, Junction-to-Ambient

Note

a. $V_{GS} > minimum V_{GS}$ at which $R_{DS(on)}$ is specified

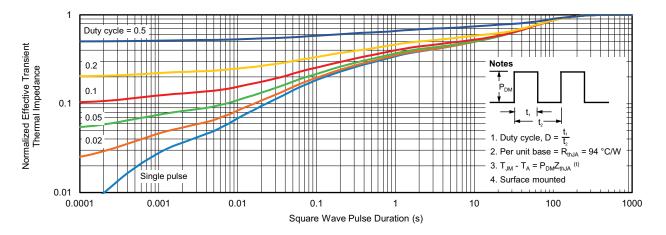




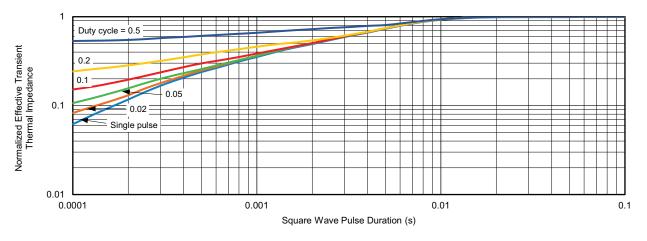
Power, Junction-to-Case

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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