100V Half-Bridge GaN Driver with Smart Integrated Bootstrap Switch

FEATURES

- **Half-Bridge Gate Driver for GaN FETs**
- **0.6Ω Pull-Up Resistance at Top Gate Driver**
- **0.2Ω Pull-Down Resistance at Bottom Gate Driver**
- **4A Peak Source, 8A Peak Sink Current Capability**
- **Smart Integrated Bootstrap Switch**
- **Split-Gate-Driver to Adjust Turn-On/Turn-Off Strength**
- **Default Low-State for All Driver Inputs and Outputs**
- **Maximum 15V Voltage Rating at INT and INB Inputs**
- **Independent INT, INB Inputs with TTL Logic Compatible**
- **Fast Propagation Delay: 10ns (Typical)**
- **Propagation Delay Matching: 1.5ns (Typical)**
- **Balanced Driver Supply Voltage: $V_{BST} \approx V_{CC}$ = 3.85V – 5.5V**
- Undervoltage and Overvoltage Lockout Protections
- Small 12-Ball WLCSP Package

APPLICATIONS

- High Frequency DC-DC Switching Power Converters
- Half-Bridge, Full-Bridge, Push-Pull Converters
- Data Center Power Supplies
- Motor Drivers, Class-D Audio Amplifiers
- Consumer, Industrial, and Automotive

GENERAL DESCRIPTION

The LT8418 is a 100V half-bridge GaN driver that integrates top and bottom driver stages, driver logic control, and protections. It can be configured into synchronous half-bridge, full-bridge topologies, or buck, boost, and buck-boost topologies. The LT8418 provides strong current sourcing/sinking capability with 0.6Ω pull-up and 0.2Ω pull-down resistance. It also integrates smart integrated bootstrap switch to generate a balanced bootstrap voltage from V_{CC} with a minimum dropout voltage.

The LT8418 provides split gate drivers to adjust the turn-on and turn-off slew rates of GaN FETs to suppress ringing and optimize EMI performance. All driver inputs and outputs have default low-state to prevent GaN FETs from false turn-on. The inputs of the LT8418, INT, and INB are independent and TTL logic compatible. Meanwhile, the LT8418 performs with a fast propagation delay of 10ns and maintains an excellent delay matching of 1.5ns between the top and bottom channels, making it suitable for high-frequency DC-DC converters, motor drivers, and class-D audio amplifiers. In addition, the LT8418 employs the WLCSP package to minimize parasitic inductance, enabling its wide use in high-performance and high-power density applications.

TYPICAL APPLICATION

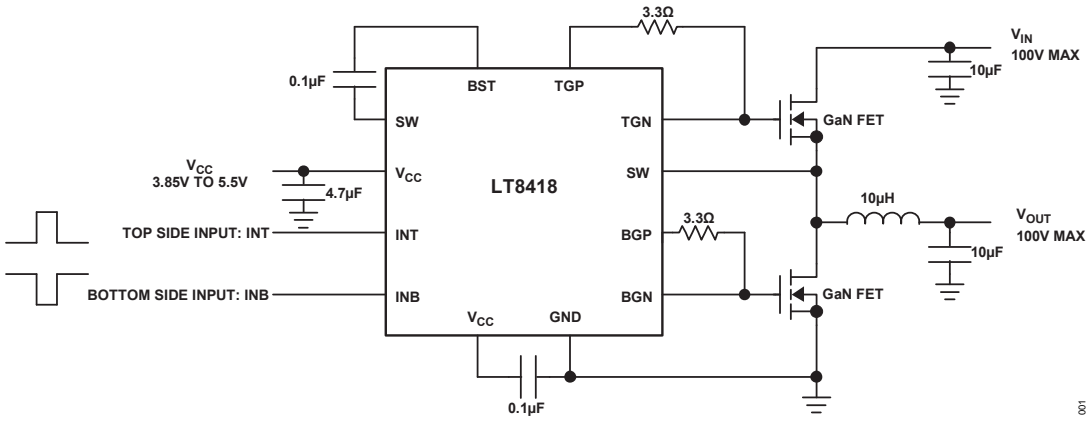

Figure 1. Highly Efficient GaN-Based Switching DC-DC Converter

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REVISION HISTORY

10/2023 – Rev. 0

SPECIFICATIONS

Table 1. Electrical Characteristics

(T_A = 25°C[1], V_{CC} = V_{BST} = 5V, V_{GND} = V_{SW} = 0V; TGP and TGN are connected; BGP and BGN are connected)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Supply Voltage and Current						
V_{CC} Operating Voltage Range	V_{CC}		3.85		5.5	V
V_{CC} Quiescent Current	I_{Q_VCC}	INT = INB = 0V		250		µA
V_{CC} Operating Current	I_{VCC}	F_{SW} = 400kHz		2.4		mA
BST Quiescent Current	I_{Q_BST}	INT = INB = 0V		80		µA
BST Operating Current	I_{BST}	F_{SW} = 400kHz		1.0		mA
Undervoltage, Overvoltage Protections						
V_{CC} UVLO Threshold	V_{UVLO_VCC}	Falling	3.14	3.35	3.67	V
V_{CC} UVLO Hysteresis	$V_{UVLO\_HYST\_VCC}$			0.2		V
V_{CC} OVLO Threshold	V_{OVLO_VCC}	Rising	5.58	6.0	6.53	V
V_{CC} OVLO Hysteresis	$V_{OVLO\_HYST\_VCC}$			0.2		V
BST UVLO Threshold	V_{UVLO_BST}	Falling	2.9	3.1	3.35	V
BST UVLO Hysteresis	$V_{UVLO\_HYST\_BST}$			0.25		V
Input Pins						
INT, INB Input Turn-On Threshold	V_{ON_INT} V_{ON_INB}	Rising	1.4	1.9	2.4	V
INT, INB Input Hysteresis	V_{HYST_INT} V_{HYST_INB}			0.4		V
INT, INB Input Resistance to Ground	R_{INT} R_{INB}			200		kΩ
Bootstrap Switch						
BST Switch Forward Drop at Low Refresh Current	V_{F_BST}	$I_{VCC-BST}$ = 100 µA		1	10	mV
BST Switch Forward Drop at High Refresh Current	V_{F_BST}	$I_{VCC-BST}$ = 100 mA		0.6	1	V
BST Switch Dynamic On-Resistance	R_{BST}	$I_{VCC-BST}$ = 100 mA		6		Ω
Gate Drivers						
TG Driver R_{ON} Gate Pull-Up Gate Pull-Down	 R_{TG_UP} R_{TG_DW}	$V_{(BST-SW)}$ = 5V		 0.6 0.2		 Ω Ω
BG Driver R_{ON} Gate Pull-Up Gate Pull-Down	 R_{BG_UP} R_{BG_DW}	V_{CC} = 5V		 0.6 0.2		 Ω Ω

(T_A = 25°C[1], V_{CC} = V_{BST} = 5V, V_{GND} = V_{SW} = 0V; TGP and TGN are connected; BGP and BGN are connected)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
TG Rise Time	t_{TGR}	CL = 1nF, 10% to 90%		2.5		ns
TG Fall Time	t_{TGF}	CL = 1nF, 90% to 10%		2.5		ns
BG Rise Time	t_{BGR}	CL = 1nF, 10% to 90%		2.5		ns
BG Fall Time	t_{BGF}	CL = 1nF, 90% to 10%		2.5		ns
Propagation Delay, Delay Matching, and Minimum Input Pulse[2]						
TG Turn-On Propagation Delay	t_{RPD_TG}	INT Rising to TG Rising (TGP = TGN = TG)		10	16	ns
TG Turn-Off Propagation Delay	t_{FPD_TG}	INT Falling to TG Falling		10	15	ns
BG Turn-On Propagation Delay	t_{RPD_BG}	INB Rising to BG Rising (BGP = BGN = BG)		10	16	ns
BG Turn-Off Propagation Delay	t_{FPD_BG}	INB Falling to BG Falling		10	15	ns
TG Turn-Off and BG Turn-On Delay Mismatch	t_{DMF}			0.5	5	ns
BG Turn-Off and TG Turn-On Delay Mismatch	t_{DMR}			0.5	6.5	ns
TG, BG Minimum Input Pulse Width	t_{TGW}, t_{BGW}			11		ns

1 The LT8418 is tested under pulsed load conditions such that $T_J \approx T_A$. The LT8418A is guaranteed to meet specifications from –40°C to 125°C junction temperature. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance, and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the formula: $T_J = T_A + (P_D \times J_A)$, where θ_{JA} (in °C/W) is the package thermal impedance.

2 The definition of propagation delay for the top or bottom side gate driver and delay matching is illustrated in the following timing diagram.

Timing Diagrams

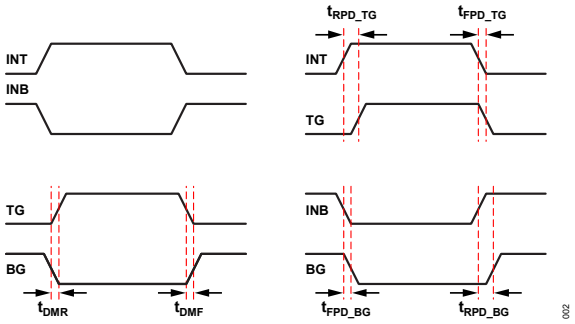


Figure 2. Timing Definitions of Propagation Delay and Delay Matching

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C[1], unless otherwise specified.

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
INB, INT	–0.3V to 15V
V_{CC}, (BST – SW)	–0.3V to 6V
BGP, BGN	–0.3V to V_{CC} + 0.3V
TGP, TGN	SW – 0.3V to BST + 0.3V
BST	–0.3V to 106V
BST (at 100ms Transient)	–0.3V to 116V
SW	-5V to 100V
SW (at 100ms Transient)	-5V to 110V
Operating Junction Temperature Range[2,3] LT8418A	-40°C to 125°C
Storage Temperature Range	-65°C to 150°C

1 Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. Exposure to any absolute maximum rating condition for extended periods may affect device reliability and lifetime.

2 The LT8418 is tested under pulsed load conditions such that $T_J \approx T_A$. The LT8418A is guaranteed to meet specifications from –40°C to 125°C junction temperature. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance, and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the formula: $T_J = T_A + (P_D \bullet J_A)$, where θ_{JA} (in °C/W) is the package thermal impedance.

3 The LT8418 includes overtemperature protection intended to protect the device during momentary overload conditions. The maximum rated junction temperature is exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

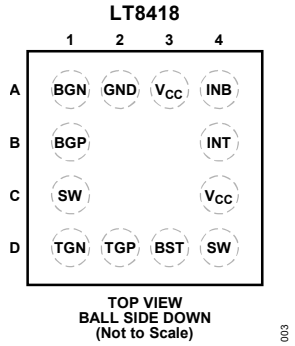
Thermal Resistance

Thermal performance is directly linked to PCB design and operating environment. Close attention to PCB thermal design is required.

Table 3. 12-Ball WLCSP Package Thermal Resistance

Thermal Resistance	
Junction-to-Ambient Θ_{JA}	73 °C/W
Junction-to-Case $\Theta_{JC\ (TOP)}$	0.6 °C/W
Junction-to-Board $\Theta_{JB\ (BOTTOM)}$	12 °C/W

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



12-Ball WLCSP Package

Package Size: 1.67mm x 1.67mm, Ball Diameter: 0.26mm, Ball Pitch Size: 0.4mm

Figure 3. Pin Diagram

Pin Descriptions

Table 4. Pin Descriptions

PIN	NAME	DESCRIPTION
A1	BGN	Pull-down branch in bottom side split gate driver output. Adding a resistor from BGN to GaN FET's gate can program the turn-off strength of the bottom side GaN FET.
A2	GND	Ground. Connect this pin to the source of the bottom side GaN FET with low inductance and resistance.
A3, C4[1]	V_{CC}	Power supply for the internal control circuitry and gate drivers. Locally bypassing this pin to ground with a minimum 4.7µF ceramic capacitor.
A4	INB	PWM input to control bottom-side gate driver. INB is TTL input logic compatible, with a default 200 kΩ pull-down resistance internally. Leave it open or tie it to ground when it is not used.
B1	BGP	Pull-up branch in bottom side split gate driver output. Adding a resistor from BGP to GaN FET's gate can program the turn-on strength of the bottom side GaN FET.
B4	INT	PWM input to control top-side gate driver. INT is TTL input logic compatible, with a default 200 kΩ pull-down resistance internally. Leave it open or tie it to ground when it is not used. The minimum input pulse width for INT is 11ns.
C1, D4[1]	SW	Switch Node. Connect SW to the source of the top synchronous GaN FET and the bottom terminal of the bootstrap capacitor with low inductance and resistance.
D1	TGN	Pull-down branch in top side split gate driver output. Adding a resistor from TGN to the GaN FET's gate can program the turn-off strength of the top side GaN FET.
D2	TGP	Pull-up branch in top side split gate driver output. Adding a resistor from TGP to the GaN FET's gate can program the turn-on strength of the top side GaN FET.
D3	BST	Bootstrap Floating Driver Supply. The BST pin has an on-die bootstrap switch from the V_{CC}, and an external bootstrap capacitor to the SW pin can be used to provide a stable and well-balanced bootstrap voltage for the top side gate driver. Locally bypass this pin to SW with a minimum 100nF ceramic capacitor.

[1] A3 and C4 are internally connected. C1 and D4 are internally connected.

BLOCK DIAGRAM

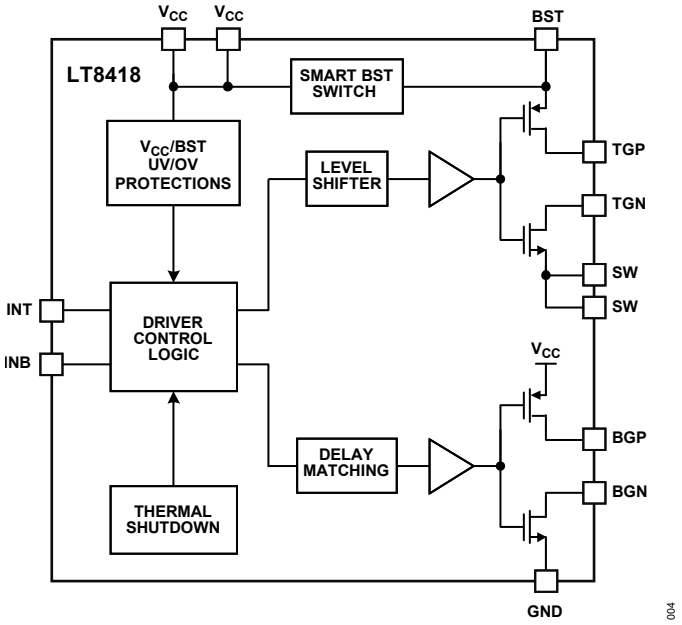


Figure 4. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

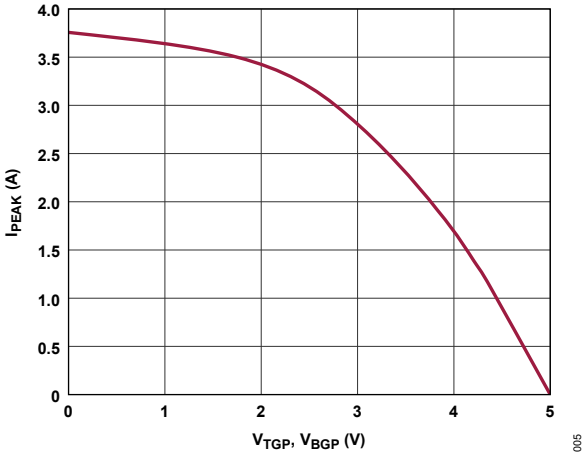


Figure 5. Peak Source Current vs. Driver Ouput Voltage

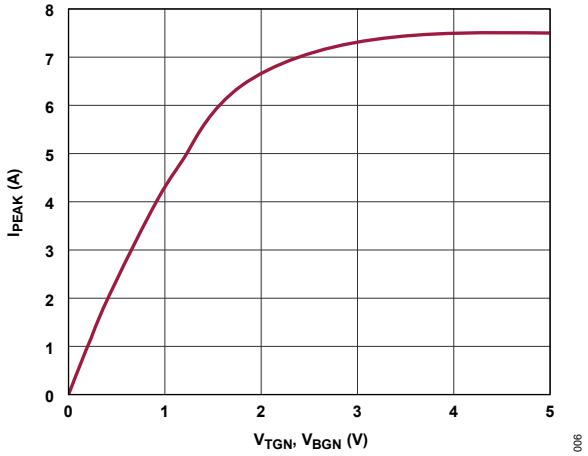


Figure 6. Peak Sink Current vs. Driver Ouput Voltage

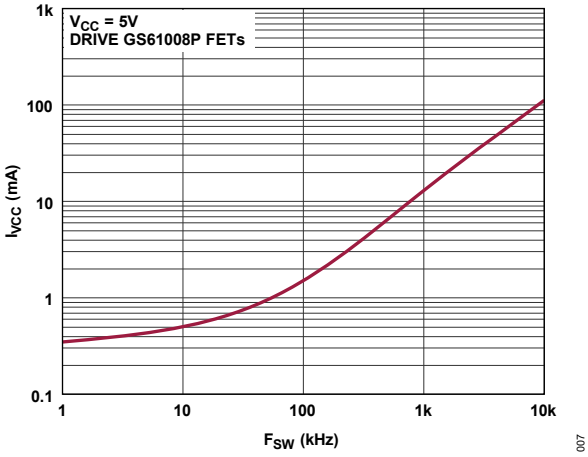


Figure 7. V_{CC} Operating Current vs. Switching Frequency

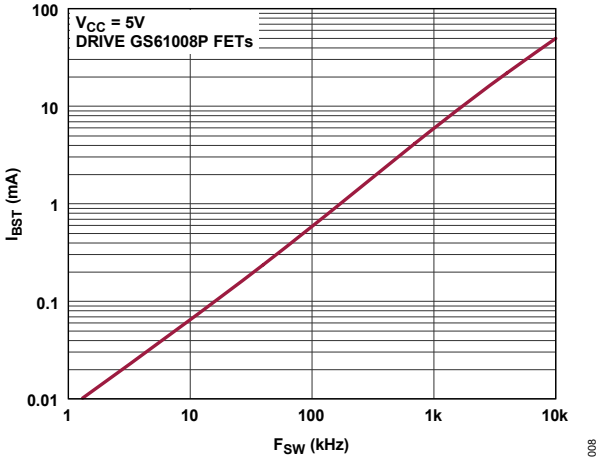


Figure 8. BST Operating Current vs. Switching Frequency

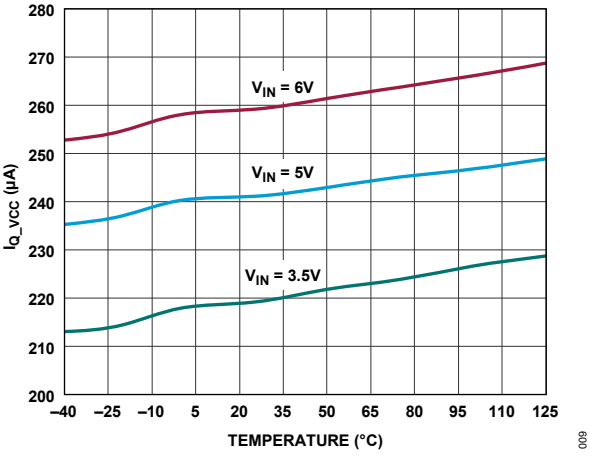


Figure 9. V_{CC} Quiescent Current vs. Temperature

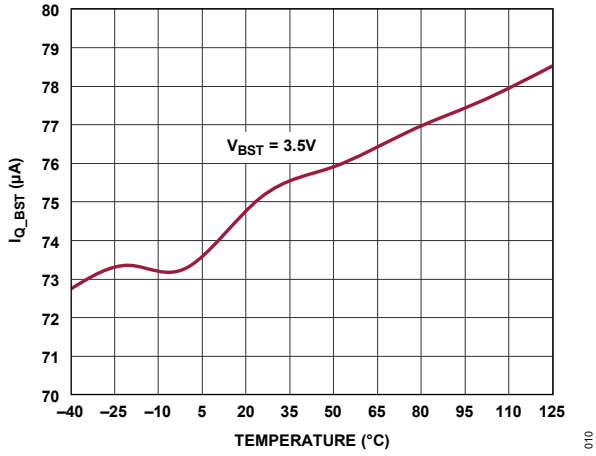


Figure 10. BST Quiescent Current vs. Temperature

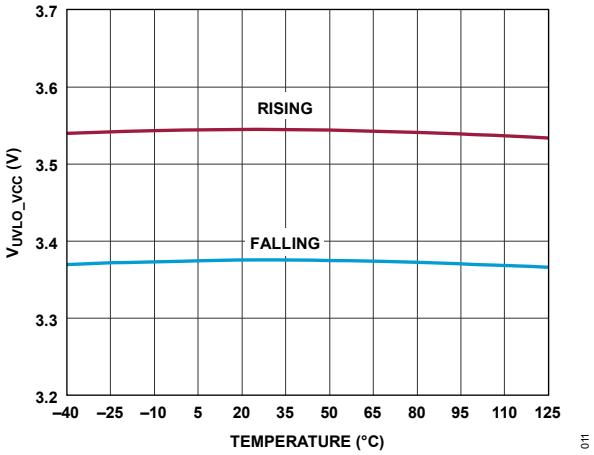


Figure 11. V_{CC} UVLO Threshold vs. Temperature

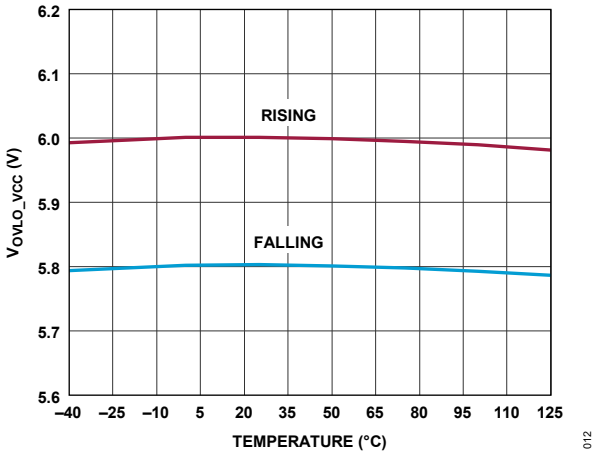


Figure 12. V_{CC} OVLO Threshold vs. Temperature

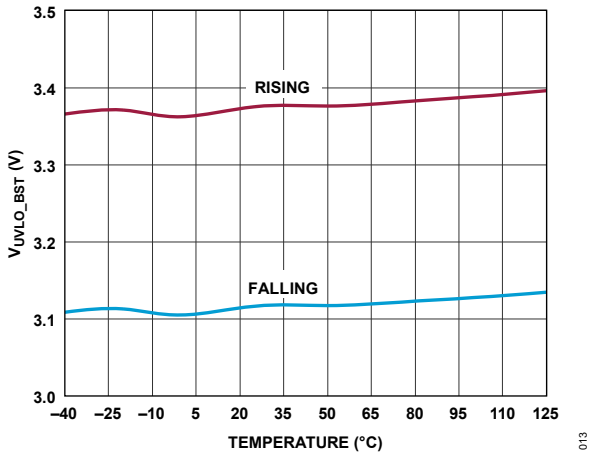


Figure 13. BST UVLO Threshold vs. Temperature

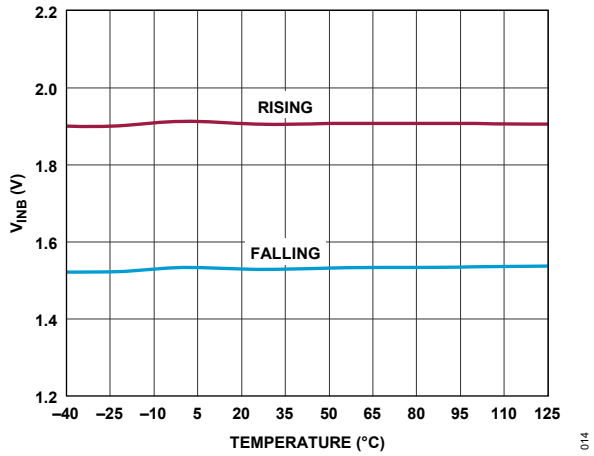


Figure 14. INB Threshold vs. Temperature

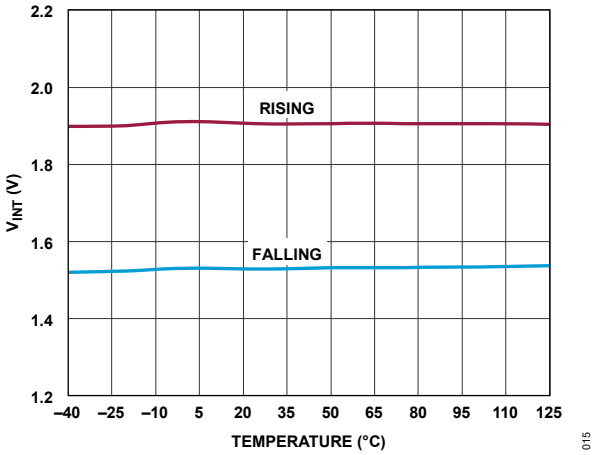


Figure 15. INT Threshold vs. Temperature

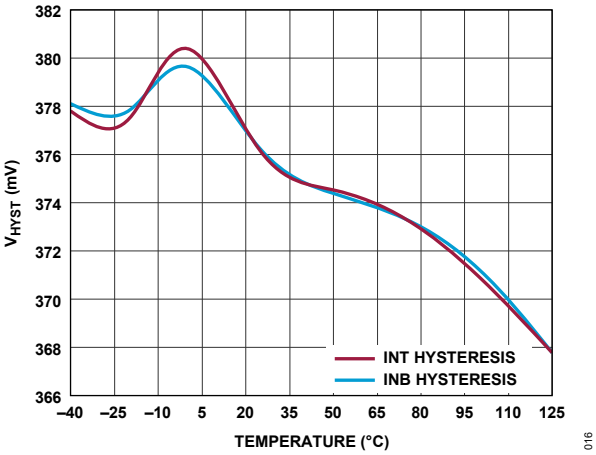


Figure 16. Input Threshold Hysteresis vs. Temperature

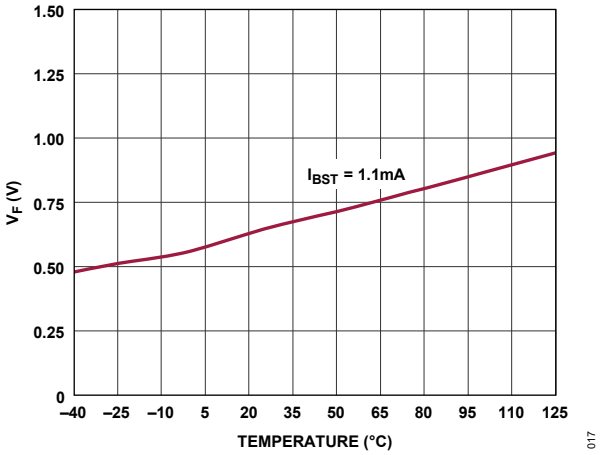


Figure 17. Bootstrap Switch Voltage vs. Temperature

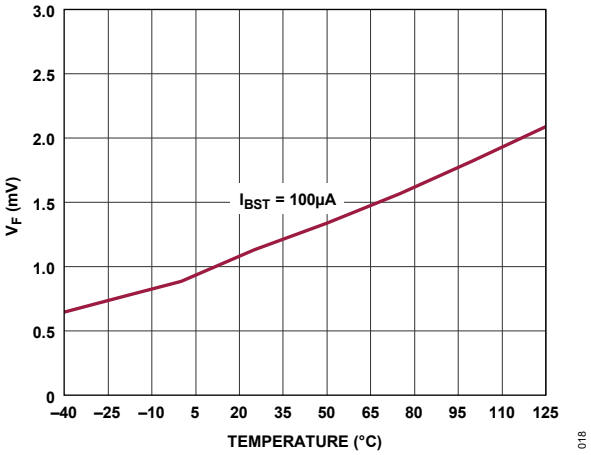


Figure 18. Bootstrap Switch Voltage vs. Temperature

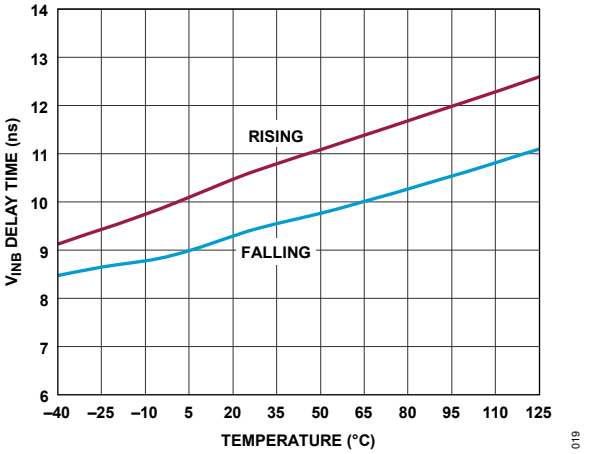


Figure 19. INB Propagation Delay vs. Temperature

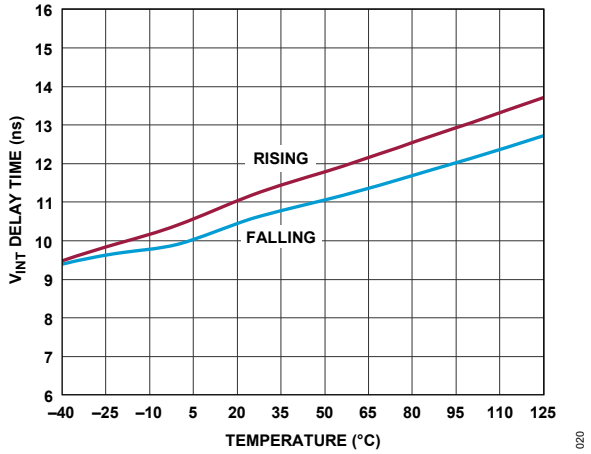


Figure 20. INT Propagation Delay vs. Temperature

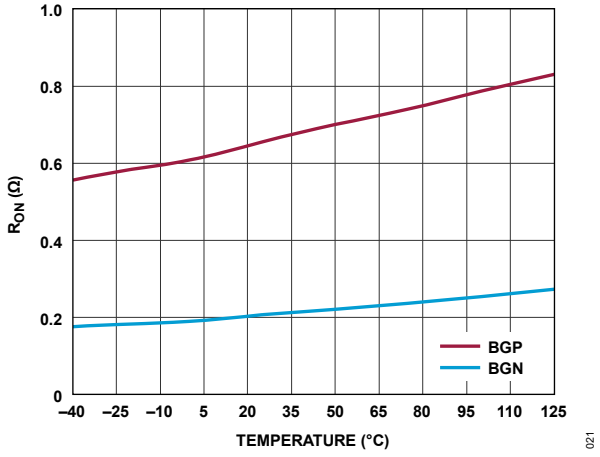


Figure 21. BG On-Resistance vs. Temperature

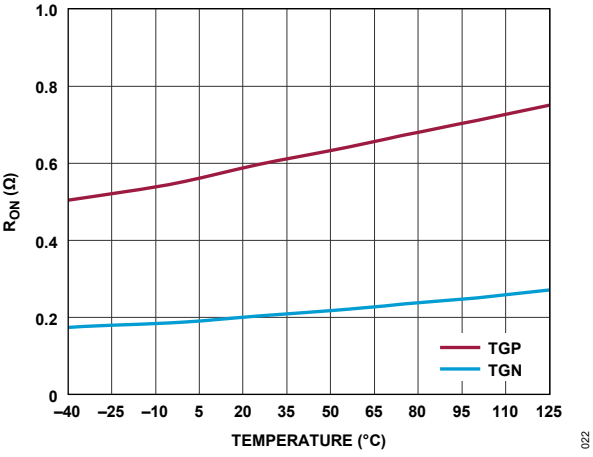


Figure 22. TG On-Resistance vs. Temperature

THEORY OF OPERATION

The LT8418 is a 100V half-bridge GaN driver that integrates top, bottom gate drivers, V_{CC}, BST, UV, and OV protection control logic. It can be used in half bridges and full bridges. It is very flexible to support multiple topologies including buck, boost, buck-boost, and a variety of applications, including data center power, class-D audio amplifier, and motor drivers. In addition, the LT8418 employs a small-footprint WLCSP package, which can be used in different applications requiring high-power density, high-frequency operation, small form factor, and low cost.

1.1. Chip Start-up, V_{CC} UVLO/OVLO Protections

The LT8418 has an undervoltage lockout (UVLO) in the V_{CC} drive power rail. When the V_{CC} voltage is falling below the threshold voltage of 3.35 V, both the TG and BG pins are turned off to prevent the GaN FETs from being falsely turned on. When the V_{CC} voltage rises above its UVLO threshold of 3.55V (with 200mV hysteresis voltage), the LT8418 is activated after a 100µs wakeup time. After that, the LT8418 senses INT and INB signals, and controls TG and BG outputs. Due to the charging time of the BST rail, TG is prohibited from turning on until the BST UV threshold of 3.35V is reached. On the other hand, to protect the GaN FETs from overdrive voltage and gate damage, V_{CC} OVLO (overvoltage lockout) feature is integrated into the LT8418. When the V_{CC} voltage rises above 6.0V, V_{CC} OV is triggered, which turns off both TG and BG; until the V_{CC} voltage falls below 5.8V, V_{CC} OV is recovered and TG/BG starts to switch again following INT and INB control signals.

1.2. Input Interface INT, INB

The input pins of the LT8418 are independently controlled with TTL input thresholds and can withstand voltages up to 15V. This allows the inputs to be directly connected to the outputs of an analog PWM controller with up to 15V power supply, eliminating the need for a buffer stage. The LT8418 input pins, INT and INB, are independent and TTL logic compatible. The LT8418 provides a fast propagation delay of 10ns and maintains an excellent delay matching of 2.5ns between the top and bottom channels, making it suitable for high-frequency switching operations. Both driver input pins, INT and INB, have a default pull-down resistor of 200kΩ to prevent GaN FETs from false turn-on. LT8418 does not implement an overlap protection. If both INT and INB are asserted, both the high-side and low-side GaN FETs are turned on. Careful consideration must be applied to the input interface to avoid a possible shoot-through condition.

1.3. Smart Bootstrap (BST) Switch and BST UVLO

During the dead time interval between TG turn-off to BG turn-on, or between BG turn-off to TG turn-on, the GaN power switch demonstrates a high reverse conduction voltage of 2V ~ 3V from source to drain (even higher at high conduction current), which can bring SW node down to –2V ~ –3V and leads to the overcharge of BST rail and permanent gate damage of GaN power switch. In the LT8418, the smart BST switch consists of power switches that can be fully controllable for BST charging or blocking. When the bottom switch is turned on and the switching node voltage is close to ground level, the BST switch is turned on to start charging the BST capacitor. In this way, the LT8418 is able to generate a well-balanced bootstrap voltage from V_{CC} with a minimum dropout voltage, which prevents GaN FETs from overcharge and gate damage, as well as achieves matched propagation delay between the top and bottom drivers and maintains balanced gate drive strength. The LT8418 provides a bootstrap UVLO protection to prevent GaN FETs from turn-on at an insufficient gate drive voltage. When the BST-SW rail falls below 3.1V, TG stops to turn on until the BST capacitor is replenished and the BST rail rises above 3.35V (250mV hysteresis), and TG starts to switch again.

1.4. Split Gate Driver

The LT8418 also provides split gate drivers for both top and bottom power switches. Thus, turn-on and turn-off slew rates of the top and bottom gate drivers are adjustable independently by connecting different values of gate resistors at TGP, TGN, BGP, and BGN pins. Besides, the LT8418 integrates strong gate drivers with 0.6Ω pull-up resistance, 0.2Ω

pull-down resistance, a strong 4A current sourcing, and 8A current sinking capability, which is suited to use to drive a variety of GaN FETs with different Q_G or $R_{DS(ON)}$ values. All driver outputs, TGP and TGN, have default 500kΩ pull-down resistance to SW node; BGP and BGN have default 500kΩ pull-down resistance to ground to prevent top and bottom GaN FETs from false turn-on.

APPLICATIONS INFORMATION

The front page shows a typical LT8418 application circuit. This section serves as a guideline for selecting external components for typical applications.

1.1. Selecting the V_{CC} and BST Capacitor

The LT8418 can support a wide range of switching frequencies. Thus, the V_{CC} and BST capacitors must be selected properly based on the system switching frequency, Q_G, of GaN FETs.

The bypass capacitor C_{VCC} provides the gate charge for the top-side and bottom-side GaN FETs. The charge to turn on the external GaN FET is referred as gate charge, Q_G, and is typically specified in the external GaN FET data sheet. Gate charge depends on the gate drive level and external GaN FET, ranging from 1nC to tens of nC. The required bypass capacitance can be approximated as:

$$C_{VCC} > \frac{Q_{GT} + Q_{GB}}{\Delta V} \quad (1)$$

where:

Q_{GT} and Q_{GB} are the gate charge of the top-side and bottom-side GaN FETs, respectively.

ΔV is the maximum allowable voltage drop across C_{VCC}.

An external boost capacitor, C_{BST}, connected between BST and SW, supplies the gate driver voltage for its respective GaN FET driver. To turn on the external GaN FET, the driver places the CBST voltage across the gate and source of the GaN FET. The C_{BST} capacitance must have at least ten times the gate capacitance to fully turn on the external GaN FET. For most applications, a capacitor value of 0.1uF for C_{BST} is sufficient. However, if multiple GaN FETs are paralleled and driven by the LT8418, the C_{BST} capacitance must be increased correspondingly and should be maintained in the following relationship:

$$C_{BST} > \frac{10Q_{GT,TOTAL}}{1V} \quad (2)$$

A BST switch is integrated into the LT8418 to keep charging the C_{BST}, eliminating the requirement of the external V_{CC}-to-BST Schottky diode. An additional diode from V_{CC} to BST may cause the overcharge of the BST rail and gate damage of high side GaN FET. When the BG/TG is low, the total current from V_{CC} is typically 250μA; when the BG/TG is switching at 400kHz with a 1nF capacitance load at driver outputs, the total current from V_{CC} is typically 2.4mA.

1.2. Selecting the Gate Resistance

The LT8418 provides split gate drivers for top and bottom GaN power switches. A typical gate resistor up to 5.6Ω can be added to TGP/TGN and BGP/BGN pins to adjust the turn-on/turn-off rate of two GaN FETs for electromagnetic interference (EMI) and efficiency optimization.

1.3. Power Dissipation

The major power dissipation on the LT8418 is the sum of the power loss on the gate driver and the BST switch. The gate driver loss is caused by charging and discharging the gate capacitance of the GaN FETs. Because the gate loss

occurs once per cycle, it is proportional to the switching frequency. Unlike a pure capacitive load, a power GaN FET's gate capacitance seen by the driver output varies with its V_{GS} voltage level (V_{CC} in this case) during switching. For simplicity, the gate power dissipation can be calculated using its gate charge Q_G. For identical GaN FETs on BG and TG, the gate loss is:

$$P_{gate} = 2Q_G \cdot V_{CC} \cdot f_{sw} \quad (3)$$

The reverse recovery loss and forward bias power loss on the traditional bootstrap diode are avoided by using the integrated BST switch. The BST switch loss is dominated by the conduction loss on its $R_{DS(ON)}$ while charging the capacitor. Larger GaN FET gate capacitance requires more current to charge the BST capacitor, resulting in more loss:

$$P_{BST} = D \cdot I_{BST}^2 \cdot R_{DS(ON),BST} \quad (4)$$

where:

I_{BST} is the BST operating current charging the top-side gate capacitance.

$R_{DS(ON),BST}$ is the on-resistance of the BST switch.

1.4. PCB Bypass and Grounding Guideline

The LT8418 requires proper bypassing on the V_{CC}, BST-SW supplies due to its high-speed switching (nanoseconds) and large AC currents. Careless component placement and PCB routing may cause excessive ringing and undershoots/overshoots.

To obtain the optimum performance from the LT8418:

- Mount the capacitors as close as possible between the V_{CC} and GND pins, and the BST and SW pins. The traces should be shortened as much as possible to reduce lead inductance.
- Use a low-inductance, low-impedance ground plane to reduce any ground drop and stray capacitance. Remember that the LT8418 can sink up to 8A peak currents and any significant ground drop degrades signal integrity.
- Plan the power/ground routing carefully. Know where the large load switching current is coming from and going. Maintain separate ground return paths for the input pin and output power stage.
- Kelvin connect the TG pin to the top GaN FET gate and SW pin to the top GaN FET source. Kelvin connect the BG pin to the bottom GaN FET gate and the driver ground to the bottom GaN FET source. Keep the copper trace between the driver output pin and load short and wide.

1.5. Soldering Guideline

Precondition the solder pad with flux for better solder flow. Because of the small solder balls, type 4 solder paste (20 microns to 38 microns grain size) or finer solder paste is recommended to apply on the pad. After placing the IC manually, a telescope should be used to ensure a good alignment. For better accuracy, it is recommended to use automated fine-pitch placement machines with vision alignment. Melt the solder paste using a hot plate instead of a heat gun to prevent the IC from being blown away. To verify good connections, vision inspection, and X-ray inspection are recommended. Failure to make good electrical or thermal contact between the balls and the copper board causes driver or system malfunction or higher thermal resistance.

OUTLINE DIMENSIONS

12-Ball Wafer Level Chip Scale Package (WLCSP)
(CB-12-17, Unit: millimeter)

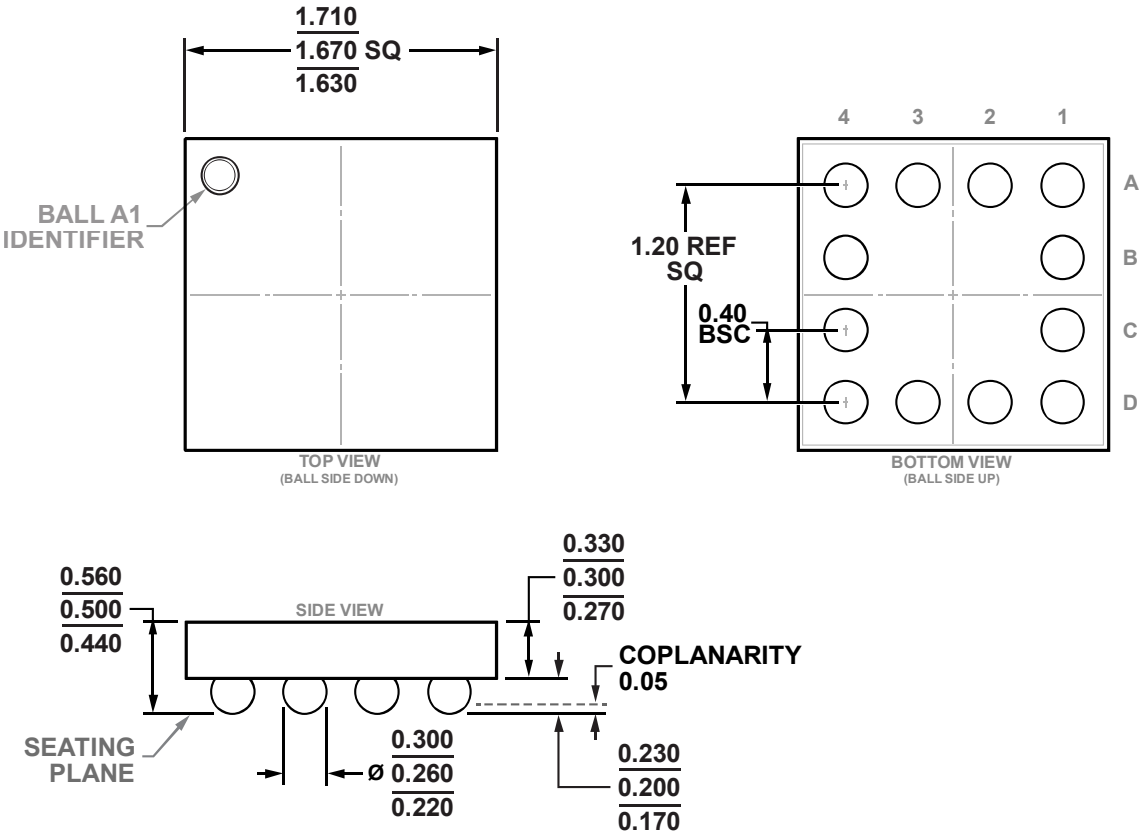


Figure 23. Package Drawing

TYPICAL APPLICATIONS

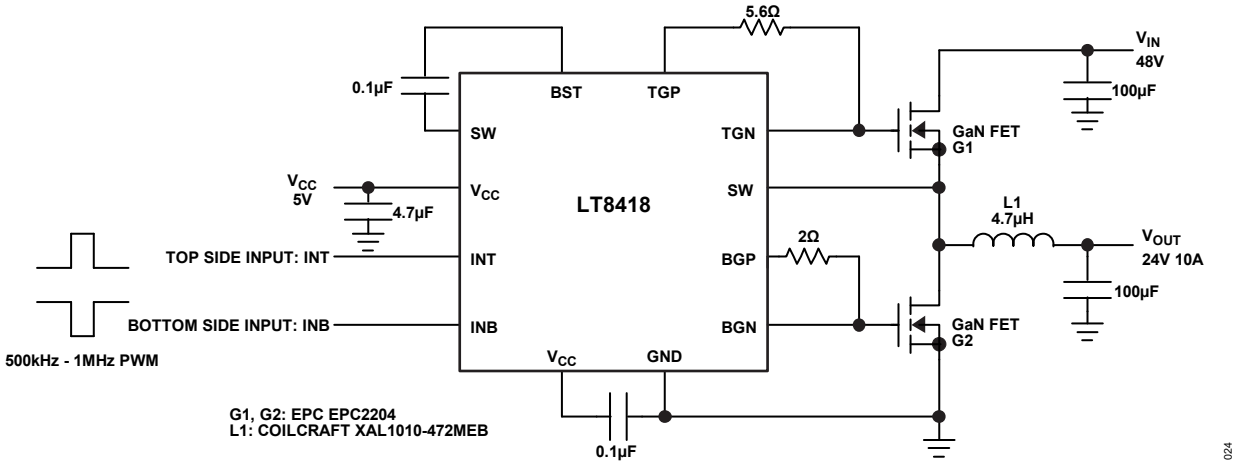


Figure 24. 48V Input, 24V and 10A Output, 500kHz to 1MHz Buck Converter

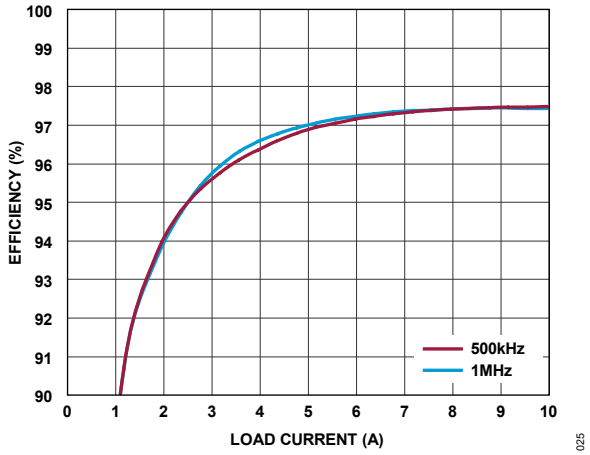


Figure 25. Efficiency vs. Load Current (with Forced Air)

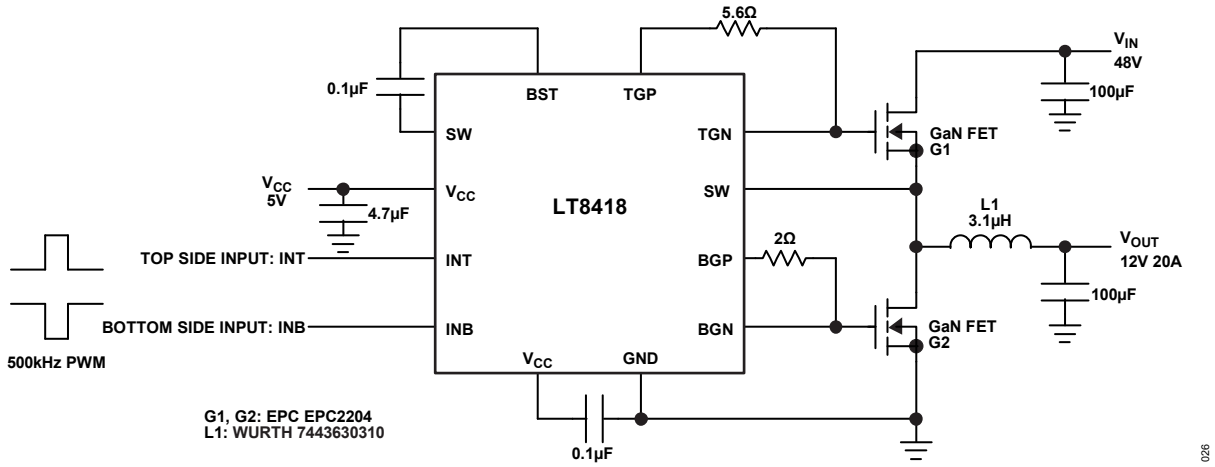


Figure 26. 48V Input, 12V 20A Output, 500kHz Buck Converter

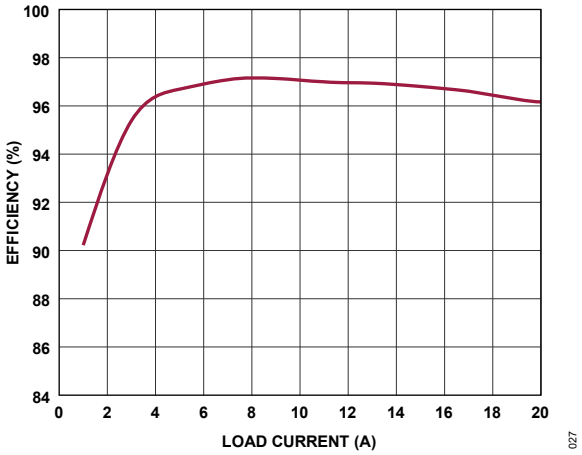


Figure 27. Efficiency vs. Load Current (with Heat Sink)

ORDERING GUIDE

Table 5. Ordering Guide

TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8418ACBZ-R7	8418	12-Ball WLCSP	-40°C to 125°C

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC7060	100V Half-Bridge Driver with Floating Grounds and Adjustable	Up to 100V supply rail, 6V ≤ V_{CC} ≤ 14V, programmable dead time control, tristate PWM input with enable pin.
LTC4449	High Speed Synchronous N-Channel MOSFET Driver	Up to 38V supply voltage, 4V ≤ V_{CC} ≤ 6.5V, 3.2A peak pull-up, 4.5A peak pull-down.
LTC4446	High Voltage Synchronous N-Channel MOSFET Driver without Shoot-Through Protection	Up to 100V supply voltage, 7.2V ≤ V_{CC} ≤ 13.5V, 2.5A/3A peak pull-up, 1.2Ω/0.55Ω peak pull-down.
LTC4444	High Voltage Synchronous N-Channel MOSFET Driver with Shoot-Through Protection	Up to 100V supply voltage, 7.2V ≤ V_{CC} ≤ 13.5V, 2.5A/3A peak pull-up, 1.2Ω/0.55Ω peak pull-down.