Self-Powered Single-Channel Isolated GaN FET Driver with Regulated Bipolar Output Drive

FEATURES AND BENEFITS

- Transformer isolation barrier
- Power-Thru integrated isolated bias
  - □ No need for high-side bootstrap
  - □ No need for external secondary-side bias
- AEC-Q100 Grade 2 qualification
- Bipolar drive output with adjustable regulated positive rail
- Built-in primary-side 3.3 V REF bias output
- 50 ns propagation delay
- Supply voltage 10.8 V < V_{DRV} < 13.2 V
- Undervoltage lockout on primary V_{DRV} and secondary V_{SEC}
- Enable pin with fast response
- Continuous ON capability—no need to recycle IN or recharge bootstrap capacitor
- CMTI > 100 V/ns dv/dt immunity
- Creepage distance 8.4 mm
- Safety regulatory approvals
  - □ 5 kV RMS V_{ISO} per UL 1577
  - □ 8 kV pk V_{IOTM} maximum transient isolation voltage
  - □ 1 kV pk maximum working isolation voltage

APPLICATIONS

- **AC-DC and DC-DC converters**: Totem-pole PFC, LLC half-/full-bridge, SR drive, multi-level converters, phase-shifted full-bridge
- **Automotive**: EV chargers, OBC
- **Industrial**: Data center, transportation, robotics, audio, motors
- **Clean Energy**: Micro-, string, and solar inverters

DESCRIPTION

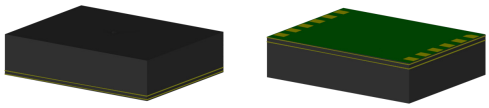
The AHV85111 isolated gate driver is optimized for driving GaN FETs in multiple applications and topologies. An isolated dual positive/negative output bias supply is integrated into the driver, eliminating the need for any external gate drive auxiliary bias supply or high-side bootstrap. The bipolar output rails, with adjustable and regulated positive rail, improves dv/dt immunity, greatly simplifies the system design, and reduces EMI through reduced total common-mode (CM) capacitance. It also allows the driving of a floating switch in any location in a switching power topology.

The driver has fast propagation delay and high peak source/sink capability to efficiently drive GaN FETs in high-frequency designs. High CMTI combined with isolated outputs for both bias power and drive make it ideal in applications requiring isolation, level-shifting, or ground separation for noise immunity.

The device is available in a compact low-profile surface-mount NH package. Several protection features are integrated, including undervoltage lockout on primary and secondary bias rails,

Continued on next page...

PACKAGE



10 mm × 7.66 mm × 2.41 mm
12-pin low-profile surface mount

Not to scale

TYPICAL APPLICATION

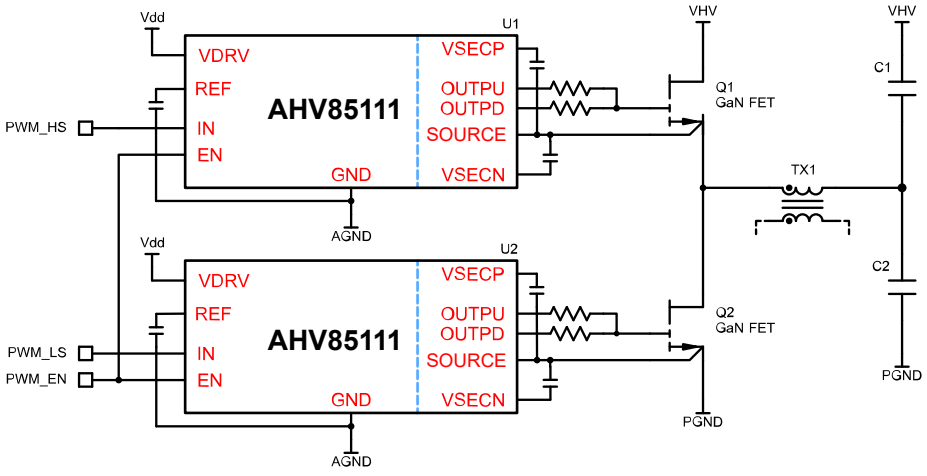


Figure 1: Typical AHV85111 half-bridge application—eliminates high-side bootstrap

DESCRIPTION (continued)

internal pull-down on IN pin and OUTPD pin, fast response enable input, overtemperature shutdown, and OUT pulse synchronization with first IN rising edge after enable (avoids asynchronous runt pulses).

SELECTION GUIDE

Part Number	Switch	# of Channels	Output	Qualification	Package	Tape & Reel Detail
AHV85111KNHTR	E-Mode GaN	1	Bipolar	AEC-Q100 Grade 2	10 mm × 7.66 mm × 2.41 mm 12-pin low-profile surface mount	13-inch 1500 pieces
AHV85111KNHLU	E-Mode GaN	1	Bipolar		10 mm × 7.66 mm × 2.41 mm 12-pin low-profile surface mount	13-inch 200 pieces

ABSOLUTE MAXIMUM RATINGS [1]

Characteristic	Symbol	Notes	Rating	Unit
Drive Supply Voltage	V_{DRV}	VDRV, wrt to GND	V_{GND} – 0.5 to 15	V
Input Data	V_{IN}	IN, wrt to GND	V_{GND} – 0.5 to 15	V
Enable	V_{EN}	EN, wrt to GND	V_{GND} – 0.5 to 15	V
Select	V_{SEL}	SEL to GND; internal use only	V_{GND} – 0.5 to 15	V
Reference Voltage	V_{REF}	3.3 V reference, wrt GND	V_{GND} – 0.5 to 4	V
Feedback Voltage	V_{FB}	1.225 V feedback, wrt SOURCE	V_{SECN} – 0.5 to 15	V
Output Drive Pull-Up	V_{OUTPU}	OUTPU to SOURCE	V_{SECN} – 0.5 to 15	V
Output Drive Pull-Down	V_{OUTPD}	OUTPD to SOURCE	V_{SECN} – 0.5 to 15	V
Isolated Bias Supply	$V_{SECP} – V_{SECN}$	Total rail	–0.5 to 15	V
Junction Temperature	T_J		–40 to 150	°C
Storage Temperature	T_{STG}		–40 to 150	°C

[1] Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD RATINGS

Characteristic	Symbol	Test Conditions	Value	Unit
Human Body Model	V_{HBM}		±2	kV
Charged Device Model	V_{CDM}		±500	V

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions [1]	Value	Unit
Junction-to-Ambient Thermal Resistance	$R_{\theta JA}$	4-layer PCB based on JEDEC standard, with no thermal vias	102	°C/W

[1] Additional thermal information available on the Allegro website.

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RECOMMENDED OPERATING CONDITIONS: Valid at –40°C < T_J < 125°C, 10.8 V < V_{DRV} < 13.2 V, $C_{SEC(NET)}$ = 47 nF, C_{OUT} = 1 nF, unless otherwise stated. [1][2]

Characteristics	Symbol	Test Conditions	Min.	Typ. [3]	Max.	Unit
SUPPLY VOLTAGE PINS						
Drive Supply Voltage	V_{DRV}		10.8	–	13.2	V
INPUT PINS						
Input Data	V_{IN}		V_{GND}	–	V_{DRV}	V
Enable Active High	V_{EN}		V_{GND}	–	V_{DRV}	V
Select	V_{SEL}	Internal use only	V_{GND}	–	V_{DRV}	V
OUTPUT PINS						
Isolated Supply Referenced to SOURCE	V_{SECP}		–	–	6	V
	V_{SECN}		–6	–	–	V
VSEC Pin Capacitor CSEC [3]	C_{SECP}	External capacitance connected between VSECP and SOURCE pins; external C_{OUT} = 1 nF	22 [4]	100	300 [5]	nF
	C_{SECN}	External capacitance connected between VSECN and SOURCE pins; external C_{OUT} = 1 nF	22 [4]	100	300 [5]	nF
	C_{SECPN}	External capacitance connected between VSECP and VSECN pins; external C_{OUT} = 1 nF	22 [4]	100	300 [5]	nF
Reference	V_{REF}	3V3 rail decoupling capacitor pin	V_{GND}	–	3.3	V
REF Pin Capacitor CREF	C_{REF}	External capacitor connected between REF and GND pin	100	–	1000	nF
Junction Temperature	T_J		–40	–	125	°C

[1] $C_{SEC(NET)}$ is the net equivalent of C_{SECP} in series with C_{SECN}, i.e., (C_{SECP} × C_{SECN}) / (C_{SECP} + C_{SECN}).
[2] Not tested in production; guaranteed by design and bench characterization.
[3] Typical values should be chosen to match the ratio of V_{SECP} to V_{SECN}.
[4] Smaller C_{SEC} values than the recommended typical value can give higher voltage ripple on C_{SEC}.
[5] Larger C_{SEC} values will mean longer startup times.

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ISOLATION CHARACTERISTICS

Characteristic	Symbol	Test Conditions	Value	Unit
General				
External Clearance	CLR	Shortest terminal-to-terminal distance through air	8.4	mm
External Creepage	CPG	Shortest terminal-to-terminal distance across the package surface	8.4	mm
Distance Through Insulation	DTI	Internal insulation thickness	200	µm
Comparative Tracking Index	CTI	According to IEC 60112	400 to 599	V
Material Group	MG	According to IEC 60664-1	II	–
Overvoltage Category		Per IEC 60664-1 at 600 V line voltage	I–IV	–
Maximum Reinforced Working Voltage [1][2]	V_{IORM}	Maximum approved working voltage for basic insulation according to UL 62368-1:2014 (Edition 2)	1000	V_{PK} V_{DC}
			700	V_{RMS}
Maximum Impulse Voltage	V_{IMP}	Tested to UL 62368 Table D1 circuit 3	8000	V_{PK}
Maximum Transient Isolation Voltage	V_{IOTM}	60 second rating, 100% production test, 1 second at 6000 V_{RMS}	7000	V_{PK}
Maximum Surge Isolation Voltage	V_{IOSM}	Tested with to UL 62368 Table D1 circuit 3 in oil at 1.6 × rating	8000	V_{PK}
Partial Discharge	q_{PD}	Method B1: At routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, $t_{ini} = 1$ s; $V_m = 1.875 \times V_{IORM}$, $t_m = 1$ s	≤5	pC
Barrier Capacitance, Input to Output	C_{IO}	$V_{IO} = 0.5 \times \sin(2\pi ft)$, f = 1 MHz	<1	pF
Insulation Resistance, Input to Output	R_{IO}		$>10^{12}$	Ω
Climatic Classification			40/105/21	–
UL1577				
Withstand Isolation Voltage	V_{ISO}	60 second rating, 100% production test, 1 second at 6000 V_{RMS}	5000	V_{RMS}

[1] Pending certification to UL 62368 Edition 2.
[2] Working Voltage evaluated for use at Pollution Degree 2 and Material Group II.

MSL RATING

Device	MSL Rating	Maximum Floor Life at Standard Ambient (30°C/60%RH)	Maximum Peak Reflow Temperature	Pre-Reflow Bake Requirement
AHV85111	MSL-3	168 hours	260°C	Per JEDEC J-STD-033C

Per JEDEC J-STD-033C, the AHV85111 devices are rated MSL3. This MSL3 rating means that once the sealed production packaging is opened, the devices must be reflowed within a “floor-life” of 168 hours (1 week) if they are stored in under standard ambient conditions (30°C and 60% relative humidity (RH)).
The peak reflow temperature should not exceed the maximum specified in MSL Rating table.
If the devices are exposed to the standard ambient for more than 168 hours, they must be baked before reflow to remove any excess moisture in the package and prevent damage during reflow soldering. The required bake times and temperatures are detailed in IPC/JEDEC standard J-STD-033C.
If the devices are exposed to higher temperature and/or RH compared to the standard ambient of 30°C/60% RH, the floor-life will be shortened due to the increased rate of moisture absorption. If the actual ambient conditions exceed the standard ambient, it is recommended that parts should always be baked per IEC/JEDEC J-STD-033C before reflow as a precaution to avoid potential device damage during reflow soldering.

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FUNCTIONAL BLOCK DIAGRAM

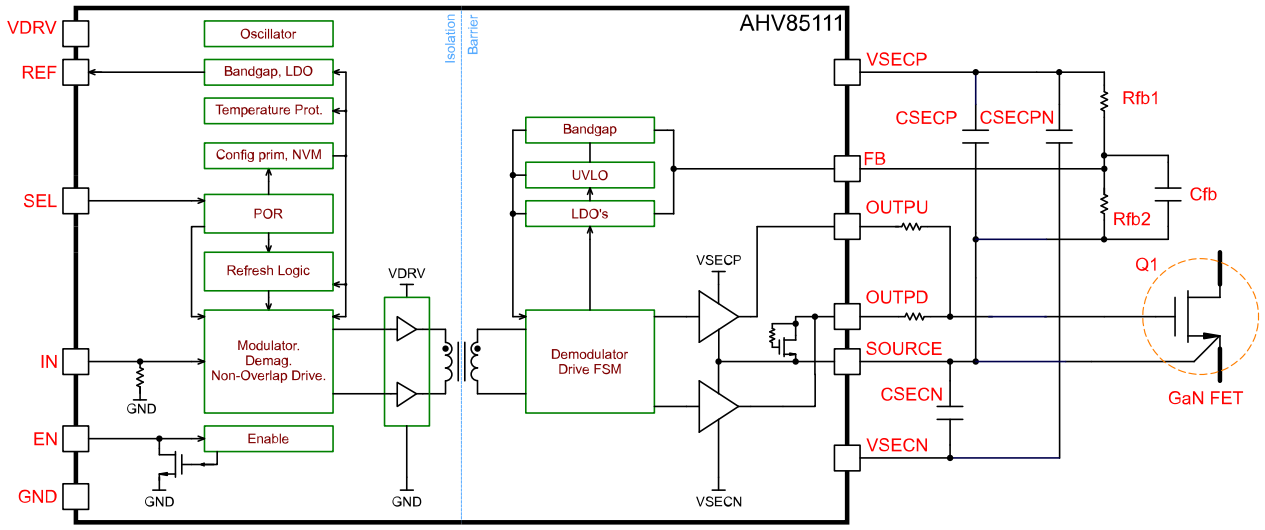
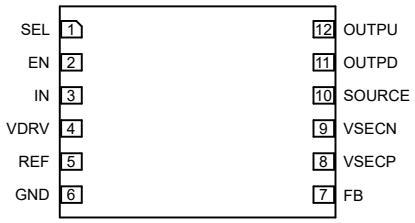


Figure 2: AHV85111 Block Diagram

PINOUT DIAGRAM AND TERMINAL LIST TABLE



Package NH Pinout (Top View)

Terminal List Table

Number	Name	Function
1	SEL	Internal use only—this pin must be tied high to VDRV.
2	EN	Bidirectional enable pin; see Figure 3.
3	IN	PWM input; see Electrical Characteristics table.
4	VDRV	Ground referenced voltage supply; this voltage indirectly sets the total output-side bias rail amplitude.
5	REF	Connection for external decoupling capacitor for internal REF rail; can be used to power external low current loads up to 2 mA.
6	GND	Ground pin for input/primary side.
7	FB	Feedback pin to adjust the regulated V_{SECP} level.
8	VSECP	Positive regulated isolated gate drive bias rail; external decoupling capacitor referenced to SOURCE.
9	VSECN	Negative unregulated isolated gate drive bias rail; external decoupling capacitor referenced to SOURCE.
10	SOURCE	Isolated output return pin.
11	OUTPD	Isolated output drive pull-down pin; see Electrical Characteristics table.
12	OUTPU	Isolated output drive pull-up pin; see Electrical Characteristics table.

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ELECTRICAL CHARACTERISTICS: Valid at –40°C < T_J < 125°C, 10.8 V < V_{DRV} < 13.2 V, $C_{SEC(NET)}$ = 47 nF, C_{OUT} = 1 nF, unless otherwise stated [1]

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY CURRENTS						
VDRV Disable Current	I_{DRV_DIS}	V_{IN} = 0, EN = 0	–	1	1.3	mA
VDRV Quiescent Current	I_{DRV_Q}	V_{IN} = 0, EN = 1	–	2	3.4	mA
VDRV Switching Current	I_{DRV_SW}	f_S = 120 kHz, EN = 1	–	9.5	13	mA
INPUT PINS						
Input Data – Logic Low	$V_{IN(L)}$		–	–	0.8	V
Input Data – Logic High	$V_{IN(H)}$		2.0	–	–	V
Input Data Hysteresis	$V_{IN(HYS)}$		–	300	–	mV
Enable Active High – Logic Low	$V_{EN(L)}$		–	–	0.8	V
Enable Active High – Logic High	$V_{EN(H)}$		2.0	–	–	V
Enable Active High – Hysteresis	$V_{EN(HYS)}$		–	400	–	mV
Internal On-Chip Pull-Down Resistance On IN Pin	R_{IN}	T_A = 25°C	–	300	–	kΩ
FB Pin Voltage [2]	V_{FB}	FB pin reference wrt VSECP	1.1	1.225	1.35	V
OUTPUT PINS						
OUTPU Pull-Up Resistance	R_{PU}		1.5	2.8	3.5	Ω
OUTPD Pull-Down Resistance	R_{PD}		0.5	1.0	1.7	Ω
Reference Voltage	V_{REF}	Regulation level	–	3.30	–	V
Reference Current	I_{REF}	Available source current	–	2	–	mA
High Level Source Current [2]	I_{SOURCE}	V_{SEC} = 5.4 V, R_{ext_pu} = 0 Ω, C_{OUT} = 10 nF	–	2	–	A
Low Level Sink Current [2]	I_{SINK}	V_{SEC} = 5.4 V, R_{ext_pd} = 0 Ω, C_{OUT} = 10 nF	–	4	–	A
PRIMARY UNDERVOLTAGE LOCKOUT						
VDRV UV Threshold, Rising [3]	V_{DRV_UVH}		9.5	10.0	10.5	V
VDRV UV Threshold, Falling [3]	V_{DRV_UVL}		8.8	9.3	9.8	V
VDRV UV Hysteresis	V_{DRV_UVHYS}		0.5	0.7	0.9	V
SECONDARY UNDERVOLTAGE LOCKOUT						
VSEC UV Threshold, Rising	V_{SEC_UVH}		4	4.4	4.9	V
VSEC UV Threshold, Falling	V_{SEC_UVL}		3.7	4.1	4.5	V
VSEC UV Hysteresis	V_{SEC_UVHYS}		0.2	0.3	0.4	V
OVERTEMPERATURE PROTECTION						
Overtemperature Threshold, Rising	T_{SD}		150	155	160	°C
Overtemperature Hysteresis	$T_{SD(HYS)}$		–	30	–	°C

[1] Not cold tested in production (–40°C); guaranteed by design and bench characterization.
[2] Not tested in production; guaranteed by design and bench characterization.
[3] When V_{DRV} is below the UVLO threshold, the driver output is actively held low.

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SWITCHING CHARACTERISTICS: Valid at –40°C < T_J < 125°C, 10.8 V < V_{DRV} < 13.2 V, $C_{SEC(NET)}$ = 47 nF, C_{OUT} = 1 nF, unless otherwise stated [1]

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
PROPAGATION TIMES						
Propagation Delay, High To Low	t_{PHL}	R_{ext_pu} = 2 Ω	–	50	100	ns
Propagation Delay, Low To High	t_{PLH}	R_{ext_pd} = 2 Ω	–	50	100	ns
RISE AND FALL TIMES						
Rise Time	t_r	R_{ext_pu} = 0 Ω, 20-80%	–	9	15	ns
Fall Time	t_f	R_{ext_pd} = 0 Ω, 20-80%	–	7	15	ns
Shortest ON Time Allowable [2]	$t_{pw(on)}$	The ON time should never be less than specified minimum	100	–	–	ns
Shortest OFF Time Allowable [2]	$t_{pw(off)}$	The OFF time should never be less than specified minimum	100	–	–	ns
STARTUP TIME						
Wait Time Before First IN Edge is Delivered After V_{DRV} is Within Specification	t_{START}		–	–	250	µs

[1] Not cold tested in production (–40°C); guaranteed by design and bench characterization.
[2] Not tested in production; guaranteed by design and bench characterization.

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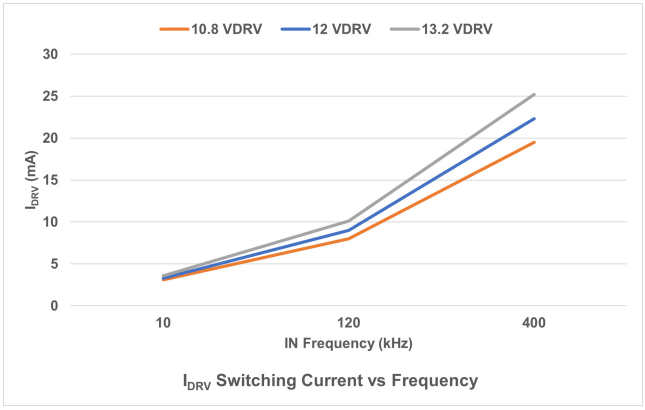
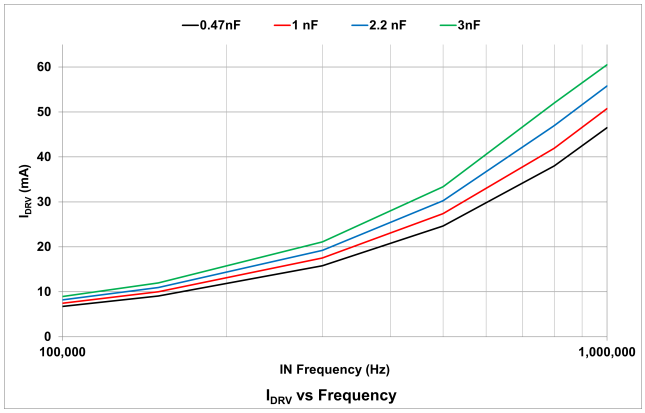
Typical IC Characteristics Curves



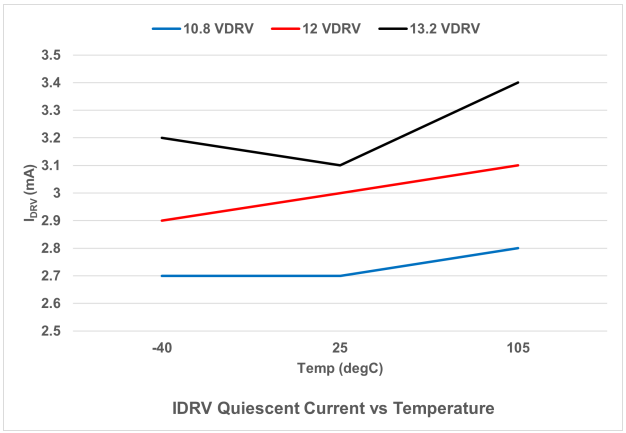
I_{DRV} Switching Current vs Frequency

C_{OUT} = 1 nF, $C_{SEC(NET)}$ = 47 nF



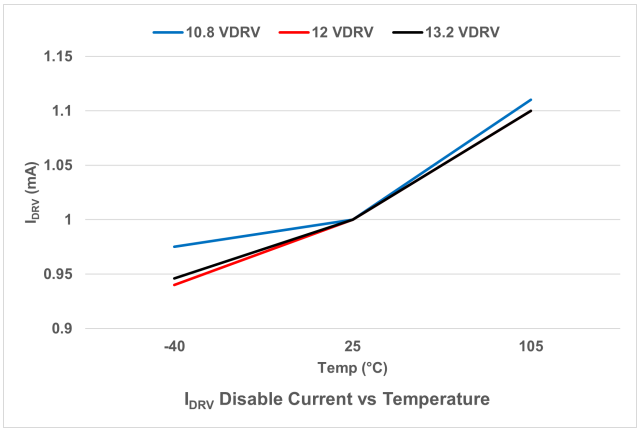
I_{DRV} vs Frequency

V_{SECP} = 5.4 V, $C_{SEC(NET)}$ = 47 nF, V_{DRV} = 12 V, T_A = 25°C



IDRV Quiescent Current vs Temperature

IN = 0, EN = 1



I_{DRV} Disable Current vs Temperature

IN = 0, EN = 0

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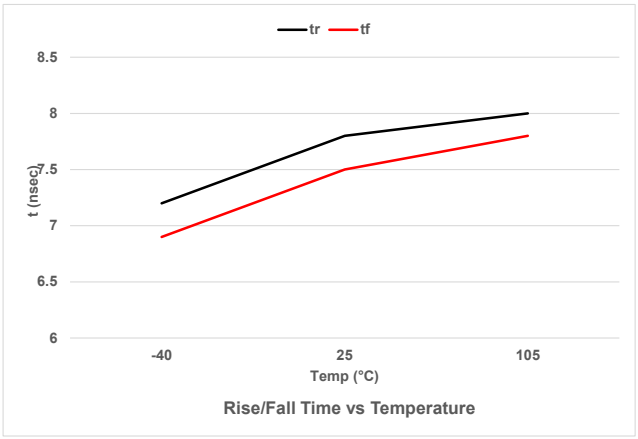
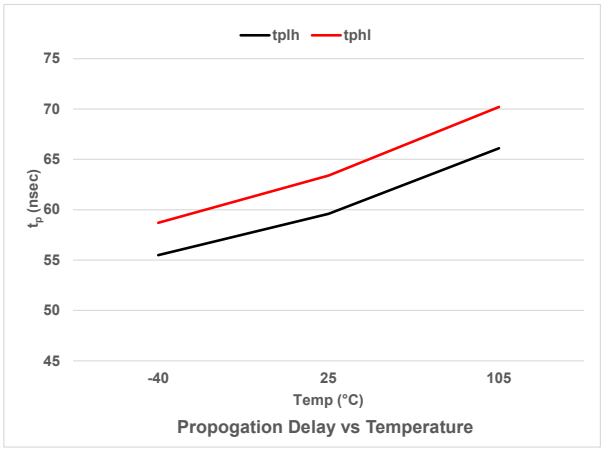
Typical IC Characteristics Curves, continued



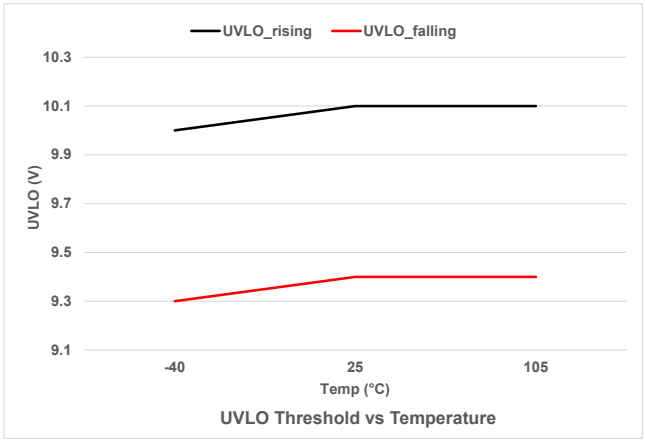
Rise/Fall Time vs Temperature

IN = PWM 150 kHz, V_{DRV} = 12 V, C_{OUT} = 1 nF



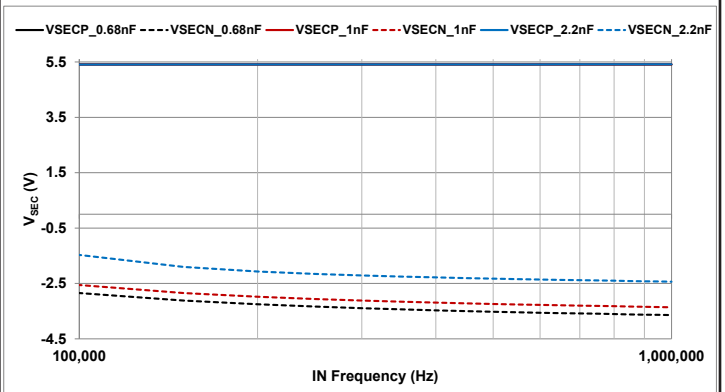
Propogation Delay vs Temperature

IN = PWM 150 kHz, V_{DRV} = 12 V, C_{OUT} = 1 nF



UVLO Threshold vs Temperature

IN = PWM 150 kHz, V_{DRV} = 12 V, C_{OUT} = 1 nF



V_{SEC} vs Frequency

$C_{SEC(NET)}$ = 47 nF, V_{DRV} = 12 V, V_{SECP} = 5.4 V

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FUNCTIONAL DESCRIPTION

The AHV85111 is a self-powered isolated gate driver. Allegro's patented Power-Thru technology allows the transfer of both PWM signal and gate power across a single transformer-based isolation barrier. This eliminates the need to provide an isolated bias supply to power the isolated side of the driver, greatly simplifying the system design. Only decoupling capacitors and programming resistors are required on the isolated side to generate the bipolar positive and negative gate drive rails V_{SECP} and V_{SECN}.

The AHV85111 driver has been optimized for driving the gate of typical Schottky-gate Enhancement-mode (E-mode) GaN FETs, such as those available from GaN Systems, Innoscience, ST, Nexperia, GaN Power International, Taiwan Semiconductor, Rohm and others. An online FET selection tool can be downloaded from the Allegro website to assist system designers, to check compatibility of various FET devices with the driver.

The isolated V_{SECP} positive bias rail is locally regulated, using an external resistor divider connect to the FB pin. The balance of the secondary bias voltage becomes the unregulated negative rail V_{SECN}. The V_{SECP} rail regulates quite well versus PWM switching frequency f_{SW} at the IN pin, for a given fixed V_{DRV} level, and for a fixed load C_{OUT} at the OUTx drive pins—the load presented by the gate of the GaN FET being driven as long as the $Q_{G(TOT)}$ versus frequency recommended operating area (ROA) curve recommendations are adhered to; see Figure 10 ROA curve. This is because the charge delivered per PWM cycle naturally increases in tandem with the charge consumed by the FET gate, so there is a good charge balance across a wide frequency range.

However, the V_{SEC} rails do vary with effective loading of the gate of FET being driven; as V_{SEC} levels fall, more charge is available to be delivered to the secondary side, while the charge consumed by the FET gate decreases with falling V_{SEC} levels. Therefore, the V_{SEC} rails will droop as far as needed until the charge delivered matches the charge consumed. For this reason, it is also very important to minimize the amount of charge diverted into any external loads. For example, a very low bias power external circuit can be powered using V_{SEC}, but the consumption should be minimal, to minimize the charge diverted away from the gate of FET. Similarly, if a gate-source pull-down resistor is desired on the load FET (to prevent false turn-on in the case of a manufacturing fault, such as an open-circuit gate turn-on resistor), the resistor value should be as large as possible. The recommended value is 100 kΩ, to minimize DC loading on V_{SEC}. Since DC load current converts to equivalent charge as $Q = I \times t$, DC loading effects will become significantly more pronounced at lower PWM frequency, as the time duration t gets longer. In particular, it should be noted that the driver will attempt to regulate the positive rail V_{SECP} as priority, with the balance of charge diverted to create the negative rail V_{SECN}. In certain situations, such as low V_{DRV}, high load FET Q_G, excessive external loading of V_{SEC}, high load FET gate leakage current I_{GSS}, or a combination of these, there may be be insufficient charge available to create a sufficient or even any negative V_{SECN}. However, the ROA curve in Figure 10 indicates the supported operating range of Q_G versus PWM frequency that maintains a minimum V_{SECN} negative rail of –1 V or better.

Since there is just a single magnetic isolation barrier to transfer both PWM signal and gate power, this also greatly reduces the total parasitic capacitance between the primary-side and isolated-side, to typically < 1 pF total for both signal and power channels. This is much less than the typical total parasitic capacitance value for a solution using a conventional isolated gate driver with a separate isolated DC-DC bias supply, where the capacitance contribution from the DC-DC isolation transformer could be as high as 10 pF or more. This reduction in isolation capacitance greatly reduces the level of noise injected back into the low-voltage control circuit by the high-voltage and high dv/dt switching nodes in the power stage half-bridge legs, reduces system level Common-Mode (CM) EMI, and saves on power loss that occurs through repetitive charging and discharging of this parasitic capacitance between the high bus voltage level and ground.

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APPLICATIONS INFORMATION

Bidirectional Enable/Disable EN Pin

EN is a bidirectional open-drain pin which requires an external resistor pull-up to the VDRV pin. The EN pin allows for management of startup and fault conditions between the PWM controller and multiple drivers, through use of a shared enable EN line. Either the PWM controller or the driver can pull the EN pin low via the EN bus, as shown in Figure 3. When the EN pin is pulled low (either externally or internally), this forces the driver into a mode where the IN pin signal is ignored, and the OUT pins are disabled and actively pulled low. When the EN pin goes high, normal driver operation is enabled.

In the event of an internal driver fault condition, such as UVLO or normal startup delay, the EN pin is actively pulled low internally by the driver. This driver pull-down can be detected by the PWM controller and used as a flag for an external fault, or to flag that the driver is ready, and PWM can commence.

The shared EN line is typically wired-AND with the controller EN pin, as shown in Figure 3. Multiple drivers can be connected in parallel with the controller on the shared EN line, such that all connected drivers will hold the EN line low until all drivers and the PWM controller have released their own EN pin, ensuring smooth safe startup of the system.

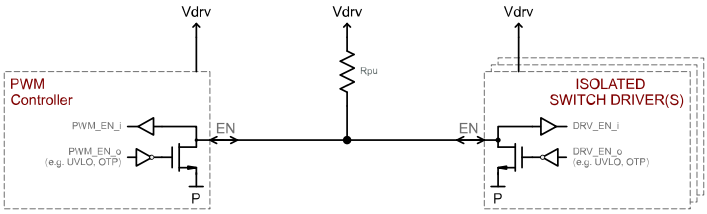

Figure 3: Example Wired-AND connection between driver and controller

Note that the EN pin has no internal pull-up or pull-down—the open-drain configuration relies on an external pull-up resistor for normal operation. Similarly, the EN pin must be actively pulled low externally to disable the driver. The EN pin should never be left floating or connected directly to VDRV or any other system bias voltage; a pull-up resistor must be used. The EN pin should be connected to VDRV through a pull-up resistor in a recommended range of 10 to 100 kΩ. The EN pin dv/dt when being pulled low or high should be at least 0.1 V/µs.

When the EN pin is pulled low, the driver output is disabled, and pulls down the OUTPD pin, regardless of the IN pin level (high or low). The driver goes to a low-power standby mode, and the isolated VSECP and VSEPN bias rails are allowed to discharge. The rate of decay of V_{SECP} and V_{SECN} depends on the value of the C_{SECP} and C_{SECN} capacitors.

When the EN pin is subsequently pulled high, the driver will re-enable, and the isolated VSEC bias rail will start to recharge. Even if the IN pin is connected to a PWM signal, the OUT pins will not respond until the VSECP rail exceeds the secondary UVLO threshold. The rate of rise of V_{SECP} depends on the PWM frequency at the IN pin. Worst-case slowest rise time is when IN = 0, using the slowest internal energy transfer mode. In this mode, the rise time will be approximately 250 µs for equivalent C_{SEC} of 47 nF to charge from zero to the rising UVLO threshold.

Startup and Shutdown Procedure

Any PWM signal applied to IN must remain low until V_{DRV} > UV threshold, to avoid parasitic charging of the V_{DRV} rail through the IN pin internal ESD structures. After V_{DRV} exceeds the UV rising threshold, a startup time delay t_{START} is required to allow all internal circuits to initialize and stabilize. During t_{START}, any IN signal inputs are ignored. EN internal pull-down will remain active during t_{START}, and will release (i.e., go open-drain) only when V_{DRV} has reached its UVLO voltage level, all on-chip voltages are stabilized, there is no overtemperature fault, and the internal t_{START} timer has elapsed. Thus, the EN pin can be used via a shared EN line to flag when t_{START} has elapsed, and the driver is ready to respond to PWM signals at the IN pin, as outlined above.

Typical startup waveforms are shown in Figure 4.

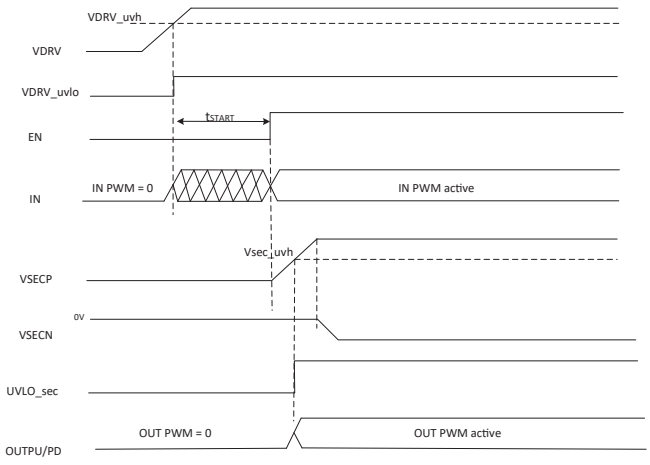

Figure 4: AHV85111 Startup Mechanism

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Once V_{DRV} drops below UVLO falling threshold, the enable signal is pulled down and the driver output shuts down. The rate of decay of V_{SEC} is determined by the VSEC capacitance as shown in Figure 5.

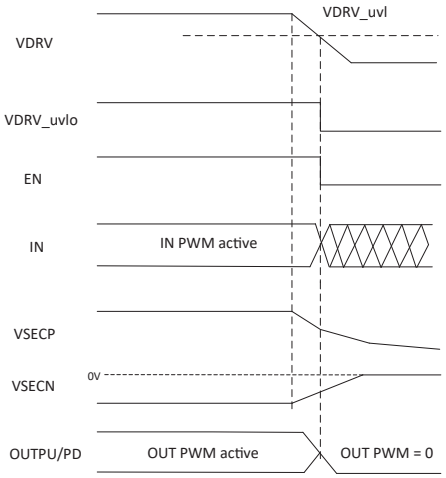

Figure 5: Shutdown Mechanism

Refresh Pulse Mechanism

In cases when IN-PWM signal frequency is low or when IN is set to continuous 1 or 0, in order to prevent VSEC voltage decay, the AHV85111 implements an internal clock of 12 µs ($t_{REFRESH}$). When $t_{REFRESH}$ elapses, the driver recharges VSEC rail to maintain output voltage. This condition persists until IN changes state as shown in Figure 6.

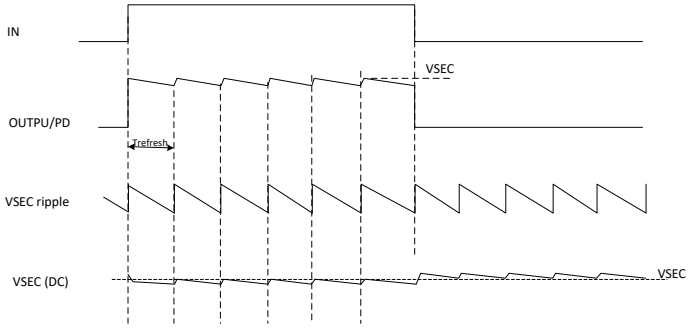

Figure 6: AHV85111 Refresh Mechanism

VSECP Voltage Setpoint

As shown in Figure 7, the feedback (FB) pin is used in conjunction with two resistors R_{FB1} and R_{FB2} to set the regulated output voltage between VSECP and SOURCE pins.

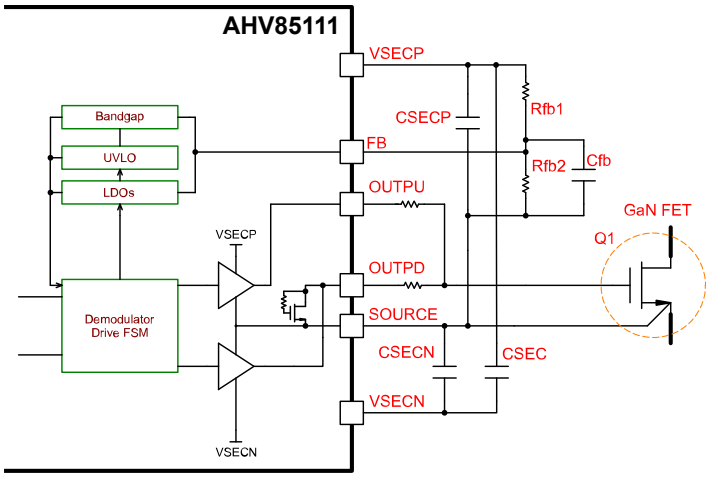

Figure 7: Rfb1 and Rfb2 used to set the desired VSECP-to-SOURCE positive bias rail regulation level

Decoupling capacitors CSECP and CSECN are connected from VSECP to SOURCE and VSECN to SOURCE respectively, to supply the peak gate charge and discharge currents. In addition, a capacitor CSECPN should be connected directly from VSECP to VSECN to ensure stability of the internal LDO—a value of 100 nF is recommended. A small noise filter cap is also recommended to be placed from FB to SOURCE to improve V_{SECP} regulation robustness to noise. Typically 100 pF is recommended for R_{FB2} = 100 kΩ

Table 1 shows resistance values (nearest E96 standard value) and associated outputs for an input voltage of V_{DRV} = 12 V, for typical V_{SECP} target setpoints. For other required V_{SECP} levels, Equation 1 can be used to calculate the required value for R_{FB1}, assuming that the V_{DRV} level is high enough to allow V_{SECP} to regulate.

Table 1: V_{SECP} – V_{SOURCE} vs. Rfb1 value; Rfb2 = 100 kΩ, V_{DRV} = 12 V

V_{SECP} – V_{SOURCE} (V)	Rfb1 (kΩ)
5.0	32.4
5.4	29.4
6.0	25.5

Equation 1:

$$R_{FB1} = \frac{R_{FB2}}{\frac{V_{SESCP}}{V_{FB}} - 1}$$

The positive output voltage is regulated on-chip with respect to the SOURCE pin, at the level set by choice of R_{FB2}, assuming that the V_{DRV} level is sufficient to allow regulation at the target

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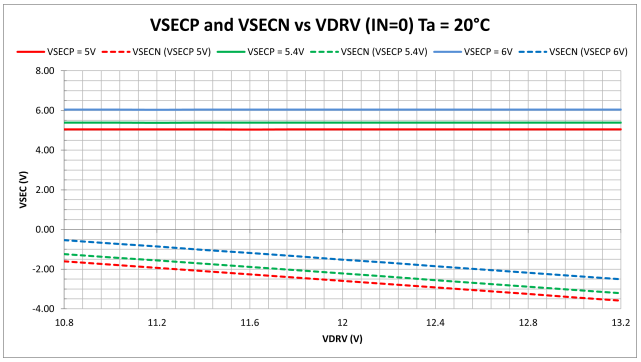
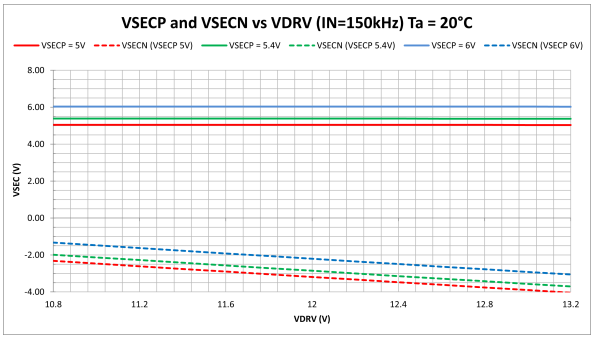
V_{SECP} level. The remaining voltage overhead, unregulated, is the negative voltage drive (stored on CSECN).

Figure 8 shows curves of the typical positive output voltage range as a function of the input voltage V_{DRV}. Note that if the V_{DRV} level is too low to allow V_{SECP} to achieve regulation, V_{SECN} will be clamped to zero. Once the V_{DRV} level is sufficient to allow V_{SECP} to regulate, and excess secondary bias voltage will then appear on the negative rail V_{SECN}.



(a) IN = 0



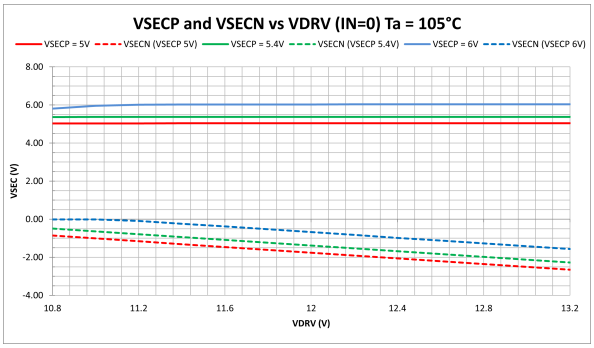
(b) IN = 150 kHz / 50% Duty Cycle, C_{OUT} = 1 nF

Figure 8: Positive and negative output voltage vs. input V_{DRV}

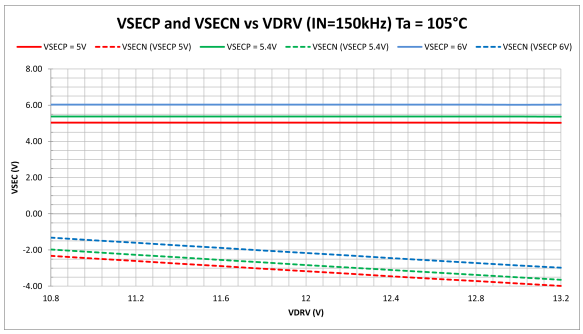
Effect of Temperature on V_{SEC}

At high operating ambient temperatures and low input PWM frequencies below 100 kHz, the total secondary-side bias rail, $V_{SECP} - V_{SECN}$, is reduced. Figure 9a shows that for minimum input supply voltage, V_{DRV}, and maximum recommended 6 V output set point, V_{SECP}, the total secondary-side bias voltage is not sufficient to maintain regulation of V_{SECP} and V_{SECN} is subsequently zero volts. Increasing V_{DRV} provides more secondary bias voltage and regulation is achieved.

At higher input frequencies, above 100 kHz, there is no reduction in $V_{SECP} - V_{SECN}$ at maximum ambient temperature. Figure 9b shows there is sufficient secondary-side bias voltage to maintain regulation across the full input voltage range.



(a) IN = 0



(b) IN = 150 kHz / 50% Duty Cycle, C_{OUT} = 1 nF

Figure 9: Effect of high ambient temperature on VSECP and VSECN

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Operating Frequency and Thermal Derating

The maximum recommended PWM frequency is 1 MHz. However, the device internal dissipation, application PCB layout, and ambient temperature must also be taken into account to ensure that the internal recommended $T_{J(MAX)}$ of 125°C is not exceeded.

Figure 10 shows the recommended operating area curve of $Q_{G(TOT)}$ versus PWM frequency that will maintain a negative rail V_{SECN} of at least –1 V at nominal V_{DRV} of 12 V. Operating further below this curve will result in even more negative off-state voltage V_{SECN}. The AHV85111 can be operated above the curve of Figure 10, but the negative rail V_{SECN} will be limited, and in some cases can be close to zero.

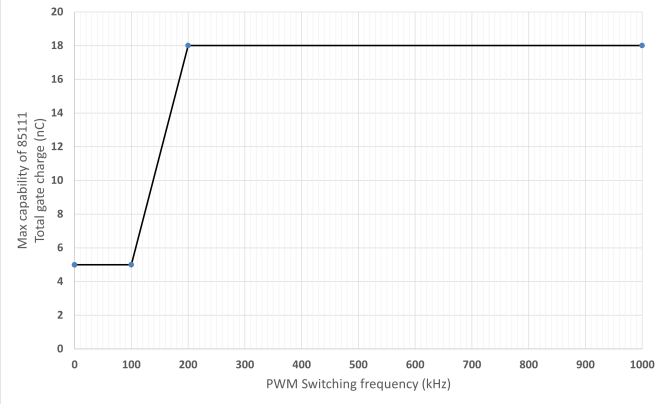

Figure 10: Recommended Operating Area Curve Max $Q_{G(TOT)}$ as a function of PWM Frequency f_{SW}, V_{DRV} = 12 V

The thermal derating curves of Figure 11 are based on the device thermal performance using JEDEC-standard PCB footprint and PCB design (layer count and size of copper planes for heatsinking). The actual thermal performance in the end system design should always be verified, since every system is different in terms of exact PCB design and ambient airflow from natural or forced convection.

Because of the required creepage distance under the IC package to meet system safety requirements, it is not allowed to put a large copper plane under the IC for heatsinking purposes. Instead, it is recommended that the primary-side GND pins and secondary-side SOURCE pins be connected to appropriate ground planes on each side, and to maximize the size of these planes to maximize thermal performance. Multiple thermal vias to larger inner-layer ground planes can also help improve thermal performance.

The effective gate capacitance C_{OUT} that loads the OUTx drive pins can be estimated from the GaN FET datasheet. The FET total charge $Q_{G(TOT)}$ is usually specified in nC, for a given V_{GS} voltage swing.

$$C_{OUT} = \frac{Q_{G(TOT)}}{V_{GS}}$$

Knowing the value of C_{OUT}, the expected level of the secondary supply rail V_{SEC} can be estimated from V_{SEC} vs. Frequency from Typical IC Characteristics curve. From C_{OUT}, V_{SEC} and the required PWM frequency F_{SW}, the total gate power can be calculated as follows:

$$P_{GATE} = f_{SW} \times C_{OUT} \times V_{SEC}^2$$

Note that V_{SEC} in this case is the full V_{GS} voltage swing from posirtive to negative, i.e., $V_{GS} = V_{SECP} - V_{SECN}$. In practice, the system design will likely use external gate resistors to control the FET turn-on and turn-off speed. The gate-drive power consumption P_{GATE} will be dissipated by the internal driver FET resistances and the external resistors, apportioned by the ratio of the resistances. The larger the value of the external resistors, the higher the power dissipation in those resistors, and the lower the dissipation in the internal driver resistances. To simplify the thermal estimates, and to add in design margin, it is assumed that all of the P_{GATE} power is dissipated inside the driver package.

The internal driver stage MOSFETs will consume drive power, and they will have switching losses, so there is an efficiency factor that needs to be accounted for when estimating the internal power consumed when delivering the P_{GATE} power.

Finally, the internal isolated bias power stage consumes power. As well as the IC quiescent power consumption, there are also drive, conduction and switching losses in the internal power FETs that drive and rectify the energy transfer through the internal isolation transformer, as well as the conduction and core losses of the transformer. These losses scale approximately linearly with PWM frequency.

Combining all of these loss mechanisms, the total package power dissipation (in mW) can be estimated using the following empirical formula, where f_{SW} is in kHz and P_{GATE} is in mW. This assumes a fixed V_{DRV} level of 12 V.

$$P_{DISS} = 0.67 \times f_{SW} + \frac{P_{GATE}}{0.7}$$

Using the standard JEDEC thermal impedances in the thermal characteristics table, the maximum allowed ambient temperature T_A can be estimated from:

$$T_{A(MAX)} = T_{J(MAX)} - P_{DISS} \times R_{TH(JA)}$$

Alternatively, Figure 11 can be used to graphically estimate the allowable $T_{A(MAX)}$ as a function of F_{SW} and C_{OUT}. The online FET selection tool can also be used to estimate expected driver temperature rise over ambient, and maximum allowed T_A.

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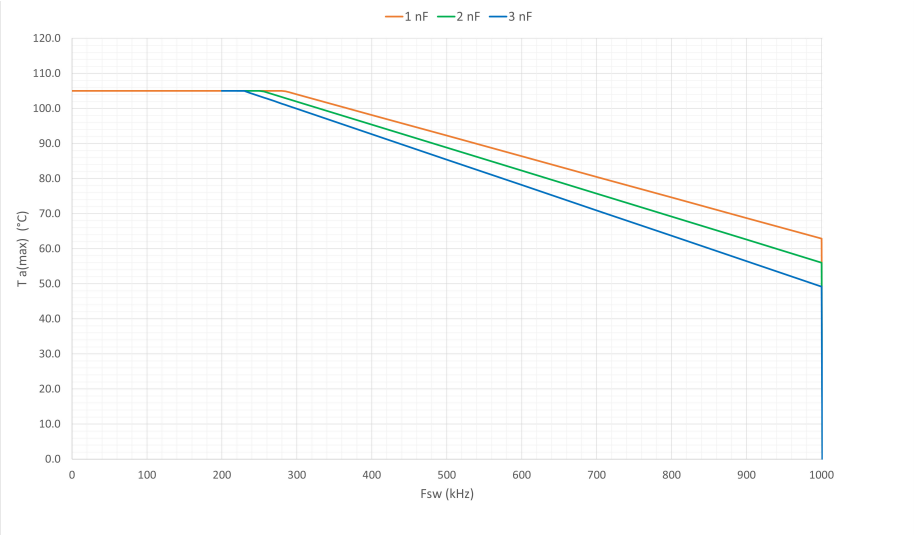

Figure 11: AHV85111 thermal derating curve as a function of load capacitance C_{OUT} and PWM frequency f_{SW}

WORKED EXAMPLE

What follows is an example calculation, based on the APEK85111KNH-02-T-MH evaluation board. Assume the target switching frequency is 400 kHz, and the required maximum ambient temperature is 85°C.

The FET used on the board is a GS-66508-B from GaN Systems. From the GaN datasheet, the $Q_{G(TOT)}$ is specified at 6.1 nC at 6 V V_{GS} swing. Therefore, the equivalent C_{OUT} is:

$$C_{OUT} = \frac{6.1}{6} = 1.0\ nF$$

Assuming V_{SECP} is set to 5.4 V, from Figure 8b, for this value of C_{OUT}, the total V_{SEC} level can be estimated as approximately 8.4 V (V_{SECP} = 5.4 V, V_{SECN} = −2.8 V). Note that the full V_{GS} swing must be used to estimate the gate power dissipation.

$$P_{GATE} = 400\ kHz \times 1.0\ nF \times 8.4^2 = 28.2\ mW$$

From this, the total package power dissipation can be estimated:

$$P_{DISS} = 0.67 \times 400 + \frac{28.2}{0.7} = 272\ mW$$

Now the maximum allowed ambient temperature can be verified to ensure that it meets the system requirement:

$$T_{A(MAX)} = 125 - 0.272 \times 102 = 97.3°C$$

This equation shows that the design can meet the required maximum ambient temperature. However, as noted above, this uses $R_{TH(JA)}$ estimates based on standardized JEDEC footprints and PCB layouts; the actual thermal performance must be verified in each individual application.

The maximum allowed ambient temperature can also be readily estimated from the curves in Figure 11. Using F_{SW} of 400 kHz, and C_{OUT} of approximately 1.0 nF, the estimate $T_{A(MAX)}$ is approximately 98°C, which is close the calculated result using the empirical loss estimation.

V_{DRV} and C_{SEC} Design Guidelines

The output gate drive amplitude is always less than V_{DRV} due to internal impedances and voltage drops.

The total secondary-side bias rail, $V_{SECP} - V_{SECN}$, depends on the V_{DRV} level applied on the primary, and effective C_{LOAD} presented by the GaN FET being driven. $C_{LOAD} = Q_{G(TOT)} / V_{GATE}$, i.e., the total gate charge at a specified V_{GATE}, divided by V_{GATE}. C_{ISS} is not an equivalent measure of C_{LOAD}. C_{ISS} is a small signal equivalent capacitance, whereas C_{LOAD} is a large-signal equivalent.

The recommended value for $C_{SEC(NET)}$ is approximately 10 to 20 times C_{LOAD} (the equivalent gate capacitance), to give approximately 5% to 10% switching ripple on the V_{SEC} rails. Other values are possible; however, lower values will result in higher ripple. Larger $C_{SEC(NET)}$ value will require a longer startup time. The maximum recommended value of $C_{SEC(NET)}$ = 100 nF should not be exceeded.

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Typical Application Example

Figure 12 shows a typical application for driving a GaN transistor with a bipolar drive arrangement.

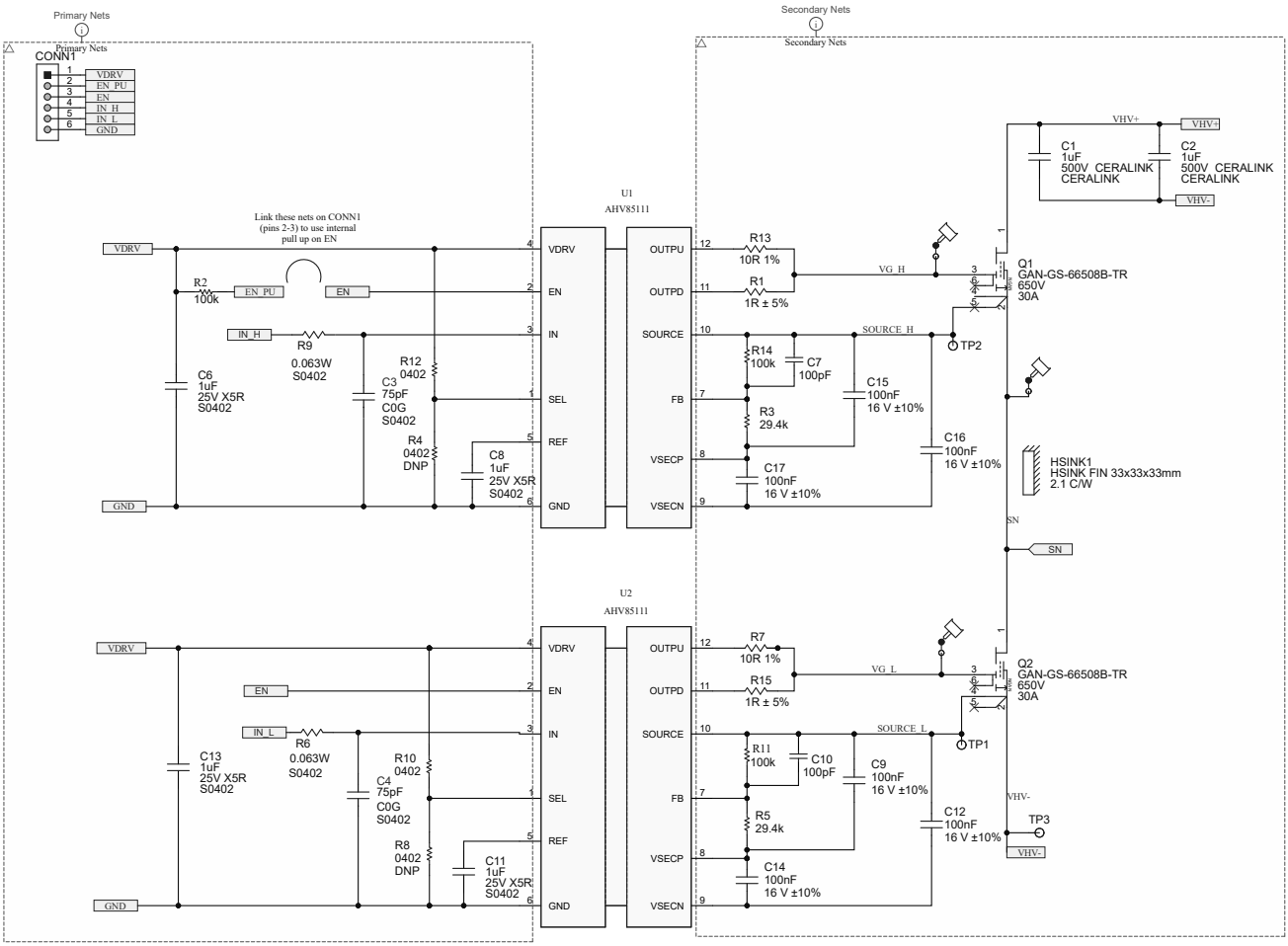

Figure 12: APEK85111KNH-02-T-MH schematic for driving a GaN transistor with a bipolar drive arrangement.

APEK85111KNH-02-T-MH is a design example for half bridge gate driver with GaN transistors. There is also a bipolar output drive configuration for additional protection against false turn-on events. The design parameters are shown in Table 2.

Table 2: Design Parameters

Parameter	Value	Unit
V_{DRV}	10.8–13.2	V
Maximum Switching Frequency	1000 [1]	kHz
$C_{SEC(NET)}$	50	nF
VSECP Voltage	5.4	V
V_{SEC_RIPPLE}	5–10	%

[1] Frequency depends on factors like heat sinking, temperature, high voltage decoupling capacitance and IN PWM duty cycle range.

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PCB LAYOUT

Layout Guidelines

The following are some key points to consider while doing the PCB layout for the best performance with AHV85111:

- Place the AHV85111 gate driver as close as possible to the transistor. This is necessary to minimize the path of the high peak currents. This arrangement will also minimize the loop inductance and noise injection on the gate signals.
- Ensure that the resistors connected between the isolated output drive pins to the gate of the transistor are high-power rated and have high power surge withstanding capability.
- Decoupling capacitors must be connected close to the VDRV/GND, REF/GND, VSECP/SOURCE, and VSECN/SOURCE pin-pairs.
- The path connecting to the source of the transistor should be minimized to avoid large parasitic inductances.

The layout should have good thermal relief to help dissipate heat from the gate driver to the PCB. It is recommended to use vias to maximize thermal conductivity.

Further detailed PCB layout guidelines are available in the application note Design and Application Guide for the AHV85111.

Layout Example

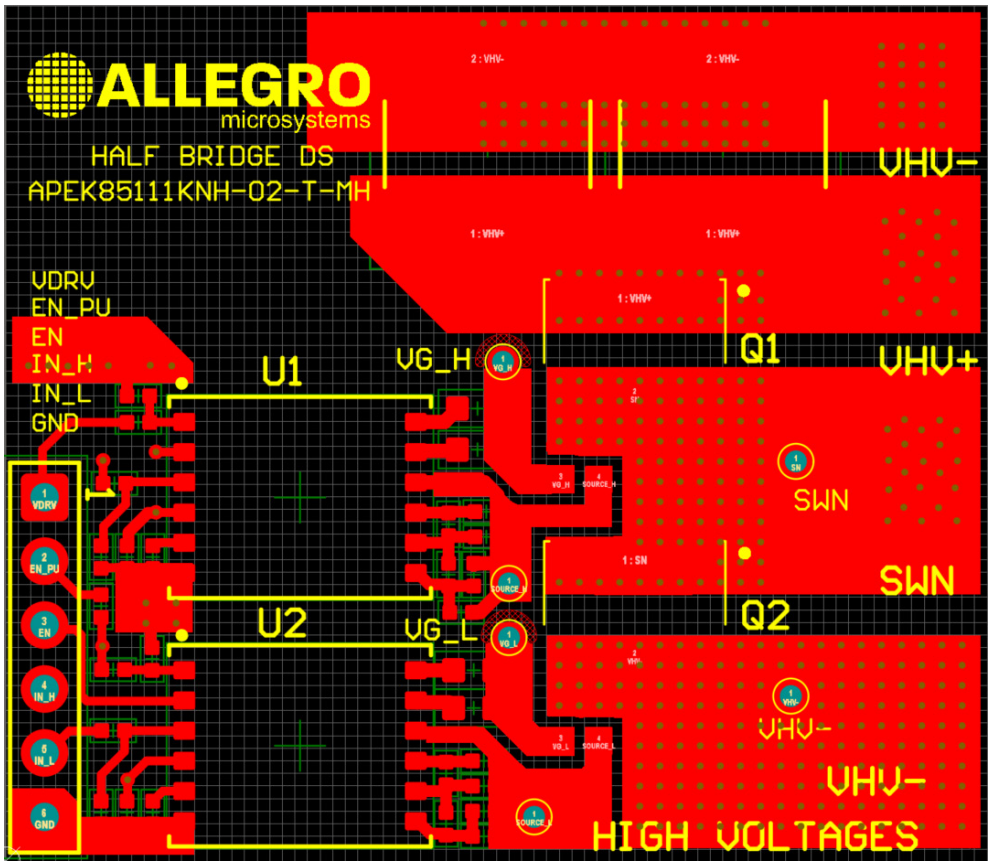

Figure 13: Example PCB Layout

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SYSTEM IMMUNITY TO EXTERNAL TRANSIENTS

During various system-level events, large transient currents can flow for short periods. Examples of this include lightning surge testing to IEC61000-4-5, and system-level ESD testing to IEC61000-4-2. During these events, the large transient currents that flow can also create large stray magnetic fields, and these can also couple unintentionally to the isolated gate driver.

It is recommended to use the driver enable (EN) pin to achieve a power-train “safe-state” during such external transient events. An example of the use of this safe-state architecture is shown in Figure 14, for a Totem-Pole PFC power stage. When a surge event is detected, the system controller inhibits the PWM gate drive signal to both GaN and MOS legs, and also pulls down the open-drain Enable (EN) lines to all drivers. This puts the power train into a safe state and ensures a robust response to the surge event.

For further details, refer to the application note Design and Application Guide for the AHV85111.

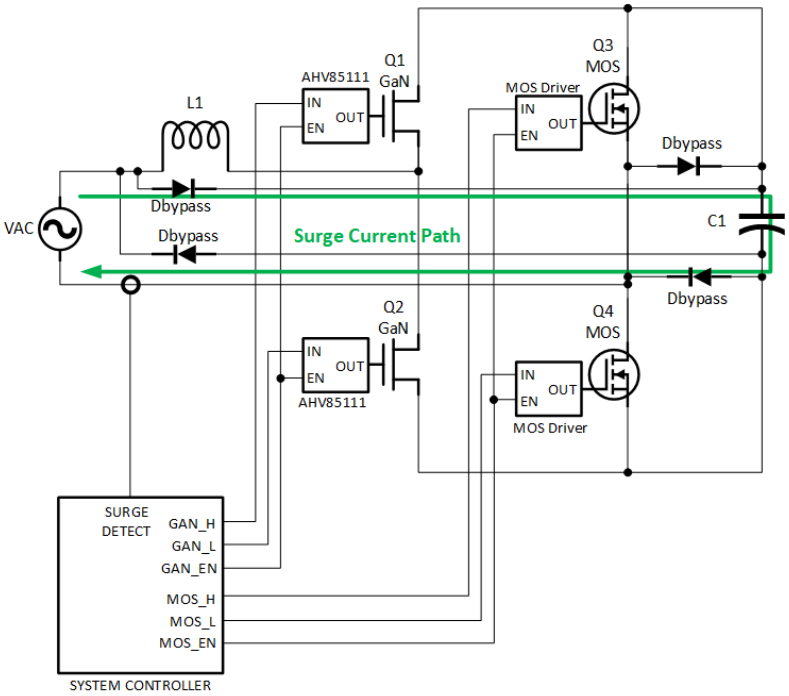

Figure 14: Block diagram of system level surge-detection inhibit signal; used to disable isolated gate drivers using the EN pins

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PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

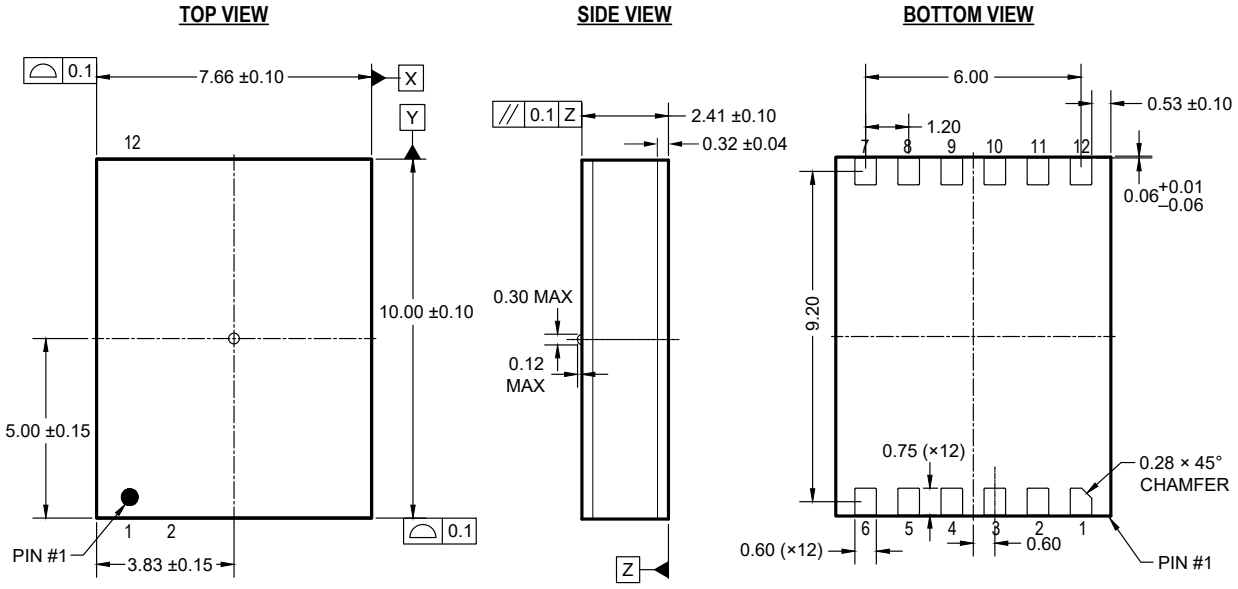
(Reference Allegro DWG-0000919)

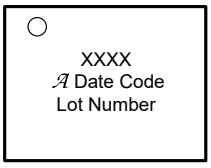
NOT TO SCALE

Dimensions in millimeters

Dimensions exclusive of mold flash, gate burrs, and dambar protrusions

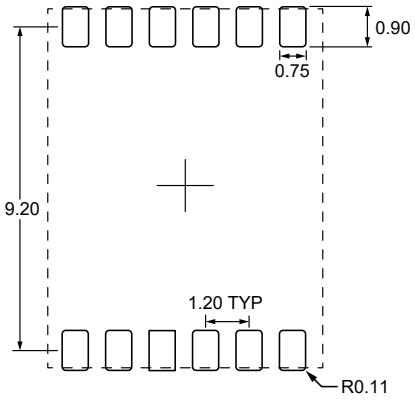
Exact case and lead configuration at supplier discretion within limits shown





STANDARD BRANDING REFERENCE VIEW

Line 1: Part Number
Line 2: Logo A, 4 digit Date Code
Line 3: Assembly Lot Number



PCB LAYOUT REFERENCE VIEW

Reference Land Pattern Layout.
All pads are a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances (reference EIA/JEDEC Standard JESD51-5)

Figure 15: AHV85111 NH Package Outline

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Revision History

Number	Date	Description
–	September 13, 2023	Initial release

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