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Common Mode Rejection Ratio in Dual Junction Field Effect Transistors

By Kirkwood Rough and Timothy S. McCune

When choosing the optimal JFET for a new circuit, a characteristic often overlooked is how the part's design affects the rejection of unwanted inputs while amplifying the signal as accurately as possible. Single JFETs provide excellent impedance matching and low-noise amplification, but lack one important quality of their dual counterparts – dual discrete devices largely reject common signals. This important characteristic – Common Mode Rejection – means that selecting the right dual JFET can be the most cost-effective way of improving signal-to-noise ratio in a design.

All dual JFETs achieve Common Mode Rejection to some extent, but creating a part to optimize this requires specialized design techniques. Linear Systems Founder John H. Hall led this work in the early 1960s as a protégé to industry pioneer Jean Hoerni at Union Carbide's semiconductor division. The need for electrical characteristic matching by the two halves of the dual component over a wide range of temperatures was obvious, but deviations in epitaxial surfaces and other issues made this design work challenging. After heated arguments with more senior developers at Union Carbide, Hall eventually convinced Hoerni to let him try his approach.

Dual transistors – bipolars as well as JFETs – had to that point been created from two separate pieces of silicon. Each die would be tested for specific electrical characteristics and then matched by hand in a special package. At room temperature, duals made this way would match, but as temperatures changed, the characteristics of the separate halves deviated from each other.

To correct this problem, Hall envisioned the most intricate dual design yet conceived. Rather than each half of the dual being set side-by-side, he would weave the transistors together. This design enabled unprecedented matching over a wide range of temperatures, creating very high Common Mode Rejection Ratios.

First with bipolar transistors and later with JFETs, Hall improved the designs of these so-called monolithic tightly matched duals over the course of a 50-year career. Hall and his design team developed new and more capable cross-coupling methods to provide current distribution nearly identical in each half of the dual component. This achieved ultra-close matching over a wide range of temperatures, the key to having consistently high Common Mode Rejection.

Common Mode Rejection Ratio, expressed in dBV, is the common coupled voltage influence over frequency on a differential amplifier input stage. The input of a discrete differential amplifier, most often, is a dual gain element such as a dual Bipolar junction transistor, MOS or junction type Field Effect transistor, Thermionic Triode, Etc. Ideally the input gain element pair is perfectly matched in transconductance (Gm), offset (ΔVin), temperature coefficient (Δt), and noise (Vn). However any two gain elements separated by a finite space will inevitably have differences in these characteristics as a function of spatial differences in fabrication. John Hall's cross-coupled dual device structure was what evolved to mitigate this problem.

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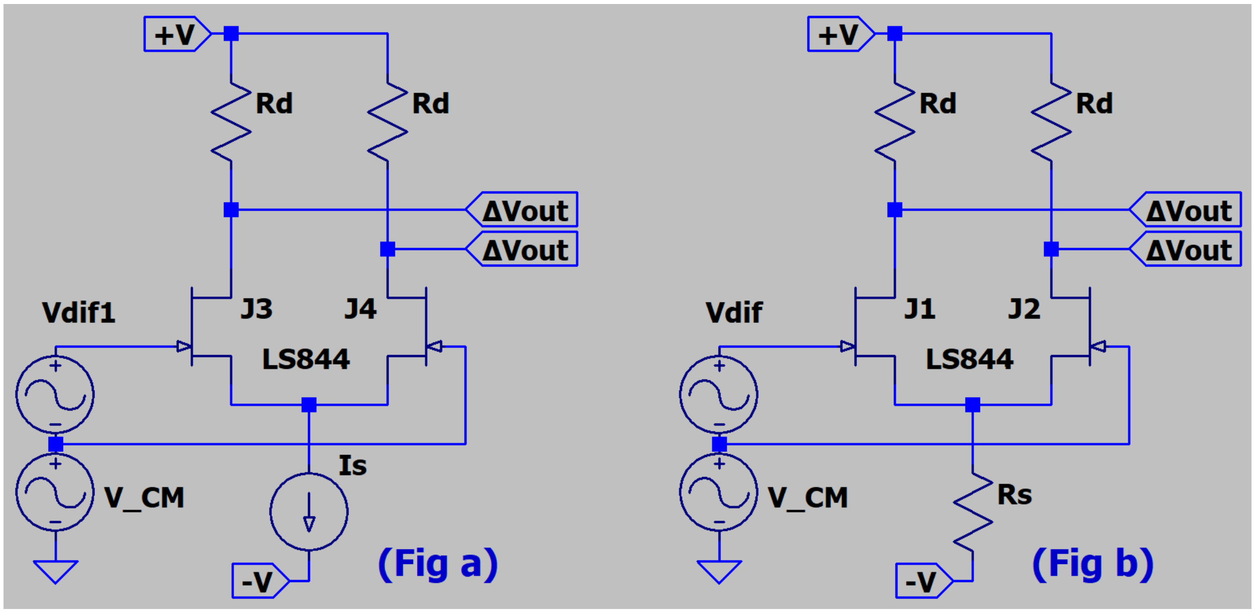
Limiting this to Junction FET's, two equally fabricated parts on a silicon wafer adjacent to each other will have differences in doping distribution concentrations, crystal uniformity and thermal offset during processing. Whereas, if both parts occupied the same space, or nearly so, distribution of fabrication differences would approach the same values and therefore approach the ideal. To that end, these JFET device structures are merged, so that the dies are a uniformly interleaved area of both JFET's.

For instance, the LS840 series of Dual JFETs fabricated this way exhibit low common mode noise, and tight matching of VGS and Gm. When used as a differential amplifier, common mode input voltage influence to the differential input voltage is minimized to its lowest value when the sources are current source biased, (High CMMR).

Common source constant current biasing maintains an invariant total drain current regardless of input signal differential amplitude having a common mode voltage influence. (***fig a***) A resistive current bias will have a varied source current and present a ΔV gain where common mode V is involved. (***fig b***) An Audio amplifier potentially benefits from resistive bias by the slight gain variation influence of input signal amplitude promoting even order harmonics. However, Instrumentation amplifiers need high linearity and typically use a constant current source bias. This results in constant total drain current with no gain modulation. Common mode voltage influence on the signal path is significantly diminished when a current source resistance approaches infinity.



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