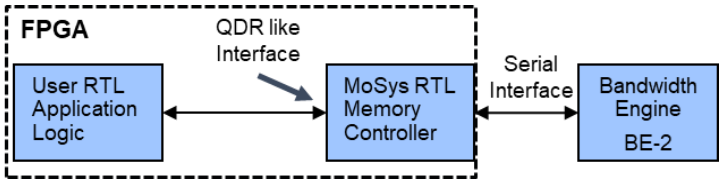
MoSys Bandwidth Engine to FPGA RTL Overview for BE-2 with 576Mb

TECH BRIEF

OVERVIEW

The FPGA RTL Memory Controller that interfaces with the MoSys Bandwidth Engine. This controller is between the User Application logic and the BE device. It handles all the logic for the Serial GigaChip Interface (GCI) between the FPGA and BE.

The signals interface at the User Application provides Bandwidth Engine User a simple SRAM memory read/write operations with burst capability. This simple interface shields the users from the BE2 commands and the scheduling logic for Bandwidth Engine memory partition timing.



The Memory Controller RTL is designed to simplify and make transparent the User Application Interface of the FPGA to the Bandwidth Engine Memory. Which in turn, uses the serial 16 lanes of SerDes and implements the GCI protocol.

BE-2 Transaction Rate

GCI Bit Rate	Lanes per port	Reads per Port	Writes per port
10.3125Gbps	4	500M	250M
12.5Gbps	4	625M	312.5M
10.3125Gbps	8	1B	500M
12.5Gbps	8	1.25B	625M

Port B for Dual Port use or with Port A for Extreme High Bandwidth Applications

KEY FEATURES

RTL memory interface to User Application is User Defined.

--**Typical I/Fs are 8, 16, 32, 36, 64 bit**

Inter-operability with all FPGA vendors

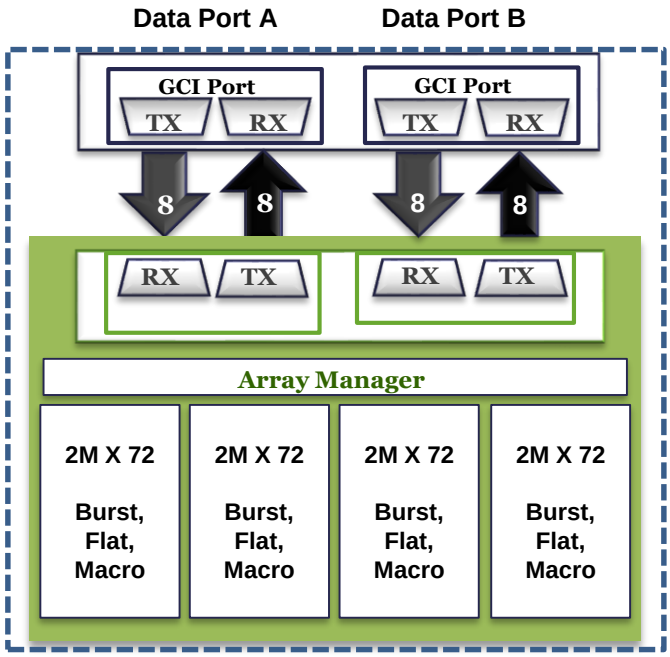
- BE-2 has 576 Mb of storage

RTL Supplied by MoSys

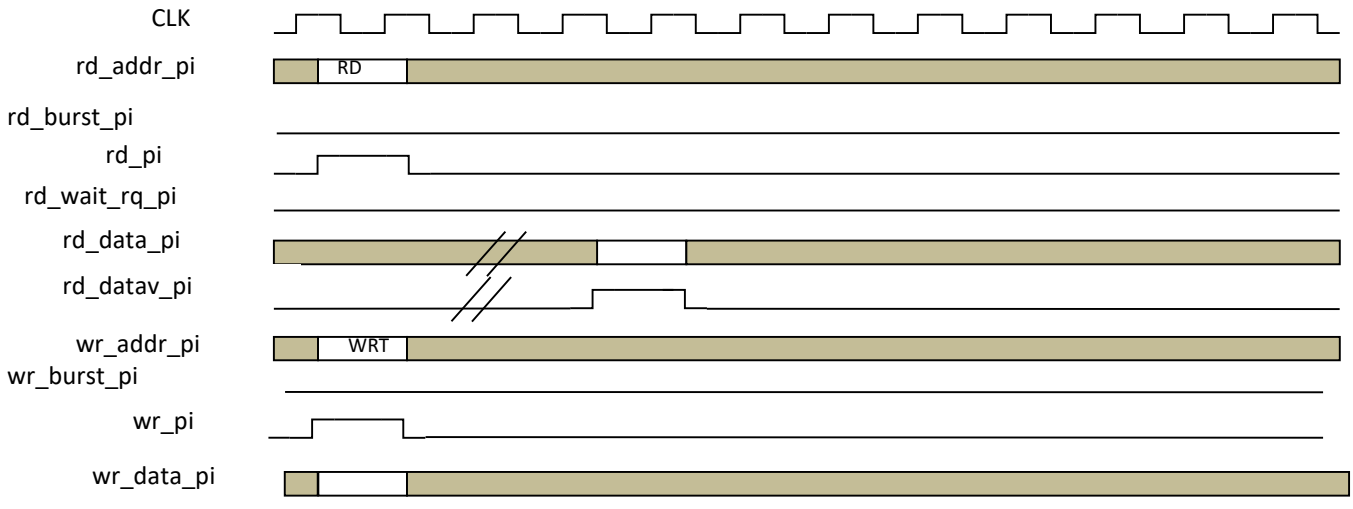
- User selected WORD width
  - x8, x16, x32, x36, x64, x72b
  - Handles issues of timing, protocol and address translation to BE memory configuration

Utilizes a MoSys serial High Speed GCI Interface

- Support 4, 8 or 16 lanes of SerDes depending on pins available and bandwidth requirements
- SerDes can operate at either 10 .3125 or 12.5 Gbps
- Controls the GCI serial Protocol



Single Read/Write Transactions



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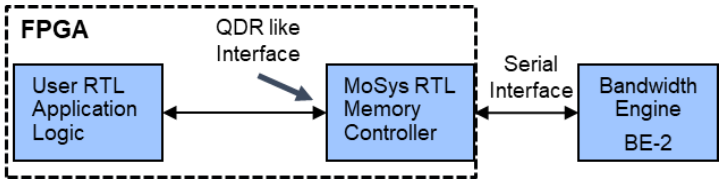

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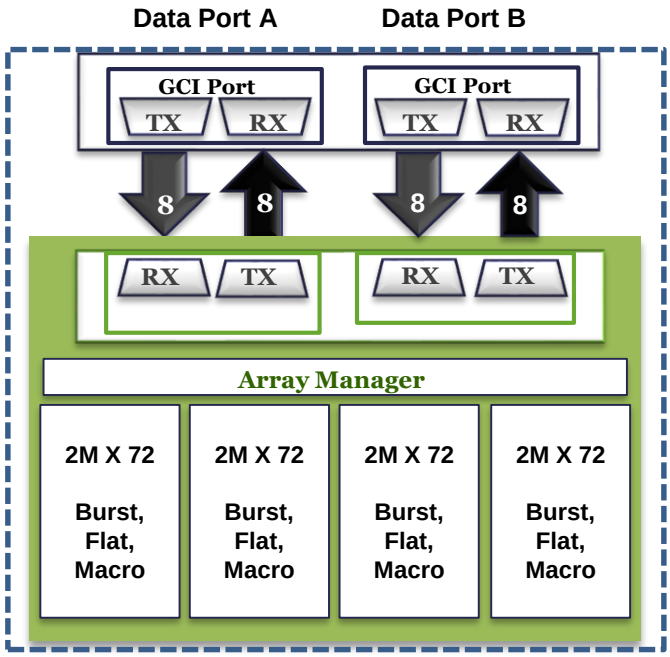

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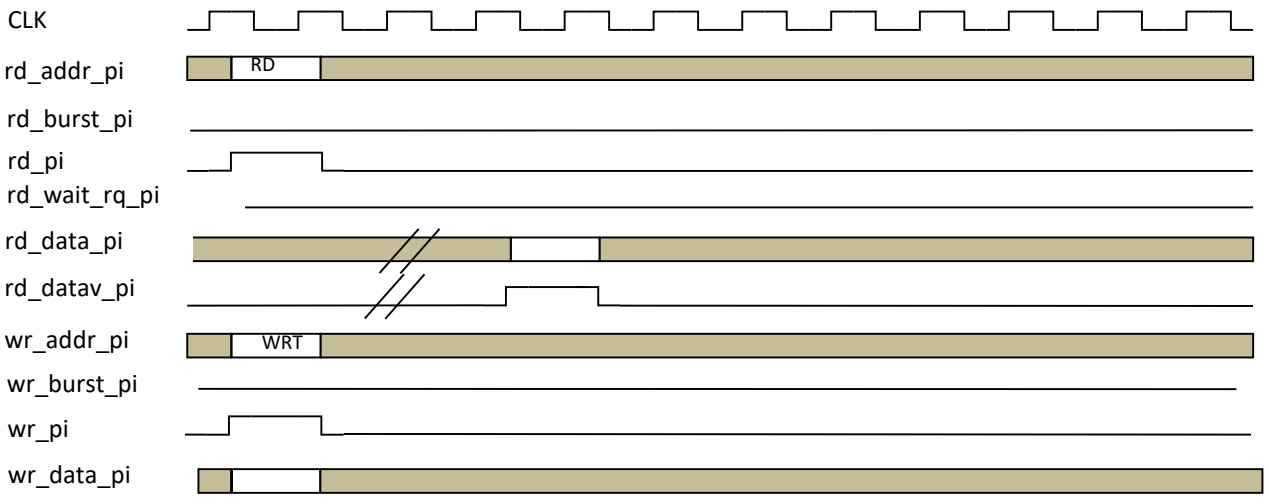


Application Read Interface Signals

SIGNAL NAME	WIDTH	DIR	DESCRIPTION
Read Interface			
rd_p	1	In	Assertion of this signal indicates that this is a read transaction.
rd_addr_p	32	In	Read address. Please refer to the Address section of this specification to see the detail of this address field.
rd_partsel_p	1	In	Indicates the BE-2 partition that this read command will be operated upon: 0 = Partition 0 for GCI port A, Partition 1 for GCI port B 1 = Partition 2 for GCI port A, Partition 3 for GCI port B
rd_data_p0	*	Out	Returned data from BE-2 memory. This data is qualified by the “rd_datav_p0” signal
rd_data_p1	*	Out	Returned data from BE-2 memory. This data is qualified by the “rd_datav_p1” signal. Note that rd_data_p1 will only have valid data if rd_data_p0 is valid as well. rd
rd_datav_p0	1	Out	The Memory Controller asserts this signal to indicate the current data in the “rd_data_p0” bus is valid
rd_datav_p1	1	Out	The Memory Controller asserts this signal to indicate the current data in the “rd_data_p1” bus is valid. Note that rd_data_p1 will only have valid data if rd_data_p0 is valid as well
rd_wait_rq_p	1	Out	The Memory controller asserts “rd_wait_rq_p” to indicate that it cannot accept the current read request from user. The User Application should hold all the request signals (rd_p, rd_addr_p …) until the de-assertion of this signal.

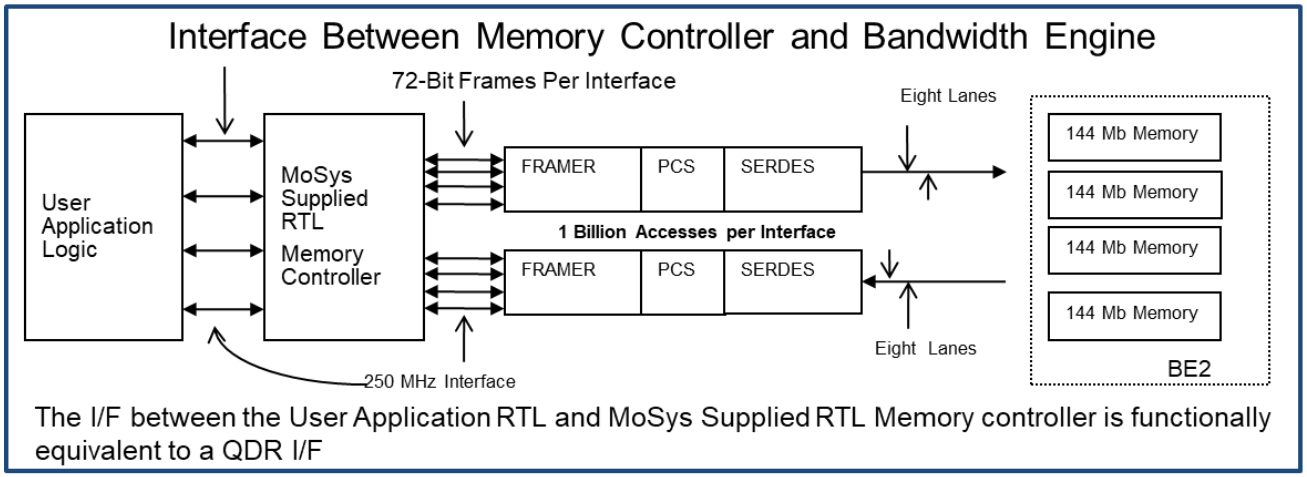
Application Write Interface Signals

SIGNAL NAME	WIDTH	DIR	DESCRIPTION
Write Interface			
wr_p	1	In	Assertion of this signal indicates that this is a write transaction.
wr_addr_p	32	In	Write address of the memory for this transaction. Please refer to the Address section of this specification to see the detail of this address field.
wr_partsel_p	1	In	Indicates the BE-2 partition that this write command will be operated upon: 0=Partition 0 for GCI port A, Partition 1 for GCI port B 1=Partition 2 for GCI port A, Partition 3 for GCI port B
wr_data_p	*	In	Write data from the User Application logic.
wr_wait_rq_p	1	Out	The Memory controller asserts “wr_wait_rq_p” to indicate that it cannot accept the current write request. The User Application should hold all the request signals (wr_p, wr_addr_p ...) until the de-assertion of this signal.

*** RTL versions available for x8, x16, x32, etc.**

The flexible MoSys RTL controller allows the user to define the word width.

The controller handles all the interface with the memory, so the user only sees a QDR like interface.



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