MSMP1 Hardware Manual

Version: **2.2**

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CHAPTER

ONE

ABOUT THIS MANUAL

1.1 Imprint

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1.2 Disclaimer

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1.5 Care and Maintenance

- Keep the device dry. Precipitation, humidity, and all types of liquids or moisture can contain minerals that will corrode electronic circuits. If your device does get wet, allow it to dry completely.
- Do not use or store the device in dusty, dirty areas. Its moving parts and electronic components can be damaged.
- Do not store the device in hot areas. High temperatures can shorten the life of electronic devices, damage batteries, and warp or melt certain plastics.
- Do not store the device in cold areas. When the device returns to its normal temperature, moisture can form inside the device and damage electronic circuit boards.
- Do not attempt to open the device.
- Do not drop, knock, or shake the device. Rough handling can break internal circuit boards and fine mechanics.
- Do not use harsh chemicals, cleaning solvents, or strong detergents to clean the device.
- Do not paint the device. Paint can clog the moving parts and prevent proper operation.
- Unauthorized modifications or attachments could damage the device and may violate regulations governing radio devices.

1.6 Change Log

Revision	Date	Revised	Comment
1.0	13.07.2022	dk	Initial creation
2.0	28.04.2023	wa	Updating STMP1 to STM32MP1, ST Microelectronics to STMicroelectronics
2.1	23.05.2023	aw	Correcting typos for table 3.8.10 MSMP1 SiP Pads • SIP Pad Y7 • SIP Pad AA6
2.2	06.03.2024	aw	• USB intefaces exchanged, interfaces are now compliant with OSM standard - Inserted chapter 3 with additional information on the OSM standard - minor changes

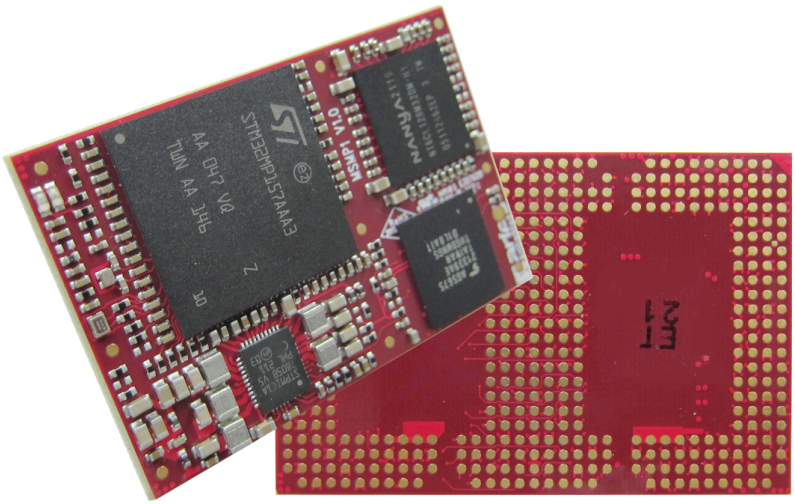
CHAPTER

TWO

OVERVIEW

2.1 MSMP1 Microprocessor SiP

The MSMP1 is the Open Standard Module compliant System-In-Package based on STMicroelectronics STM32MP1 Family architecture offering high-performance single/dual CortexA7 cores in combination with a CortexM4 core. The MSMP1 combines compact design and a wide range of services, bringing low power consumption, thermal efficiency and low-cost to embedded systems.



MSMP1 fits to an OSM size M SoM in a size of only 30x45mm. Due to its 476 contacts the SoM offer the CPU almost transparently so that it can be used almost without functional restrictions due to the pin-multiplexing of the CPU.

2.2 Feature Set

- **STM32MP1 (STMicroelectronics)**
  - Single/Dual Cortex-A7, up to 800MHz
  - Cortex-M4, up to 209MHz
- 512MB – 1GB DDR3L RAM
- 4GB – 64GB eMMC NAND Flash
- 10/100/1000MBit Ethernet
- USB2.0 Host/OTG
- 2x CAN
- UART, I2C, SPI
- ADC, DAC
- Parallel display port
- Camera interface
- compliant to the SGET OSM standard
- size M, 30x45mm
- 476 contacts
- 0°C..+70°C commercial temperature range
- -30°C..+85°C industrial temperature range

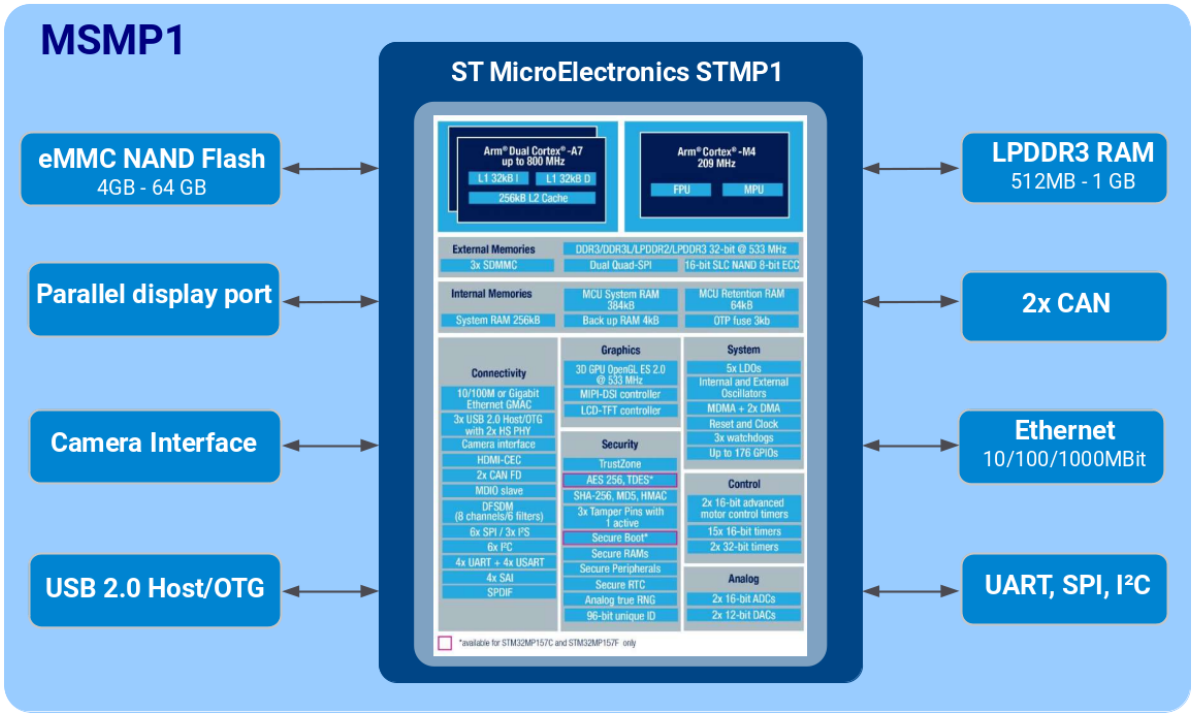
2.3 Order Codes

The MSMP1 SoM is available in the following standard configurations:

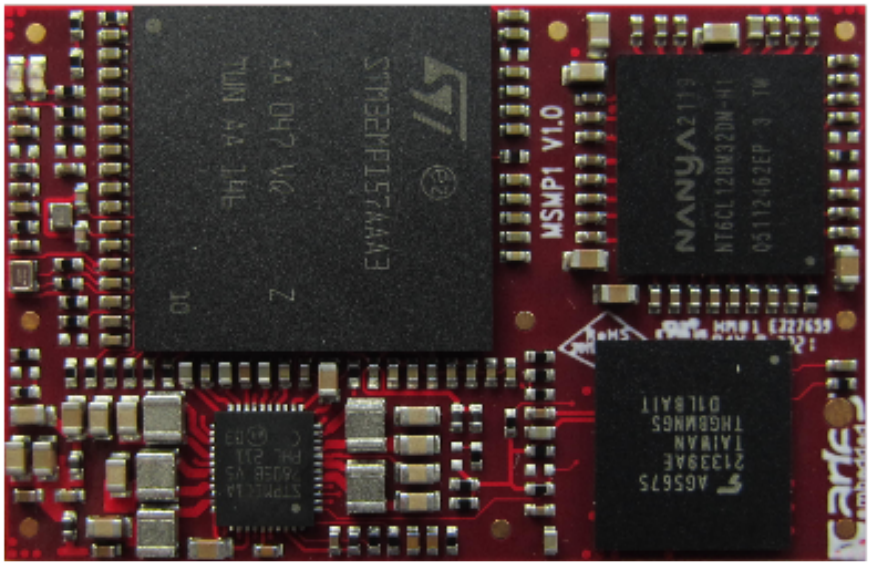
- **MSMP151-A0C**
  - STM32MP151
  - 512MB LPDDR3 RAM
  - no eMMC
  - 512MBit SPI NOR
  - -25...+85°C
- **MSMP157-BAA**
  - STM32MP157
  - 1GByte LPDDR3 RAM
  - 4GB eMMC
  - 128MBit SPI NOR
  - -25...+85°C

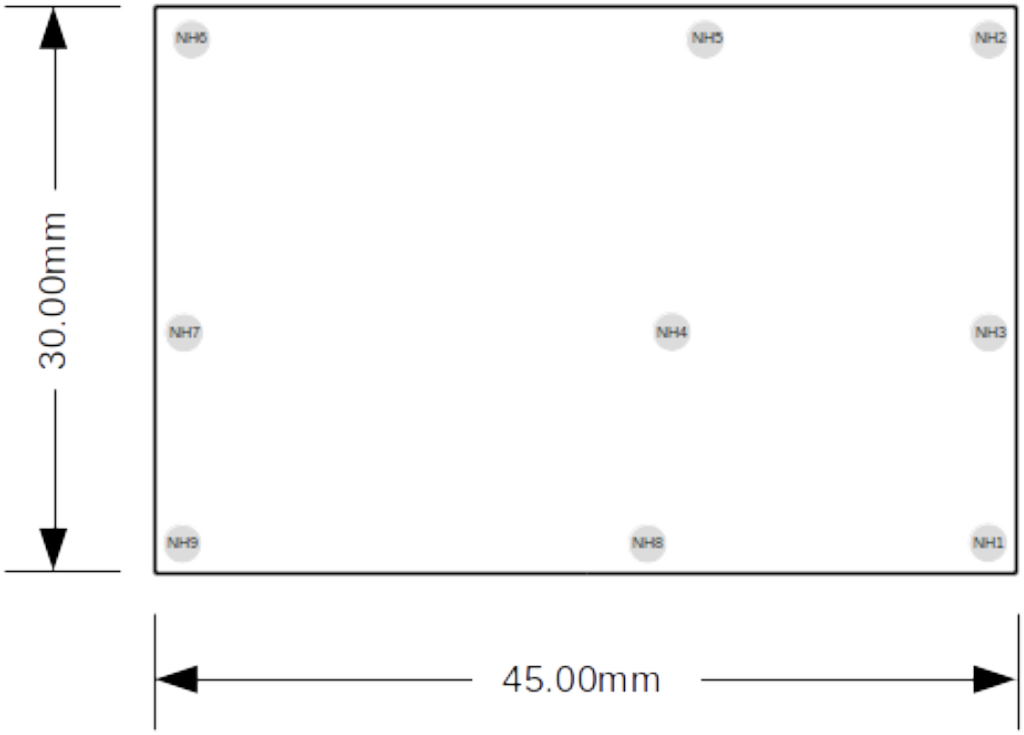
Please contact ARIES Embedded under sales@aries-embeded.de for more information about the availability of other standard products of MSMP1 or custom configurations.

2.4 Block Diagram



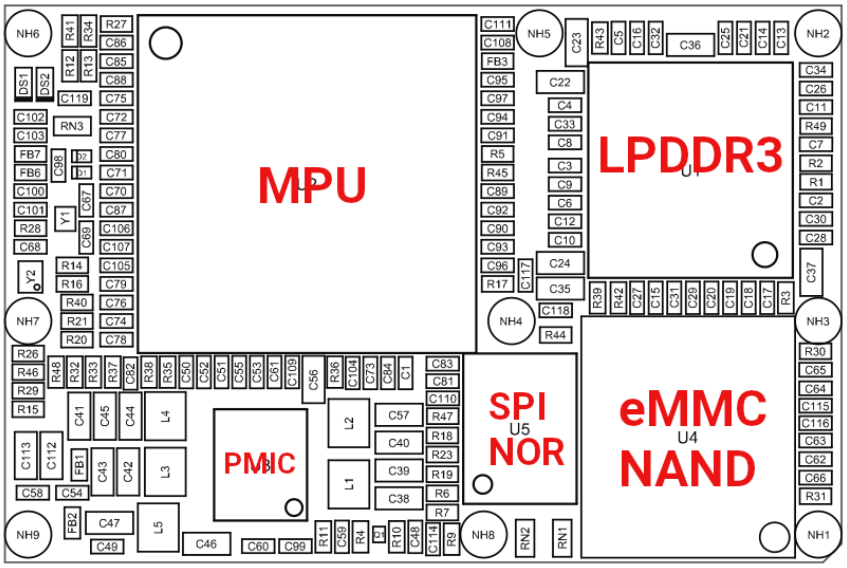
2.5 Dimensions



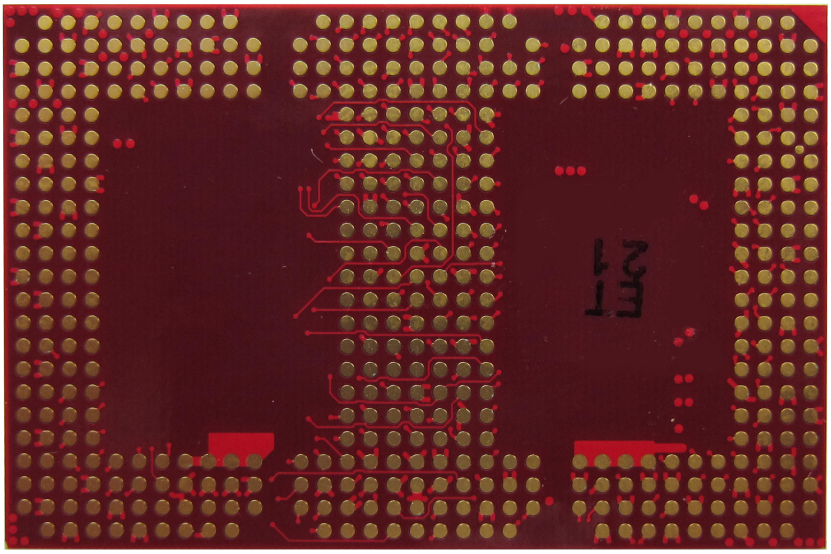


2.6 Part Overview

Assembly Top

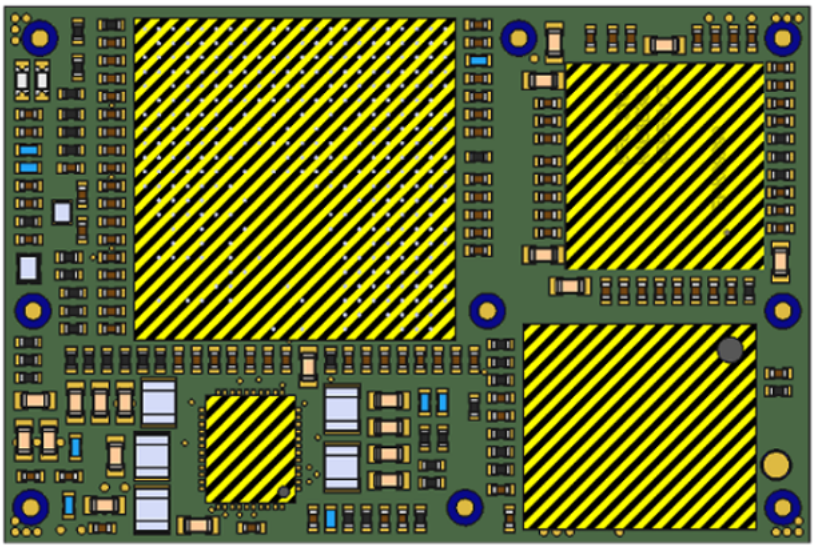


Assembly Bottom



2.7 Handling Recommendations

To avoid mechanical damage to the components populated on MSMP1 it is strongly recommended not to apply mechanical force on the Ball Grid Array (BGA) components. The BGA components are marked as shaded in the figure below:



CHAPTER

THREE

OPEN STANDARD MODUL (OSM)

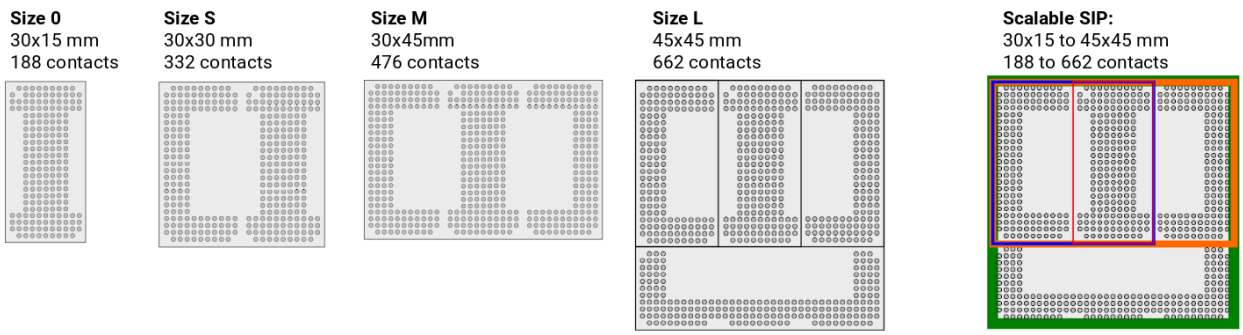
The idea of all Open Standard Modules™ is to create a new, future proof and versatile standard for small-size, low-cost embedded computer modules, combining the following key characteristics:

- Completely machine processible during soldering, assembly and testing
- Pre-tinned LGA package for direct PCB soldering without connector
- Pre-defined soft- and hardware interfaces
- Open-Source in soft- and hardware

The Open Standard Module™ specification allows developing, producing and distributing embedded modules for the most popular MCU32, ARM and x86 architectures. For a growing number of IoT applications this standard helps to combine the advantages of modular embedded computing with increasing requirements regarding costs, space and interfaces.

3.1 Module Sizes and Dimensions

OSM SoMs are highly scalable in size, performance and functionality as they are available in different mechanical sizes and contact count:



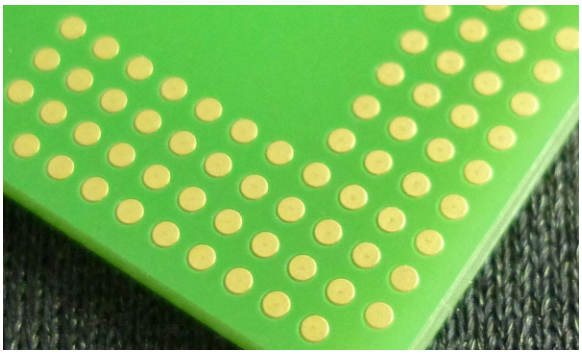
Size	Metrics	Contact Count	Colour Outline
Size-0 – “Zero”	30 mm x 15 mm	188 contacts	red
Size-S – “Small”	30 mm x 30 mm	332 contacts	blue
Size-M – “Medium”	30 mm x 45 mm	476 contacts	orange
Size-L – “Large”	45 mm x 45 mm	662 contacts	green

3.2 Contact Characteristics:

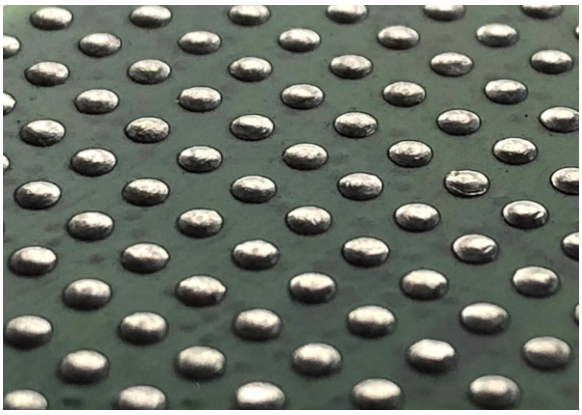
OSM SoMs are available with different contact characteristics:

3.2.1 ENIG-LGA

All OSM-SoMs by ARIES Embedded are using ENIG-LGA contacts on its PCBs:



3.2.2 Fused Tin Grid Array

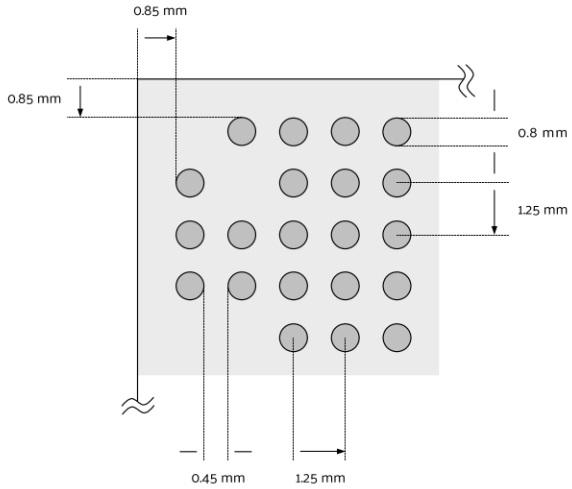


3.2.3 BGA

3.3 Contact Grid

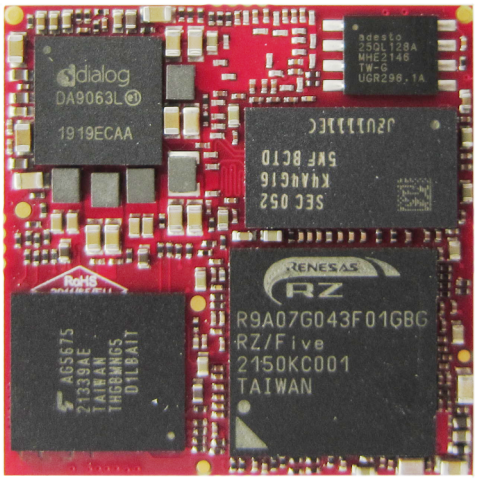
The Contact Grid for the Open Standard Module™ Specification is symmetrically and defines the following dimensions:

- Contact Diameter: 0.8 mm
- Contact Grid: 1.25 mm
- Contact-to-Contact: 0.45 mm
- Contact-to-Edge: 0.85 mm

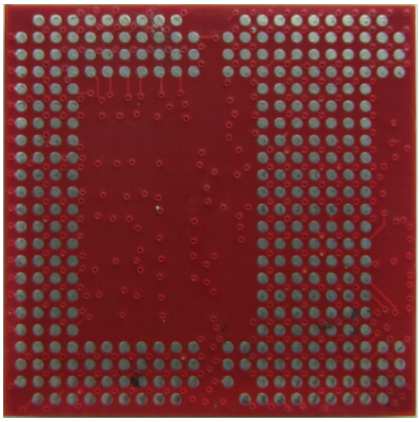


3.4 Recommendations for Processing OSM System on Modules

In the following the MSRZFive-AAA SoM will be used as a reference.



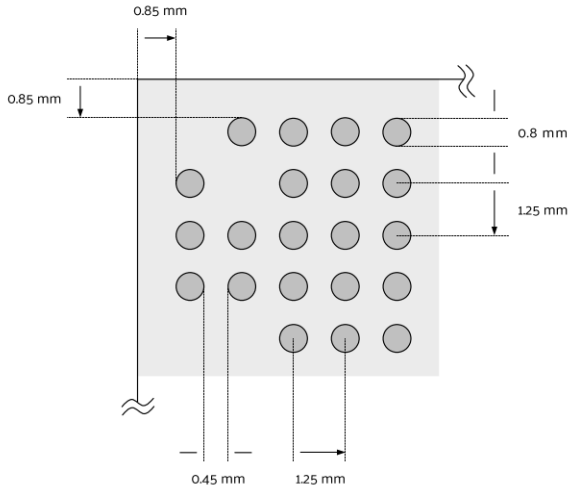
MSRZFive is available as a LGA332 package with round flat pads on the solder side of the SoM:



3.4.1 Design

3.4.1.1 Layout PCB

The connecting pad size of the baseboard layout should be similar to the layout of e.g. the FIVEberry baseboard. The pad size is defined with 0.8mm, the pitch 1.25mm.



3.4.1.2 Stencil

The stencil should have a with of 120µm. The openings in the stencil should be round shape with a diameter of 0.8mm, accordingly.

3.4.2 Process Recommendation

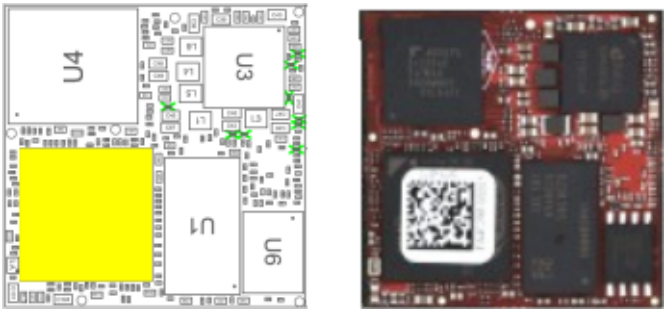
3.4.2.1 Storage

The OSM SoMs are to be handeled as moisture sensitive components. The SoMs shall be stored in suitable vacuum packages with dry packs.

The processing of the SoMs with opened package is limited to 168 hours at a maximum of 30°C and 60% air moisture. In case these values are exceeded and additional drying is necessary, the requirements of J-STD-033 have to b considered.

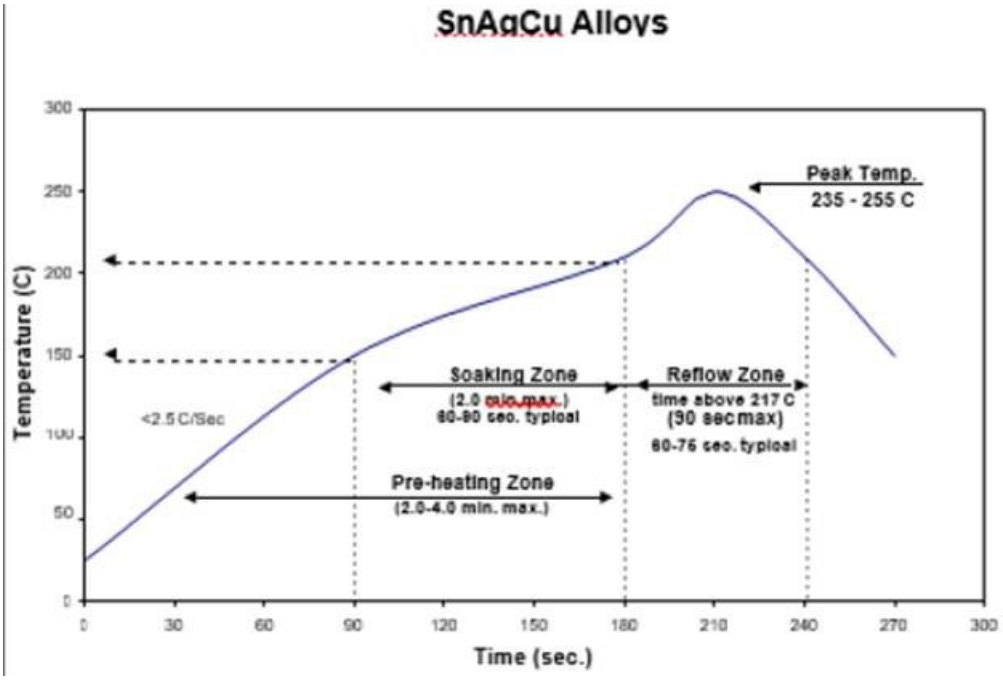
3.4.2.2 Production

For mounting the OSM SoMs the SoMs will be offered to the SMT machine in a tray or a reel. For the pickup of the SoM, using a vacuum nozzle, the SoM should be picked up by using a mechanical point as much as possible in the middle of the SoM, e.g. on U2 (yellow marking).



3.4.2.3 Reflow Soldering

The SoM can be soldered in a reflow soldering process, using a standard RoHS profile. Below picture show the recommendation for the solder paste Kester NP545.



3.5 OSM Design Guide

The primary purpose of OSM Design Guide is to serve as a suggestion for developers of OSM Carrier Boards and for OSM Module customers who wish to have a OSM based system developed. The document should also be valuable to FAEs and Product managers to help them understand the OSM Module infrastructure.

The OSM Design Guide is avaible for download (after registration) under https://sget.org/standards/osm/

CHAPTER

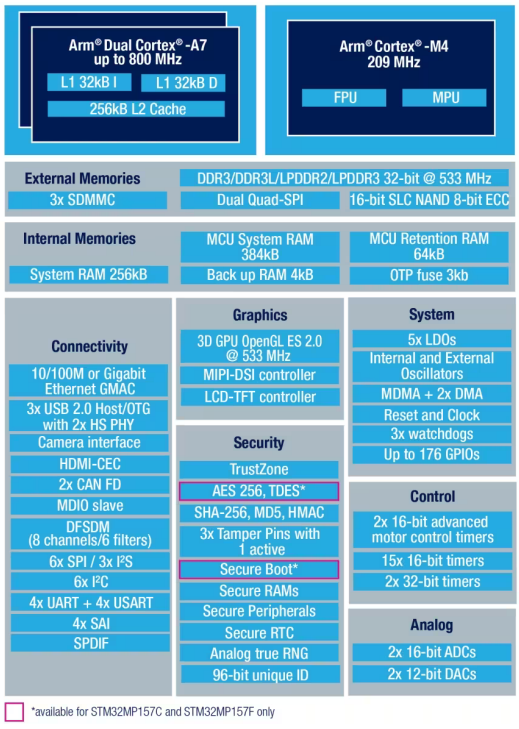
FOUR

RESOURCES

4.1 Components

4.1.1 MPU

STM32MP157 microprocessors are based on the flexible architecture of a Dual Arm® Cortex®-A7 core running up to 800 MHz and Cortex®-M4 at 209 MHz combined with a dedicated 3D graphics processing unit (GPU) and MIPI-DSI display interface and a CAN FD interface. As well as an LCD-TFT display controller, the STM32MP157 line offers 3D GPU, MIPI DSI display interface, CAN FD, 10/100M or Gigabit Ethernet, 3x USB 2.0 Host/OTG and advanced analog.



For more information about the STM32MP157A/D microprocessor please refer to the documentation which is available from STMicroelectronics.

4.1.2 LPDDR3 SDRAM

The MSMP1 is equipped with 1 block of NANYA NT6CL128M32DM-H1 or NT6CL256M32AM LPDDR3 SDRAM resulting in up to 4/8 GB of 32bit memory. Device is available in the commercial temperature range -30°C. . . +105°C. The memory interface operates with 1866Mbps speed rate. The memory interface is clocked at 933MHz using the 1.2V/1.8V SDRAM standard interface.

4.1.2.1 MPU Signals for LPDDR3

MPU Pin	Function	LPDDR3 Pin		MPU Pin	Function	LPDDR3 Pin
K19	DDR_A0	R2		E21	DDR_DQ0	P9
M18	DDR_A1	P2		F21	DDR_DQ1	N9
J18	DDR_A2	N2		H21	DDR_DQ2	N10
J19	DDR_A3	N3		E20	DDR_DQ3	N11
T18	DDR_A4	M3		J21	DDR_DQ4	M8
H19	DDR_A5	F3		H20	DDR_DQ5	M9
U19	DDR_A6	E3		H22	DDR_DQ6	M10
F18	DDR_A7	E2		G19	DDR_DQ7	M11
U18	DDR_A8	D2		N22	DDR_DQ8	F11
H18	DDR_A9	C2		R21	DDR_DQ9	F10
G22	DDR_DQS0_P	L10		P21	DDR_DQ10	F9
G21	DDR_DQS0_N	L11		T20	DDR_DQ11	F8
T22	DDR_DQS1_P	G10		V20	DDR_DQ12	E11
R22	DDR_DQS1_N	G11		R20	DDR_DQ13	E10
C21	DDR_DQS2_P	P10		U21	DDR_DQ14	E9
B22	DDR_DQS2_N	P11		V21	DDR_DQ15	D9
Y21	DDR_DQS3_P	D10		B21	DDR_DQ16	T8
Y22	DDR_DQS3_N	D11		D21	DDR_DQ17	T9
G20	DDR_DM0	L8		D22	DDR_DQ18	T10
T21	DDR_DM1	G8		B20	DDR_DQ19	T11
C22	DDR_DM2	P8		A20	DDR_DQ20	R8
AA22	DDR_DM3	D8		E22	DDR_DQ21	R9
N20	DDR_CLK_P	J3		D20	DDR_DQ22	R10
N21	DDR_CLK_N	J2		A21	DDR_DQ23	R11
R19	DDR_CKE	K3		V22	DDR_DQ24	C11
–	GND	K4		W20	DDR_DQ25	C10
L18	DDR_CS0_N	L3		AB21	DDR_DQ26	C9
L18	DDR_CS0_N	L4		AB20	DDR_DQ27	C8
L21	DDR_ODT	J8		AA21	DDR_DQ28	B11
–	GND	B3		AA20	DDR_DQ29	B10
–	–	B4		W22	DDR_DQ30	B9
–	–	–		W21	DDR_DQ31	B8

4.1.3 SPI-NOR Flash

MSMP1 features a SPI-NOR device in a range of 128MBit to 512MBit.

Device	Capacity
W25Q128JVEIQ	128MBit
W25Q256JVEIQ	256MBit
W25Q512JVEIQ	512MBit

The SPI-NOR flash device uses the following connections:

MPU Pin	Function	SPI-NOR Pin
W13	CS#	1
AB11	DO	2
AA10	WP#	3
	GND	4
AB10	DI	5
V12	CLK	6
AA11	RES#	7
	VCC	7

4.1.4 eMMC Flash

The MSMP1 supports one eMMC NAND Flash in the range of 4-64 GByte. The eMMC provides a high-speed memory card interface compliant with JEDEC Version 5.0, eliminating the need for users to be concerned about directly controlling Flash Memories.

MPU Pin	Function	eMMC Pin
D11	SDMMC2_CMD	M5
B11	SDMMC2_D7	B6
E13	SDMMC2_D6	B5
E11	SDMMC2_D5	B4
F15	SDMMC2_D4	B3
C13	SDMMC2_D3	B2
A12	SDMMC2_D2	A5
B12	SDMMC2_D1	A4
A13	SDMMC2_D0	A3
E2	–	H5
A10	SDMMC2_CK	M6
R2	NRST	K5

4.1.5 PMIC

The power management on the MSMP1 SoM is provided by a STPMIC1xPQR ST-Microelectronics fully integrated power management IC. The device integrates advanced low power features controlled by a host processor via I^2C and IO interface.

MSMP1 is operational for supply voltages in the range of 2.8V to 5.5V.

MSMP1 is available, depending on the installed PMIC, in a version to support either 1.8V IO-voltage or 3.3V IO-voltage.

PMIC Derivatives

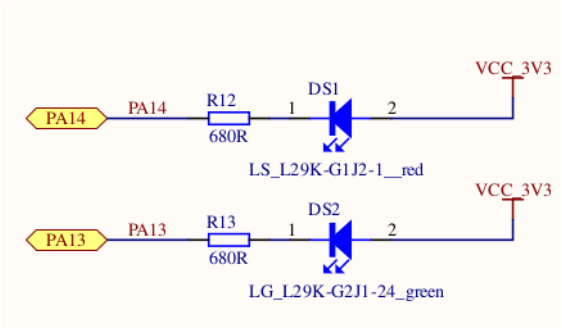
Device	I/O Voltage	Comment
STPMIC1A	3.3V	Standard
STPMIC1B	1.8V	

PMIC connections

MPU Pin	Function	PMIC Pin	SiP Pads
G1	I2C4_SCL/PMIC	4 SCL	–
H4	I2C4_SDA/PMIC	3 SDA	–
T1	PWR_ON	44 PWRCTRL	–
R2	NRST	1 RSTn	–
N2	PMIC/WAKEUP	2 WAKEUP	–
–	PMIC/PONKEYn	17 PONKEYn	AA9
N1	PI8_WKUP	43 INTn	–

4.1.6 User LEDs

The ports PA13 and PA14 are connected to user LEDs as follows:



MPU Pin	Function	SiP Pads	Remarks
R3	PA14	F17	3V3, 680R to PA14 red LED
W3	PA13	E17	3V3, 680R to PA13 green LED

4.2 Interfaces

4.2.1 I2C

When using MSMP1 in conformity to the OSM standard two I2C interfaces are available:

MPU Pin	Function	SiP Pads	Remarks
B9	I2C2_SCL	AA15	2k2 pullup to VCC
E10	I2C2_SDA	AA16	2k2 pullup to VCC
G3	I2C6_SCL	AA20	2k2 pullup to VCC
H3	I2C6_SDA	AA21	2k2 pullup to VCC

4.2.2 I2S

When using MSMP1 in conformity to the OSM standard one I2S interface is available:

MPU Pin	Function	SiP Pads
E1	I2S2_SDI (TIM8_CH4)	V21
E3	I2S2_SDO (TIM8_ETR)	W21
D7	I2S2_MCK (GPIO/UART8_TX_CH4)	V18
D1	I2S2_WS (TIM5_CH4)	W18
E2	I2S2_CK (TIM8_BKIN2)	W20

4.2.3 SPI

When using MSMP1 in conformity to the OSM standard three SPI interface are available:

MPU Pin	Function	SiP Pads
G2	SPI1_SCK	D29
H5	SPI1_MISO	C29
K5	SPI1_MOSI	D30
F4	SPI1_NSS	C30
C5	SPI3_SCK	U16
A8	SPI3_MISO	U15
AA8	SPI3_MOSI	V15
V6	SPI3_NSS	Y15
E4	SPI4_SCK	Y21
C12	SPI4_MISO	Y22
B4	SPI4_MOSI	Y23
D5	SPI4_NSS	AA23

4.2.4 JTAG

MPU Pin	Function	SiP Pads
D17	JTAG_TCK	N17
E17	JTAG_TMS	N19
D16	JTAG_TDI	P17
E16	JTAG_TDO	R17
E15	JTAG_NTRST	R19

4.2.5 UART

4.2.5.1 UART

MPU Pin	Function	SiP Pads
AA11	UART7_RX (SPI5_NSS)	A14
AA10	UART7_TX (SPI5_SCK)	B13
AB10	UART7_RTS (SPI5_MISO)	C13
AB11	UART7_CTS (SPI5_MOSI)	C14

4.2.5.2 UART-Console

MPU Pin	Function	SiP Pads
V13	UART4_RX	D22
U11	UART4_TX	D23

4.2.5.3 USART

MPU Pin	Function	SiP Pads
F9	USART2_RX (GPIO)	D14
D9	USART2_TX (GPIO)	D13
C9	USART2_RTS (FMC_NOE)	D15
C4	USART2_CTS (TIM1_BKIN)	D16
F10	USART2_CK (GPIO)	B21

4.2.6 TIMER/PWM

MPU Pin	Function	SiP Pads
B13	PA8 (TIM1_CH1)	E18
A11	PA9 (TIM1_CH2)	F18
A4	PE13 (TIM1_CH3)	G18
Y16	PA11 (TIM1_CH4)	H18
B1	PH10 (TIM5_CH1)	J18
B3	PH11 (TIM5_CH2)	K18

4.2.7 Ethernet

MPU Pin	Function	SiP Pads
U8	ETH_RGMII_CLK125	N16
AB4	ETH_RGMII_GTX_CLK	J15
Y5	ETH_RGMII_TX_CTL	K16
AA1	ETH_RGMII_TXD0	H15
AA2	ETH_RGMII_TXD1	G15
Y1	ETH_RGMII_TXD2	H16
Y2	ETH_RGMII_TXD3	G16
V4	ETH_RGMII_RX_CLK	R15
Y9	ETH_RGMII_RX_CTL	M15
AB6	ETH_RGMII_RXD0	K15
AA6	ETH_RGMII_RXD1	L15
V11	ETH_RGMII_RXD2	N15
W2	ETH_RGMII_RXD3	P15
W1	ETH_GMII_RX_ER	L16
AB7	ETH_GMII_CRS	E16
Y6	ETH_GMII_COL	F15
AB3	ETH_MDC	T16
AB2	ETH_MDIO	T15
W5	ETH_MDINT	M2
J4	ETH_PHYINT	R34

4.2.8 FDCAN

MPU Pin	Function	SiP Pads
D3	FDCAN1_TX	AC17
C2	FDCAN1_RX	AB17
V10	FDCAN2_TX	AC19
AA7	FDCAN2_RX	AB19

4.2.9 COM/FMC

MPU Pin	Function	SiP Pads
M3	PD14 (GPIO/FMC_AD0)	A15
L1	PD15 (GPIO/FMC_AD1)	A16
C10	PD0 (GPIO/FMC_AD2/I2C5_SDA)	A17
B10	PD1 (GPIO/FMC_AD3/I2C5_SCL)	A18
W10	PE7 (GPIO/FMC_AD4/QSPI_BK2_IO0)	A19
Y12	PE8 (GPIO/FMC_AD5/QSPI_BK2_IO1)	A20
W11	PE9 (GPIO/FMC_AD6/QSPI_BK2_IO2)	A21
W14	PE10 (GPIO/FMC_AD7/QSPI_BK2_IO3)	B15
AB9	PD11 (GPIO/FMC_CLE)	B16
W12	PD12 (GPIO/FMC_ALE)	B17
L3	PD6 (GPIO/FMC_NWAIT)	B18
A9	PD5 (GPIO/FMC_NWE)	B19
W15	PG9 (GPIO/FMC_NCE)	B20
N2	PC13 (RTC_OUT1)	C15

4.2.10 USB1 Interface (OTG)

MPU Pin	Function	SiP Pads
AA14	USB1_D_N	AB23
AB14	USB1_D_P	AC22
Y17	OTG_ID	AB22
V15	OTG_VBUS	AB20

4.2.11 USB2 Interface (Host)

MPU Pin	Function	SiP Pads
AB15	USB2_D_N	AB13
AA15	USB2_D_P	AC14

4.2.12 DISPLAY-RGB

MPU Pin	Function	SiP Pads
F3	LCD_R0	C17
J2	LCD_R1	AA29
L6	LCD_R2	Y7
K4	LCD_R3	AA6
J1	LCD_R4	Y6
K2	LCD_R5	AA5
K1	LCD_R6	Y5
L5	LCD_R7	Y4
L4	LCD_G0	C19
H6	LCD_G1	AA30
L2	LCD_G2	W4
J3	LCD_G3	V3
K6	LCD_G4	V4
D8	LCD_G5	U3
E7	LCD_G6	T3
E8	LCD_G7	T4
B8	LCD_B0	C21
A7	LCD_B1	AA31
B7	LCD_B2	R4
C7	LCD_B3	R3
B6	LCD_B4	P3
A6	LCD_B5	N3
C6	LCD_B6	N4
A5	LCD_B7	M3
D2	LCD_CLK	M4
H1	LCD_VSYNC	L3
H2	LCD_HSYNC	K3
T4	LCD_BL_CTRL	K4
B5	LCD_DE	J4

4.2.13 DISPLAY-DSI

MPU Pin	Function	SiP Pads
A15	DSI_DATA0_N	AB11
B15	DSI_DATA0_P	AB10
A17	DSI_DATA1_N	AC9
B17	DSI_DATA1_P	AC8
A16	DSI_CLK_N	AB8
B16	DSI_CLK_P	AB7
V14	PD13/DSI_TE	AA3

4.2.14 SDCARD

MPU Pin	Function	SiP Pads
E12	SDMMC1_CK	F21
D12	SDMMC1_CMD	E20
E14	SDMMC1_D0	G20
D14	SDMMC1_D1	G21
F14	SDMMC1_D2	H20
D15	SDMMC1_D3	H21
Y4	SD_CardDetect	J21
W13	PB6/SD_PWR_EN	D21
V9	PB10/SD_WP	D20

4.2.15 GPIO

MPU Pin	Function	SiP Pads
B13	PA8 (GPIO/TIM1_CH1)	E18
A11	PA9 (GPIO/TIM1_CH2)	F18
A4	PE13 (GPIO/TIM1_CH3)	G18
Y16	PA11 (GPIO/TIM1_CH4)	H18
B1	PH10 (GPIO/TIM5_CH1)	J18
B3	PH11 (GPIO/TIM5_CH2)	K18
W16	PA12 (GPIO/TIM1_ETR)	D17
W3	PA13 (GPIO/DBTRGI)	E17
R3	PA14 (GPIO/DBTRGO)	F17
F11	PB7 (GPIO/TIM4_CH2)	G17
AB8	PB8 (GPIO/TIM4_CH3)	H17
F12	PB9 (GPIO/TIM4_CH4)	J17
U10	PC0 (GPIO)	K17
U3	PC3 (GPIO)	L17
D13	PC7 (GPIO)	D19
M1	PD8 (GPIO)	E19
M2	PD9 (GPIO)	F19
E9	PE6 (GPIO/TIM1_BKIN2)	G19
F13	PF2 (GPIO)	H19
V3	PF3 (GPIO)	J19
V12	PF10 (GPIO/QSPI_CLK)	K19
W6	PF15 (GPIO)	L19
W4	PG2 (GPIO)	D3
U4	PG3 (GPIO/CAN_STBY)	D4
Y8	PG8 (GPIO/ETH_CLK)	E3
D10	PG15 (GPIO)	E4
A3	PH4 (GPIO)	F3
A2	PH5 (GPIO)	F4
D6	PH8 (GPIO)	G3
E6	PH9 (GPIO)	G4
F5	PH12 (GPIO/TIM5_CH3)	U32

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Table 2 – continued from previous page

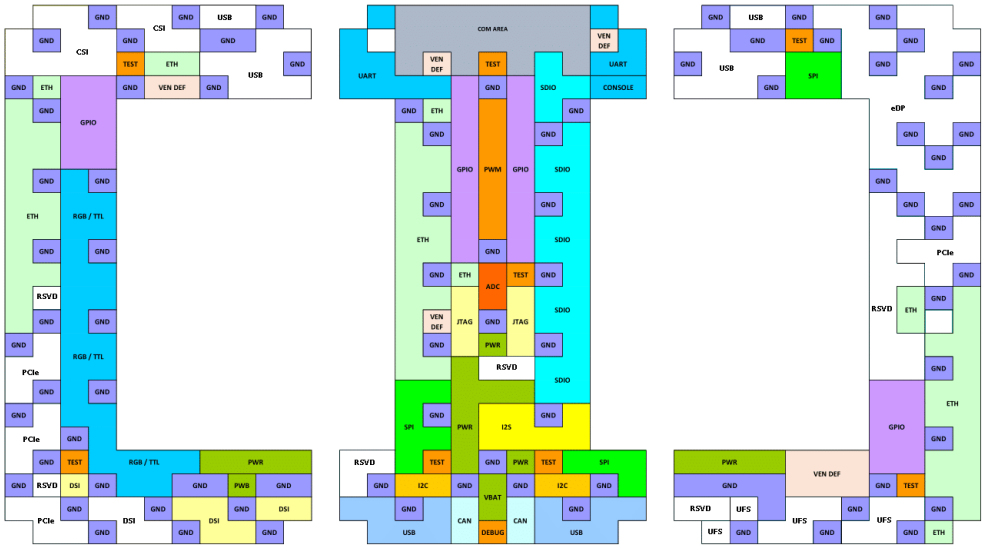
MPU Pin	Function	SiP Pads
C1	PH15 (GPIO/TIM8_CH3N)	U33
J6	PI4 (GPIO/TIM8_BKIN)	V32
F2	PI5 (GPIO/TIM8_CH1)	V33
G5	PI6 (GPIO/TIM8_CH2)	W32
F1	PI7 (GPIO/TIM8_CH3)	W33
J5	PI9 (GPIO)	Y32
T3	PI11 (GPIO)	H3
AA5	PB1 (GPIO/TIM1_CH3N)	Y33
Y11	PG7 (GPIO/UART8_RTS)	W15
AA9	PG10 (GPIO/UART8_CTS)	W16

4.2.16 ADC

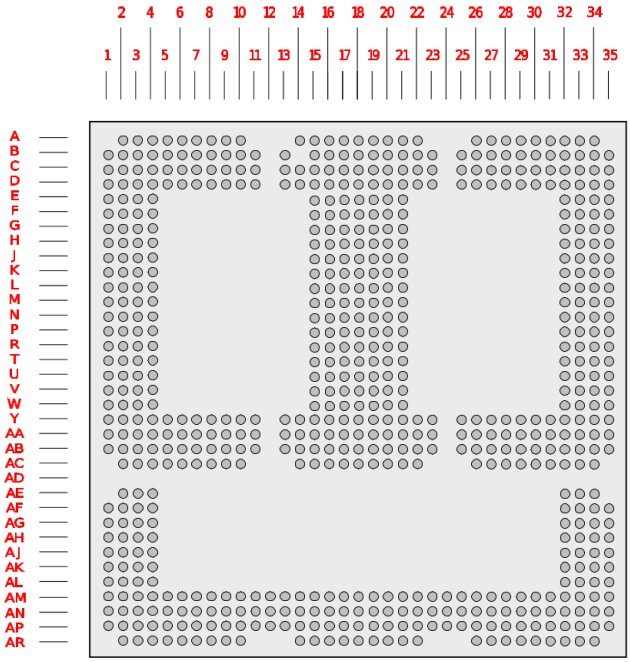
MPU Pin	Function	SiP Pads
R4	ANA0/ADC1_IN0	M18
W8	PF11/ADC1_IN2 (GPIO)	B22
V8	PF12/ADC1_IN6 (GPIO)	C16
AA3	PA0/ADC1_IN16 (GPIO)	P16
U5	PA5/ADC1_IN19 (GPIO)	C6
T5	ANA1/ADC2_IN1	N18
W7	PF13/ADC2_IN2 (GPIO)	C7
W9	PA6/ADC2_IN3 (GPIO)	D6
V7	PF14/ADC2_IN6 (GPIO)	D7
AB5	PB0/ADC2_IN9 (GPIO)	Y29

4.2.17 MSMP1 SiP Pads

4.2.17.1 Contact Groups



4.2.17.2 Contact Grid Numbering



4.2.17.3 Contact Table

MPU Pin	Function	SiP Pads		MPU Pin	Function	SiP Pads
ETHERNET						
AB4	ETH_RGMII_GTX_CLK	J15		AA1	ETH_RGMII_TXD0	H15
AA2	ETH_RGMII_TXD1	G15		Y1	ETH_RGMII_TXD2	H16
Y1	ETH_RGMII_TXD2	H16		Y2	ETH_RGMII_TXD3	G16
Y5	ETH_RGMII_TX_CTL	K16		V4	ETH_RGMII_RX_CLK	R15
AB6	ETH_RGMII_RXDO	K15		AA6	ETH_RGMII_RXD1	L15
V11	ETH_RGMII_RXD2	N15		W2	ETH_RGMII_RXD3	P15
W2	ETH_RGMII_RXD3	P15		W1	ETH_GMII_RX_ER	L16
Y9	ETH_RGMII_RX_CTL	M15		AB7	ETH_GMII_CRS	E16
Y6	ERH_GMII_COL	F15		U8	ETH_RGMII_CLK125	N16
AB3	ETH_MDC	T16		AB2	ETH_MDIO	T15
–	–	H1		–	–	G1
–	–	F1		–	–	G2
–	–	F2		–	–	J2
–	–	P1		–	–	J1
–	–	K1		–	–	M1
–	–	N1		–	–	K2
–	–	L1		–	–	D2
–	–	E1		W5	ETH_MDINT	M2
–	–	N35		–	–	Y35
–	–	AA35		–	–	Y34
–	–	AA34		–	–	V34
–	–	W35		–	–	V35
–	–	U35		–	–	R35
–	–	P35		–	–	U34
–	–	T35		–	–	AC34
–	–	AB35		J4	ETH_PHYINT	R34
CAN						
D3	FDCAN1_TX	AC17		C2	FDCAN1_RX	AB17
V10	FDCAN2_TX	AC19		AA7	FDCAN2_RX	AB19
USB						
AA15	USB2_D_P	AC14		AB15	USB2_D_N	AB13
–	–	AC16		–	–	AB14
–	–	AC15		–	–	AB16
AB14	USB1_D_P	AC22		AA14	USB1_D_N	AB23
–	–	AC20		Y17	OTG_ID (GPIO)	AB22
–	–	AC21		V15	OTG_VBUS	AB20
–	–	D10		–	–	D11
–	–	C10		–	–	D9
–	–	C8		–	–	C9
–	–	A9		–	–	A8
–	–	B11		–	–	B10
–	–	D25		–	–	D26
–	–	C26		–	–	D27
–	–	C28		–	–	C27
–	–	A28		–	–	A27
–	–	B26		–	–	B25

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Table 3 – continued from previous page

MPU Pin	Function	SiP Pads		MPU Pin	Function	SiP Pads
SDIO						
D3	FDCAN1_TX	AC17		C2	FDCAN1_RX	AB17
V10	FDCAN2_TX	AC19		AA7	FDCAN2_RX	AB19
AA15	USB1_D_P	AC14		AB15	USB1_D_N	AB13
–	–	AC16		–	–	AB14
–	–	AC15		–	–	AB16
AB14	USB2_D_P	AC22		AA14	USB2_D_N	AB23
–	–	AC20		Y17	OTG_ID (GPIO)	AB22
–	–	AC21		V15	OTG_VBUS	AB20
–	–	D10		–	–	D11
–	–	C10		–	–	D9
–	–	C8		–	–	C9
–	–	A9		–	–	A8
–	–	B11		–	–	B10
UART						
V13	UART4_RX	D22		U11	UART4_TX	D23
AA11	UART7_RX (SPI5_NSS)	A14		AA10	UART7_TX (SPI5_SCK)	B13
AB10	UART7_RTS (SPI5_MISO)	C13		AB11	UART7_CTS (SPI5_MOSI)	C14
F9	USART2_RX (GPIO)	D14		D9	USART2_TX (GPIO)	D13
C9	USART2_RTS (NAND_NOE)	D15		C4	USART2_CTS (TIM1_BKIN)	D16
–	–	A22		–	–	B23
–	–	C22		–	–	C23
SPI/I2C/I2S						
B9	I2C2_SCL	AA15		E10	I2C2_SDA	AA16
G3	I2C6_SCL	AA20		H3	I2C6_SDA	AA21
E1	I2S2_SDI (TIM8_CH4)	V21		E3	I2S2_SDO (TIM8_ETR)	W21
–	–	V19		–	–	W19
D7	I2S2_MCK (GPIO/UART8_TX)	V18		D1	I2S2_WS (TIM5_CH4)	W18
E2	I2S2_CK (TIM8_BKIN2)	W20		A8	SPI3_MISO	U15
AA8	SPI3_MOSI	V15		AA9	PG10 (GPIO/UART8_CTS)	W16
Y11	PG7 (GPIO/UART8_RTS)	W15		V6	SPI3_NSS	Y15
C5	SPI3_SCK	U16		C12	SPI4_MISO	Y22
B4	SPI4_MOSI	Y23		D5	SPI4_NSS	AA23
E4	SPI4_SCK	Y21		H5	SPI1_MISO	C29
K5	SPI1_MOSI	D30		F4	SPI1_NSS	C30
G2	SPI1_SCK	D29		–	–	–
GPIO/ADC/PWM						
R4	ANA0/ADC1_IN0	M18		T5	ANA1/ADC2_IN1	N18
B13	PA8 (GPIO/TIM1_CH1)	E18		A11	PA9 (GPIO/TIM1_CH2)	F18
A4	PE13 (GPIO/TIM1_CH3)	G18		Y16	PA11 (GPIO/TIM1_CH4)	H18
B1	PH10 (GPIO/TIM5_CH1)	J18		B3	PH11 (GPIO/TIM5_CH2)	K18
W16	PA12 (GPIO/TIM1_ETR)	D17		W3	PA13 (GPIO/DBTRGI)	E17
R3	PA14 (GPIO/DBTRGO)	F17		F11	PB7 (GPIO/TIM4_CH2)	G17
AB8	PB8 (GPIO/TIM4_CH3)	H17		F12	PB9 (GPIO/TIM4_CH4)	J17

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Table 3 – continued from previous page

MPU Pin	Function	SiP Pads		MPU Pin	Function	SiP Pads
U10	PC0 (GPIO)	K17		U3	PC3 (GPIO)	L17
D17	PC7 (GPIO)	D19		M1	PD8 (GPIO)	E19
M2	PD9 (GPIO)	F19		E9	PE6 (GPIO/TIM1_BKIN2)	G19
F13	PF2 (GPIO)	H19		V3	PF3 (GPIO)	J19
V12	PF10 (GPIO/QSPI_CLK)	K19		W6	PF15 (GPIO)	L19
W2	PG2 (GPIO)	D3		U4	PG3 (GPIO/CAN_STBY)	D4
Y8	PG8 (GPIO/ETH_CLK)	E3		D10	PG15 (GPIO)	E4
A3	PH4 (GPIO)	F3		A2	PH5 (GPIO)	F4
D6	PH8 (GPIO)	G3		E6	PH9 (GPIO)	G4
F5	PH12 (GPIO/TIM5_CH3)	U32		C1	PH15 (GPIO/TIM8_CH3N)	U33
J6	PI4 (GPIO/TIM8_BKIN)	V32		F2	PI5 (GPIO/TIM8_CH1)	V33
G5	PI6 (GPIO/TIM8_CH2)	W32		F1	PI7 (GPIO/TIM8_CH3)	W33
J5	PI9 (GPIO)	Y32		AA5	PB1 (GPIO/TIM1_CH3N)	Y33
VENDOR DEFINED PINS						
W8	PF11/ADC1_IN2 (GPIO)	B22		V8	PF12/ADC1_IN6 (GPIO)	C16
AA3	PA0/ADC1_IN16 (GPIO)	P16		U5	PA5/ADC1_IN19 (GPIO)	C6
W7	PF13/ADC2_IN2 (GPIO)	C7		W9	PA6/ADC2_IN3 (GPIO)	D6
V7	PF14/ADC2_IN6 (GPIO)	D7		AB5	PB0/ADC2_IN9 (GPIO)	Y29
N3	BOOT0	Y30		P4	BOOT2	Y31
J2	LCD_R1	AA29		L6	LCD_R2	Y7
K4	LCD_R3	AA6		–	–	–
COM						
M3	PD14 (GPIO/FMC_AD0)	A15		L1	PD15 (GPIO/FMC_AD1)	A16
C10	PD0 (GPIO/FMC_AD2/ I2C5_SDA)	A17		B10	PD1 (GPIO/FMC_AD3/ I2C5_SCL)	A18
W10	PE7 (GPIO/FMC_AD4/ QSPI_BK2_IOO)	A19		Y12	PE8 (GPIO/FMC_AD5/ QSPI_BK2_IO1)	A20
W11	PE9 (GPIO/FMC_AD6/ QSPI_BK2_IO2)	A21		W14	PE10 (GPIO/FMC_AD7/ QSPI_BK2_IO3)	B15
AB9	PD11 (GPIO/FMC_CLE)	B16		W12	PD12 (GPIO/FMC_ALE)	B17
L3	PD6 (GPIO/FMC_NWAIT)	B18		A9	PD5 (GPIO/FMC_NWE)	B19
W15	PG9 (GPIO/FMC_NCE)	B20		F10	USART2_CK (GPIO)	B21
N2	PC13 (RTC_OUT1)	C15		F3	LCD_R0	C17
L4	LCD_G0	C19		B8	LCD_B0	C21
CONFIG/JTAG						
D17	JTAG_TCK	N17		–	JTAG_RTCK	P19
E17	JTAG_TMS	N19		D16	JTAG_TDI	P17
E16	JTAG_TDO	R17		E15	JTAG_nTRST	R19
–	DEBUG_EN	AC18		–	TEST_GENERIC	C18
RGB DISPLAY						
L6	LCD_R2	Y7		K4	LCD_R3	AA6
J1	LCD_R4	Y6		K2	LCD_R5	AA5
K1	LCD_R6	Y5		L5	LCD_R7	Y4
L2	LCD_G2	W4		J3	LCD_G3	V3
K6	LCD_G4	V4		D8	LCD_G5	U3

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Table 3 – continued from previous page

MPU Pin	Function	SiP Pads		MPU Pin	Function	SiP Pads
E7	LCD_G6	T3		E8	LCD_G7	T4
B7	LCD_B2	R4		C7	LCD_B3	R3
B6	LCD_B4	P3		A6	LCD_B5	N3
C6	LCD_B6	N4		A5	LCD_B7	M3
D2	LCD_CLK	M4		H1	LCD_VSYNC	L3
H2	LCD_HSYNC	K3		T4	LCD_BL_CTRL	K4
B5	LCD_DE	J4		R2	NRST	J3
T3	PI11 (GPIO)	H3		–	–	–
MIPI DSI						
A15	DSI_DATA0_N	AB11		B15	DSI_DATA0_P	AB10
A17	DSI_DATA1_N	AC9		B17	DSI_DATA1_P	AC8
–	DSI_DATA2_N	AC6		–	DSI_DATA2_P	AC5
–	DSI_DATA3_N	AB5		–	DSI_DATA3_P	AB4
A16	DSI_CLK_N	AB8		B16	DSI_CLK_P	AB7
V14	PD13/DSI_TE (GPIO)	AA3		–	–	–
MIPI CSI						
–	CSI_DATA0_N	C1		–	CSI_DATA0_P	B1
–	CSI_DATA1_N	A2		–	CSI_DATA1_P	A3
–	CSI_DATA2_N	A5		–	CSI_DATA2_P	A6
–	CSI_DATA3_N	B6		–	CSI_DATA3_P	B7
–	CSI_CLOCK_N	B3		–	CSI_CLOCK_P	B4
–	CAM_MCK	C2		–	I2C-CAM_SDA/CSI_TX_N	C3
–	I2C_CAM_SCL/CSI_TX_P	C4		–	–	–
PCIe						
–	PCIe_A_HSI0_P	AB1		–	PCIe_A_HSI0_N	AB2
–	PCIe_A_HSO0_P	AC2		–	PCIe_A_HSO0_N	AC3
–	PCIe_A_PRSTN	W2		–	PCIe_A_PERST	V2
–	PCIe_REFCLK_P	W1		–	PCIe_REFCLK_N	Y1
–	PCIe_WAKE	T2		–	PCIe_SMDAT	U1
–	PCIe_SMCLK	T1		–	PCIe_SM_ALERT	R2
–	PCIe_B_HSIO_P	L34		–	PCIe_B_HSI0_N	M34
–	PCIe_B_HSO0_P	K35		–	PCIe_B_HSO0_N	L35
–	PCIe_B_PRSNT	K33		–	PCIe_B_PERST	L33
eDP/eDP++						
–	eDP_A_LANE0_P	A30		–	eDP_A_LANE0_N	A31
–	eDP_A_LANE1_P	B31		–	eDP_A_LANE1_N	B32
–	eDP_A_LANE2_P	A33		–	eDP_A_LANE2_N	A34
–	eDP_A_LANE3_P	B34		–	eDP_A_LANE3_N	B35
–	eDP_A_AUX_P	C33		–	eDP_A_AUX_N	C34
–	eDP_A_AUX_SEL	D32		–	eDP_A_BL_HPD	D33
–	eDP_A_BL_EN	D31		–	eDP_A_BL_PWM	C31
–	eDP_B_LANE0_P	D35		–	eDP_B_LANE0_N	E35
–	eDP_B_LANE1_P	E34		–	eDP_B_LANE1_N	F34
–	eDP_B_LANE2_P	G35		–	eDP_B_LANE2_N	H35
–	eDP_B_LANE3_P	H34		–	eDP_B_LANE3_N	J34
–	eDP_B_AUX_P	G33		–	eDP_B_AUX_N	H33
–	eDP_B_AUX_SEL	F32		–	eDP_B_BL_HPD	G32

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Table 3 – continued from previous page

MPU Pin	Function	SiP Pads		MPU Pin	Function	SiP Pads
–	eDP_B_BL_EN	E32		–	eDP_B_BL_PWM	E33
UFS						
–	UFS_TX0_N	AC29		–	UFS_TX0_P	AC28
–	UFS_RX0_N	AC32		–	UFS_RX0_P	AC31
–	UFS_TX1_N	AB30		–	UFS_TX1_P	AB29
–	UFS_RX1_N	AB33		–	UFS_RX1_P	AB32
–	UFS_RESET	AB27		–	UFS_CLK	AC26
PWR						
–	5V	Y17		–	–	Y19
–	–	W17		–	VCC_SD	U18
–	VBAT	AA18		–	VBAT	AB18
–	NRST	U17		T2	CAR_PWR_EN	V17
N4	BOOT1	U19		–	VBUS_OTG	M17
–	VBUS_SW	M19		–	–	Y16
–	3.3V 1.8V	Y20		–	5V	Y8
–	5V	Y9		–	5V	Y10
–	5V	Y11		U1	PWR_LP	Y3
–	–	C5		–	PMIX/PONKEYn	AA9
–	5V	Y25		–	5V	Y26
–	5V	Y27		–	5V	Y28
–	–	AA33		–	–	B29
GND						
–	GND	D18		–	GND	E15
–	GND	E21		–	GND	F16
–	GND	F20		–	GND	J16
–	GND	J20		–	GND	L18
–	GND	M16		–	GND	M20
–	GND	P18		–	GND	A4
–	GND	A7		–	GND	A10
–	GND	B2		–	GND	B5
–	GND	B8		–	GND	B9
–	GND	C11		–	GND	D1
–	GND	D5		–	GND	D8
–	GND	E2		–	GND	H2
–	GND	H4		–	GND	L2
–	GND	L4		–	GND	P2
–	GND	P4		–	GND	A26
–	GND	A29		–	GND	A32
–	GND	B27		–	GND	B28
–	GND	B30		–	GND	B33
–	GND	C25		–	GND	C32
–	GND	C35		–	GND	A10
–	GND	D28		–	GND	D34
–	GND	F33		–	GND	F35
–	GND	G34		–	GND	H32
–	GND	J33		–	GND	R16
–	GND	R20		–	GND	V16
–	GND	V20		–	GND	Y18
–	GND	AA14		–	GND	AA17

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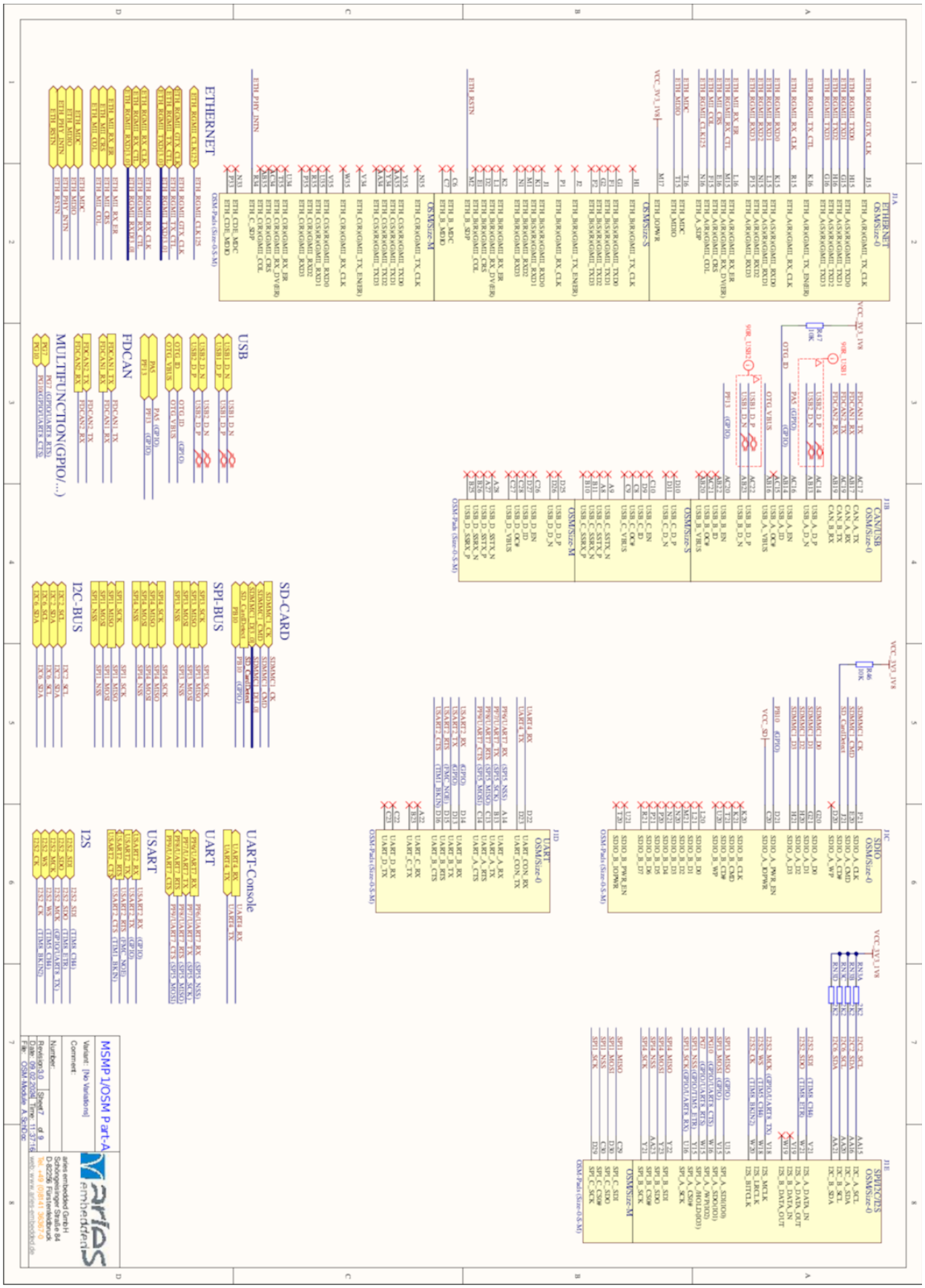
Table 3 – continued from previous page

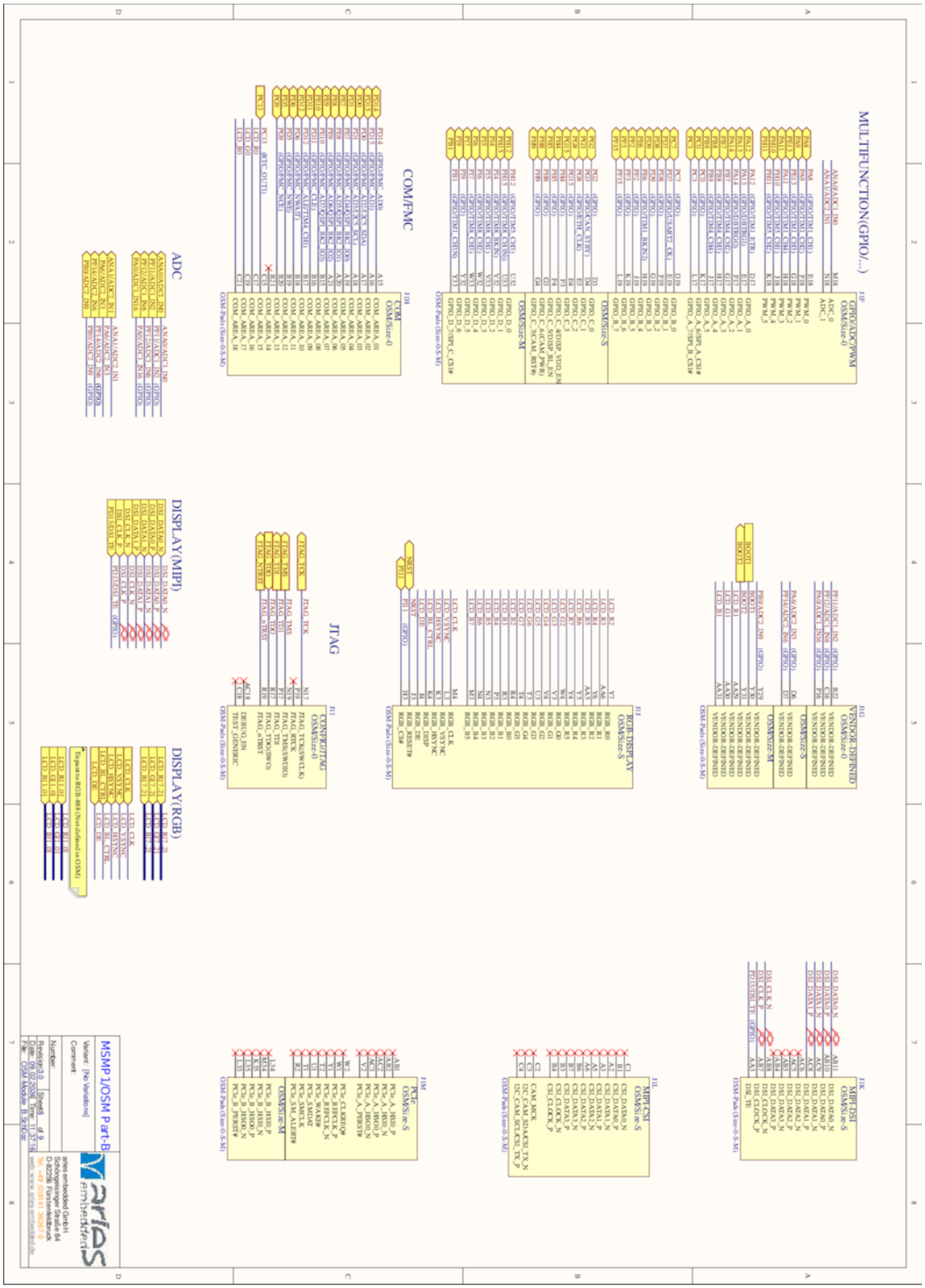
MPU Pin	Function	SiP Pads		MPU Pin	Function	SiP Pads
–	GND	AA19		–	GND	AA22
–	GND	AB15		–	GND	AB21
–	GND	R1		–	GND	U2
–	GND	U4		–	GND	V1
–	GND	W3		–	GND	Y2
–	GND	AA1		–	GND	AA4
–	GND	AA7		–	GND	AA8
–	GND	AA10		–	GND	AA11
–	GND	AB3		–	GND	AB6
–	GND	AB9		–	GND	AC4
–	GND	AC7		–	GND	AC10
–	GND	J35		–	GND	K34
–	GND	M35		–	GND	N34
–	GND	T34		–	GND	W34
–	GND	AA25		–	GND	AA26
–	GND	AA27		–	GND	AA28
–	GND	AA32		–	GND	AB28
–	GND	AB31		–	GND	AB34
–	GND	AC27		–	GND	AC30
–	GND	AC33		–	–	–
RESERVED						
–	RESERVED	R18		–	RESERVED	T17
–	RESERVED	T18		–	RESERVED	T19
–	RESERVED	Y13		–	RESERVED	Y14
–	RESERVED	AA13		–	RESERVED	N2
–	RESERVED	AA2		–	RESERVED	J32
–	RESERVED	K32		–	RESERVED	L32
–	RESERVED	M32		–	RESERVED	M33
–	RESERVED	N32		–	RESERVED	N33
–	RESERVED	P32		–	RESERVED	P33
–	RESERVED	P34		–	RESERVED	R32
–	RESERVED	R33		–	RESERVED	T32
–	RESERVED	T33		–	RESERVED	AB25
–	RESERVED	AB26		–	–	–

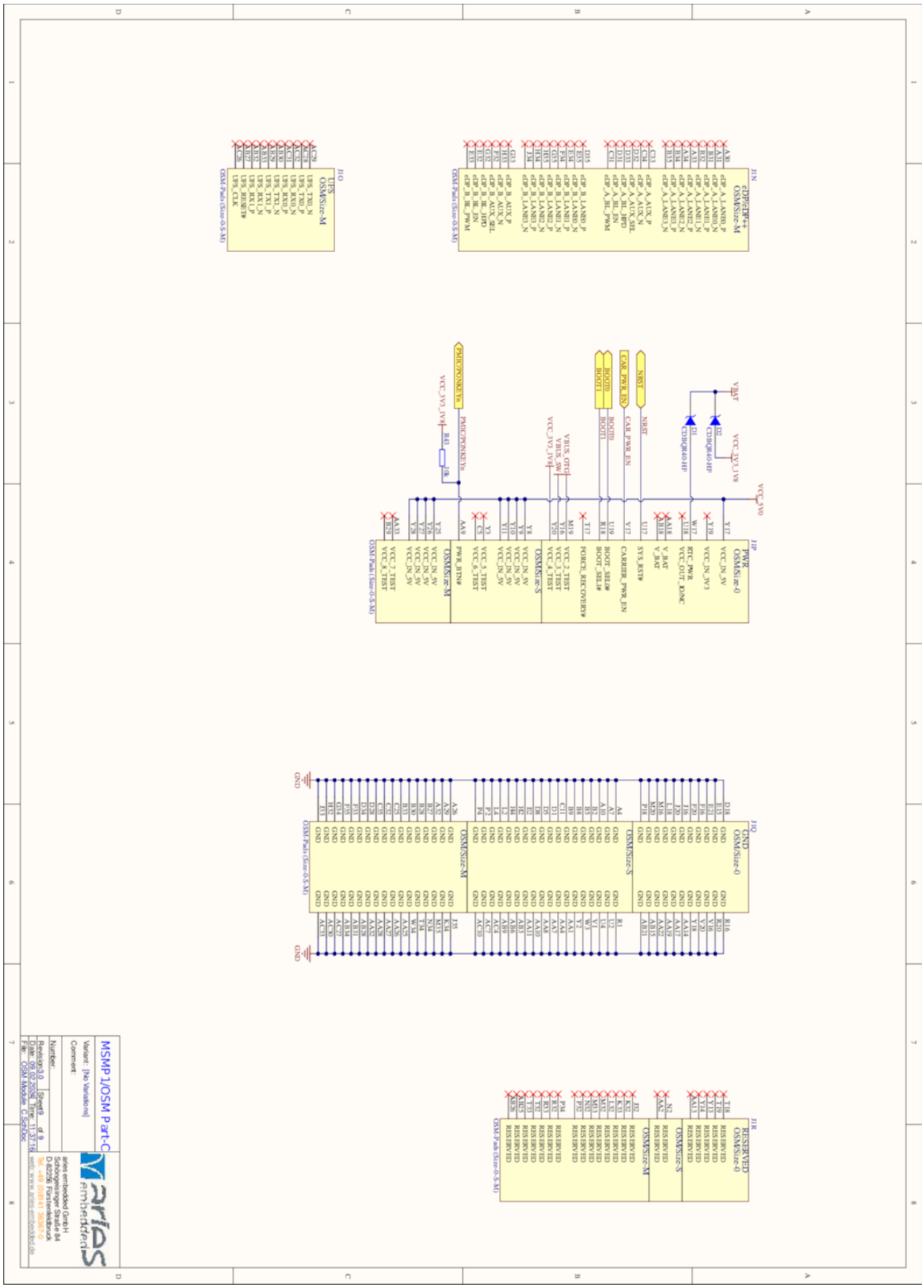
4.3 Schematics

Schematics for the MSMP1 SiP may be obtained on request. Please contact sales@aries-embedded.de.

Below the OSM schematics footprint is shown:


ETHERNET
ETHERNET
OSMSize-0
ETH_ARAVGMII_TX_CLK
ETH_RGMII_GTX_CLK
ETH_RGMII_TXD0
ETH_RGMII_TXD1
ETH_RGMII_TXD2
ETH_RGMII_TXD3
ETH_RGMII_TX_CTL
ETH_RGMII_RX_CLK
ETH_RGMII_RXD0
ETH_RGMII_RXD1
ETH_RGMII_RXD2
ETH_RGMII_RXD3
ETH_MII_RX_ER
ETH_RGMII_RX_CTL
ETH_ARAVGMII_RX_ER
ETH_ARAVGMII_RXD0
ETH_ARAVGMII_RXD1
ETH_ARAVGMII_RXD2
ETH_ARAVGMII_RXD3
ETH_ARAVGMII_RX_DV(ER)
ETH_ARAVGMII_CRS
ETH_ARAVGMII_COL
ETH_A_SDP
ETH_MDC
ETH_MDIO
VCC_3V3_1V8
OSMSize-S
ETH_JOPWR
ETH_BSVRGMII_TX_CLK
ETH_BSVRGMII_TXD0
ETH_BSVRGMII_TXD1
ETH_BSVRGMII_TXD2
ETH_BSVRGMII_TXD3
ETH_BSVRGMII_TX_EN(ER)
ETH_BSVRGMII_RX_CLK
ETH_BSVRGMII_RXD0
ETH_BSVRGMII_RXD1
ETH_BSVRGMII_RXD2
ETH_BSVRGMII_RXD3
ETH_BSVRGMII_RX_DV(ER)
ETH_BSVRGMII_CRS
ETH_BSVRGMII_COL
ETH_B_SDP
ETH_RSTN
ETH_PHY_INTN
ETHERNET
ETH_RGMII_CLK125
ETH_RGMII_GTX_CLK
ETH_RGMII_TXD0
ETH_RGMII_TXD1
ETH_RGMII_TXD2
ETH_RGMII_TXD3
ETH_RGMII_TX_CTL
ETH_RGMII_RX_CLK
ETH_RGMII_RXD0
ETH_RGMII_RXD1
ETH_RGMII_RXD2
ETH_RGMII_RXD3
ETH_MII_RX_ER
ETH_MII_CRS
ETH_MII_COL
ETH_MDC
ETH_MDIO
ETH_PHY_INTN
ETH_RSTN
OSMSize-M
ETH_CRS(RGMII_RX_DV)
ETH_CRS(RGMII_CRS)
ETH_CRS(RGMII_COL)
ETH_CDE_MDC
ETH_CDE_MDIO
ETH_C_SDP
ETH_CRS(RGMII_TX_CLK)
ETH_CRS(RGMII_TXD0)
ETH_CRS(RGMII_TXD1)
ETH_CRS(RGMII_TXD2)
ETH_CRS(RGMII_TXD3)
ETH_CRS(RGMII_TX_EN(ER))
ETH_CRS(RGMII_RX_ER)
ETH_CRS(RGMII_RX_CLK)
ETH_CRS(RGMII_RXD0)
ETH_CRS(RGMII_RXD1)
ETH_CRS(RGMII_RXD2)
ETH_CRS(RGMII_RXD3)
ETH_CRS(RGMII_TX_CLK)
ETH_B_MDC
ETH_B_MDIO
OSMSize-M
ETH_CRS(RGMII_TX_CLK)
CAN/USB
OSMSize-0
FDCAN1_TX
FDCAN1_RX
FDCAN2_TX
FDCAN2_RX
CAN_A_TX
CAN_A_RX
CAN_B_TX
CAN_B_RX
USB_A_DP
USB_A_DN
USB_A_ID
USB_A_OC#
USB_A_VBUS
USB_B_DP
USB_B_DN
USB_B_ID
USB_B_OC#
USB_B_VBUS
OTG_VBUS
PA5 (GPIO)
PB13 (GPIO)
USB1_D_P
USB1_D_N
USB2_D_P
USB2_D_N
OSMSize-S
USB_C_DP
USB_C_DN
USB_C_ID
USB_C_OC#
USB_C_VBUS
OSMSize-M
USB_D_DP
USB_D_DN
USB_D_ID
USB_D_OC#
USB_D_VBUS
USB_C_SSTX_N
USB_C_SSTX_P
USB_C_SSRX_N
USB_C_SSRX_P
USB_D_SSTX_N
USB_D_SSTX_P
USB_D_SSRX_N
USB_D_SSRX_P
OSM Pads (Size-0-S-M)
SDIO
OSMSize-0
SDMMC1_CK
SDMMC1_CMD
SDMMC1_D0
SDMMC1_D1
SDMMC1_D2
SDMMC1_D3
SD_CardDetect
SD_CardDetect
PB10 (GPIO)
SDIO_A_CLK
SDIO_A_CMD
SDIO_A_D0
SDIO_A_D1
SDIO_A_D2
SDIO_A_D3
SDIO_A_CD#
SDIO_A_WP
SDIO_A_IOPWR
SDIO_B_CLK
SDIO_B_CMD
SDIO_B_D0
SDIO_B_D1
SDIO_B_D2
SDIO_B_D3
SDIO_B_D4
SDIO_B_D5
SDIO_B_D6
SDIO_B_D7
SDIO_B_PWR_EN
SDIO_B_IOPWR
OSM Pads (Size-0-S-M)
SPI/I2C/I2S
OSMSize-0
I2C_A_SCL
I2C_A_SDA
I2C_B_SCL
I2C_B_SDA
I2S2_SDI (TIM15_CH1)
I2S2_SDO (TIM15_ETR)
I2S2_MCK (GPIO)/UART8_TX)
I2S2_CK (TIM15_BKIN2)
I2S_A_DATA_IN
I2S_A_DATA_OUT
I2S_B_DATA_IN
I2S_B_DATA_OUT
I2S_MCLK
I2S_LRCLK
I2S_BITCLK
SPI_A_SDI(IO0)
SPI_A_SDO(IO1)
SPI_A_WP/IO2)
SPI_A_HOLD/IO3)
SPI_A_CS#
SPI_A_SCK
SPI_B_SDI
SPI_B_SDO
SPI_B_CS#
SPI_B_SCK
OSMSize-M
SPI_C_SDI
SPI_C_SDO
SPI_C_CS#
SPI_C_SCK
SPI1_MISO (GPIO)
SPI1_MOSI
SPI1_NSS
SPI1_SCK
SPI4_MISO
SPI4_MOSI
SPI4_NSS
SPI4_SCK
PG10 (GPIO)/UART5_CTS)
SPI5_NSS (GPIO)/TIM5_ETR)
SPI5_SCK (GPIO)/UART8_RTS)
PG7 (GPIO)/UART6_TX)
PG8 (GPIO)/UART6_RX)
PB15 (GPIO)/UART4_RTS)
PB14 (GPIO)/UART4_CTS)
PB9 (GPIO)/UART4_TX)
PB8 (GPIO)/UART4_RX)
RSVA
RSVB
RSVC
RSVD
RSVE
RSVF
RSVG
RSVH
UART-Console
UART
OSMSize-0
UART4_RX
UART4_TX
UART
OSMSize-0
UART_CON_RX
UART_CON_TX
UART_A_RX
UART_A_TX
UART_A_RTS
UART_A_CTS
UART_B_RX
UART_B_TX
UART_B_RTS
UART_B_CTS
UART_C_RX
UART_C_TX
UART_D_RX
UART_D_TX
OSM Pads (Size-0-S-M)
SD-CARD
SDMMC1_CK
SDMMC1_CMD
SDMMC1_D0
SDMMC1_D1
SDMMC1_D2
SDMMC1_D3
SD_CardDetect
PB10 (GPIO)
SPI-BUS
SPI1_SCK
SPI1_MISO
SPI1_MOSI
SPI1_NSS
SPI4_SCK
SPI4_MISO
SPI4_MOSI
SPI4_NSS
I2C-BUS
I2C2_SCL
I2C2_SDA
I2C4_SCL
I2C4_SDA
I2C5_SCL
I2C5_SDA
FDCAN
FDCAN1_TX
FDCAN1_RX
FDCAN2_TX
FDCAN2_RX
PA5
PB13
USB
USB1_D_N
USB1_D_P
USB2_D_N
USB2_D_P
OTG_ID
OTG_VBUS
MULTIFUNCTION(GPIO/...)
PG12
PG8 (GPIO)/UART6_RX)
PG7 (GPIO)/UART6_TX)
PG10 (GPIO)/UART5_CTS)
USART
USART2_RX (GPIO)
USART2_TX (GPIO)
USART2_RTS (DMC_WR)
USART2_CTS (TIM2_BKIN)
UART
PB8(UART4_RX (SPI5_NSS)
PB9(UART4_TX (SPI5_SCK)
PB14(UART4_RTS (SPI5_MISO)
PB15(UART4_CTS (SPI5_MOSI)
I2S
I2S2_SDI (TIM15_CH1)
I2S2_SDO (TIM15_ETR)
I2S2_MCK (GPIO)/UART8_TX)
I2S2_WS (TIM15_CH1)
I2S2_CK (TIM15_BKIN2)
MSMP1/OSM Part-A
Variant: [No Variation]
Comment
Number
Revision:3.0
Sheet 7 of 9
Date: 06.02.2024 Time: 11:37:16
File: OSM-Module_A.SchDoc
aries embedded GmbH
Schloppenringer Straße 84
D-82256 Fürstenfeldbruck
Tel.: +49 (0)8141 360367-0
web: www.aries-embedded.de


MULTIFUNCTION(GPIO/...)
GPIO/ADC/PWM
OSM-Size-0
VENDOR-DEFINED
OSM-Size-M
COM/FMC
COM
OSM-Size-0
ADC
ADC
DISPLAY(MIPI)
DISPLAY(RGB)
JTAG
CONFIG/JTAG
RGB-DISPLAY
OSM-Size-S
MIPI-CSI
OSM-Size-S
MIPI-DSI
OSM-Size-S
PCIe
OSM-Size-E
MSMP1/OSM Part-B
Variant: [No Variation]
Comment
Number:
Revision:3.0
Sheet 8 of 9
Date: 09.12.2024 Time: 11:37:16
File: OSM-Module_B_3x3.dsn
aries embedded GmbH
Schlipsheimer Straße 84
D-82256 Fürstenfeldbruck
Tel.:+49 (0)8141 360671-0
web: www.aries-embedded.de


MSMP1/OSM Part-G
aries embedded GmbH
Schoppenlanger Straße 84
D-82256 Fürstenfeldbruck
Tel.: +49 (0)8141 360367-0
web: www.aries-embedded.de
Variant: [No Variation]
Comment
Number:
Revision:3.0
Sheet 9 of 9
Date: 09.02.2021 Time: 11:37:16
File: OSM-Module G.SchDoc
J1N
J1O
J1P
J1Q
J1R
VCC_5V0
VBAT
NRST
BOOT0
BOOT1
CARR_PWR_EN
PMIC_PENIRQ_N
GND