A5G21H605W19N

Airfast RF Power GaN Transistor

Rev. 1 — 21 December 2023 Product data sheet

This 85 W asymmetrical Doherty RF power GaN transistor is designed for cellular base station applications requiring very wide instantaneous bandwidth capability covering the frequency range of 2110 to 2200 MHz.

This part is characterized and performance is guaranteed for applications operating in the 2110 to 2200 MHz band. There is no guarantee of performance when this part is used in applications designed outside of these frequencies.

2100 MHz

- Typical Doherty Single−Carrier W−CDMA Reference Circuit Performance: V_{DD} = 48 Vdc, I_{DQA} = 300 mA, V_{GSB} = −5.0 Vdc, P_{out} = 85 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. (1)

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
2110 MHz	16.3	56.1	8.9	−26.3
2140 MHz	16.5	57.6	8.6	−27.3
2170 MHz	16.2	57.1	8.2	−28.9

1. All data measured with device soldered to NXP reference circuit.

Features

- High terminal impedances for optimal broadband performance
- Advanced high performance in−package Doherty
- Improved linearized error vector magnitude with next generation signal
- Able to withstand extremely high output VSWR and broadband operating conditions
- Plastic package

A5G21H605W19N

2110–2200 MHz, 85 W Avg., 48 V AIRFAST RF POWER GaN TRANSISTOR

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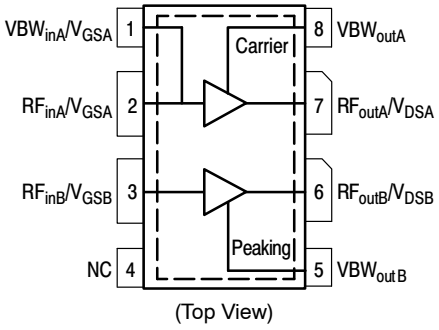


(Top View)

Note: Exposed backside of the package is the source terminal for the transistor.

Figure 1. Pin Connections

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain−Source Voltage	V_{DSS}	125	Vdc
Gate−Source Voltage	V_{GS}	−16, 0	Vdc
Operating Voltage	V_{DD}	55	Vdc
Maximum Forward Gate Current, $I_{G\ (A+B)}$, @ T_C = 25°C	I_{GMAX}	90	mA
Storage Temperature Range	T_{stg}	−65 to +150	°C
Case Operating Temperature Range	T_C	−55 to +150	°C
Maximum Channel Temperature	T_{CH}	225	°C

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Value	Unit
Operating Voltage	V_{DD}	48	Vdc

Table 3. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance by Infrared Measurement, Active Die Surface−to−Case Case Temperature 124°C, P_D = 95 W	$R_{\theta SC}$ (IR)	0.46 (1)	°C/W
Thermal Resistance by Finite Element Analysis, Channel−to−Case Case Temperature 124°C, P_D = 94.8 W	$R_{\theta CHC}$ (FEA)	0.8 (2)	°C/W

Table 4. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JS−001−2017)	2
Charge Device Model (per JS−002−2014)	C3

Table 5. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22−A113, IPC/JEDEC J−STD−020	3	245	°C

Table 6. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Off Characteristics (3)						
Off−State Drain Leakage		$I_{D(BR)}$				mAdc
(V_{DS} = 150 Vdc, V_{GS} = −8 Vdc)	Carrier		—	—	13.2	
(V_{DS} = 150 Vdc, V_{GS} = −8 Vdc)	Peaking		—	—	26.4	
On Characteristics — Side A, Carrier						
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 30 mAdc)		$V_{GS(th)}$	−4.6	−2.6	−1.9	Vdc
Gate Quiescent Voltage (V_{DD} = 48 Vdc, I_{DA} = 300 mAdc, Measured in Functional Test)		$V_{GSA(Q)}$	−3.1	−2.6	−2.1	Vdc
On Characteristics — Side B, Peaking						
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 60 mAdc)		$V_{GS(th)}$	−4.6	−2.6	−1.9	Vdc

1. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.
2. $R_{\theta CHC}$ (FEA) must be used for purposes related to reliability and limitations on maximum channel temperature. MTTF may be estimated by the expression MTTF (hours) = $10^{[A + B/(T + 273)]}$, where T is the channel temperature in degrees Celsius, A = −11.6 and B = 9129.
3. Each side of device measured separately.

(continued)

Table 6. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (1) (In NXP Doherty Production Test Fixture, 50 ohm system) V_{DD} = 48 Vdc, I_{DQA} = 300 mA, V_{GSB} = (V_t – 1.87) Vdc, P_{out} = 85 W Avg., f = 2140 MHz, Single–Carrier W–CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	13.7	15.1	18.0	dB
Drain Efficiency	η_D	48.0	55.3	—	%
Saturated Power (Pulsed CW, 5% Duty Cycle)	P_{sat}	56.6	57.9	—	dBm
Adjacent Channel Power Ratio	ACPR	—	–29.6	–22.0	dBc
Wideband Ruggedness (In NXP Doherty Production Test Fixture, 50 ohm system) I_{DQA} = 300 mA, V_{GSB} = –4.5 Vdc, f = 2140 MHz, Additive White Gaussian Noise (AWGN) with 10 dB PAR					
ISBW of 400 MHz at 55 Vdc, 123 W Avg. Modulated Output Power (3 dB Input Overdrive from 85 W Avg. Modulated Output Power)	No Device Degradation				
Typical Performance (In NXP Doherty Fixture, 50 ohm system) V_{DD} = 48 Vdc, I_{DQA} = 300 mA, V_{GSB} = –4.8 Vdc, 2110–2170 MHz Bandwidth					
Pulsed CW, 10% Duty Cycle					
Saturated Power (2)	P_{sat}	—	676	—	W
AM/PM (2) (Maximum value measured at saturated power across the 2110–2170 MHz bandwidth)	Φ	—	–25	—	°
Gain Variation @ Avg. Power over Temperature (–40°C to +85°C) (3)	ΔG	—	0.016	—	dB/°C
Output Power Variation @ Saturated Power over Temperature (–40°C to +85°C) (3)	ΔP_{sat}	—	0.0035	—	dB/°C
Single–Carrier W–CDMA, Unclipped					
Gain Flatness in 60 MHz Bandwidth @ P_{out} = 85 W Avg. (2)	G_F	—	1.5	—	dB
2–Tone CW					
VBW Resonance Point (2) (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	240	—	MHz

Table 7. Ordering Information

Device	Tape and Reel Information	Package
A5G21H605W19NR3	R3 Suffix = 250 Units, 44 mm Tape Width, 13–inch Reel	OM–780–4S4S

1. Internally matched part.
2. All data measured with device soldered to NXP characterization fixture.
3. All data measured in NXP production fixture.

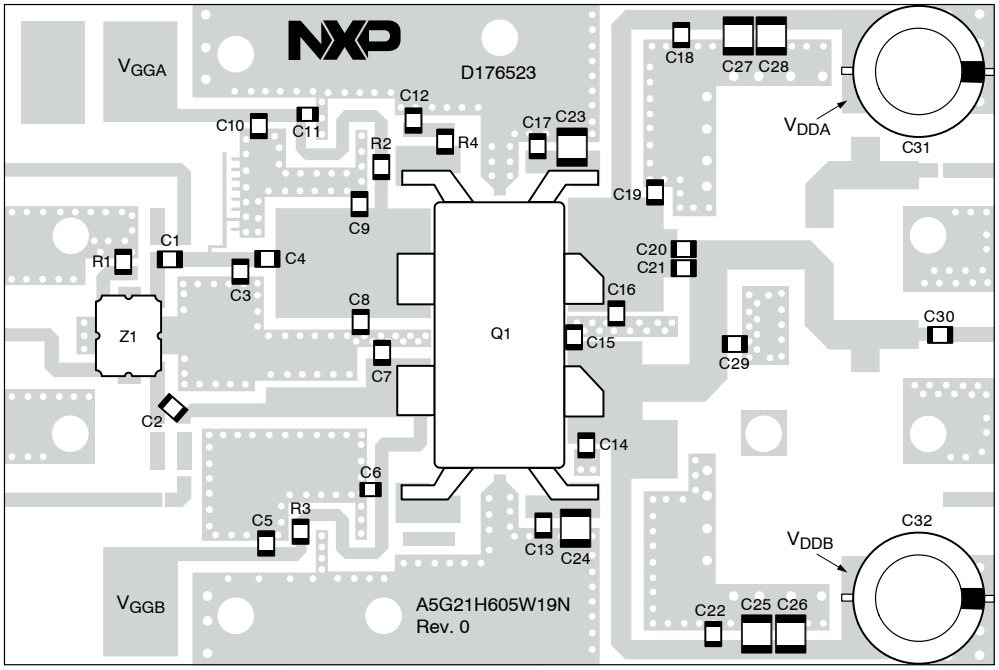
Correct Biasing Sequence for GaN Depletion Mode Transistors in a Doherty Configuration

Bias ON the device

1. Set gate voltage V_{GSA} and V_{GSB} to –5 V.
2. Set drain voltage V_{DSA} and V_{DSB} to nominal supply voltage (+48 V).
3. Increase V_{GSA} (carrier side) until I_{DQA} current is attained.
4. Increase V_{GSB} (peaking side) to target bias voltage.
5. Apply RF input power to desired level.

Bias OFF the device

1. Disable RF input power.
2. Adjust gate voltage V_{GSA} and V_{GSB} to –5 V.
3. Adjust drain voltage V_{DSA} and V_{DSB} to 0 V. Allow adequate time for drain voltage to reduce to 0 V from external drain capacitors.
4. Disable V_{GSA} and V_{GSB}.



Note: All data measured with device soldered to NXP reference circuit.

aaa−051314

Figure 2. A5G21H605W19N Reference Circuit Component Layout — 2.0″ (5.1 cm) × 3.0″ (7.6 cm)

Table 8. A5G21H605W19N Reference Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2, C4, C13, C17, C18, C22	12 pF Chip Capacitor	GQM2195C2E120FB12D	Murata
C3	0.8 pF Chip Capacitor	600F0R8BT250XT	ATC
C5, C10, C12	1.0 μF Chip Capacitor	GJ821BR71H105KA12L	Murata
C6, C11	12 pF Chip Capacitor	GQM1875C2E120FB12D	Murata
C7	0.75 pF Chip Capacitor	GQM2195C2ER75BB12D	Murata
C8	1.0 pF Chip Capacitor	600F1R0BT250XT	ATC
C9, C19	0.5 pF Chip Capacitor	GQM2195C2ER50BB12D	Murata
C14	0.8 pF Chip Capacitor	GQM2195C2ER80BB12D	Murata
C15	1.8 pF Chip Capacitor	600F1R8BT250XT	ATC
C16	0.2 pF Chip Capacitor	600F0R2BT250XT	ATC
C20	1.1 pF Chip Capacitor	600F1R1BT250XT	ATC
C21	1.2 pF Chip Capacitor	600F1R2BT250XT	ATC
C23, C24, C25, C26, C27, C28	10 μF Chip Capacitor	C3225X7S1H106K	TDK
C29	0.3 pF Chip Capacitor	600F0R3BT250XT	ATC
C30	12 pF Chip Capacitor	600F120JT250XT	ATC
C31, C32	470 μF, 100 V Electrolytic Capacitor	MCGPR100V477M16X32	Multicomp
Q1	RF Power GaN Transistor	A5G21H605W19N	NXP
R1	50 Ω, 8 W Termination Chip Resistor	C8A50Z4B	Anaren
R2, R3	3.3 Ω, 1/8 W Chip Resistor	CRCW08053R30NEA	Vishay
R4	10 Ω, 1/8 W Chip Resistor	RK73H2ATTS10R0F	KOA Speer
Z1	1800–2300 MHz, 90°, 3 dB Hybrid Coupler	X3C21P1−03S	Anaren
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D176523	MTL

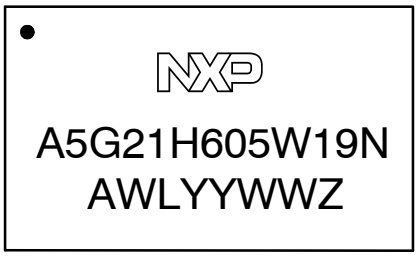


Figure 3. Product Marking

Table 9. Product Marking Trace Code

Identifier	Description
A	Assembly location
WL	Wafer lot indicator
YYWW	Date code
Z	Assembly lot

Package Information

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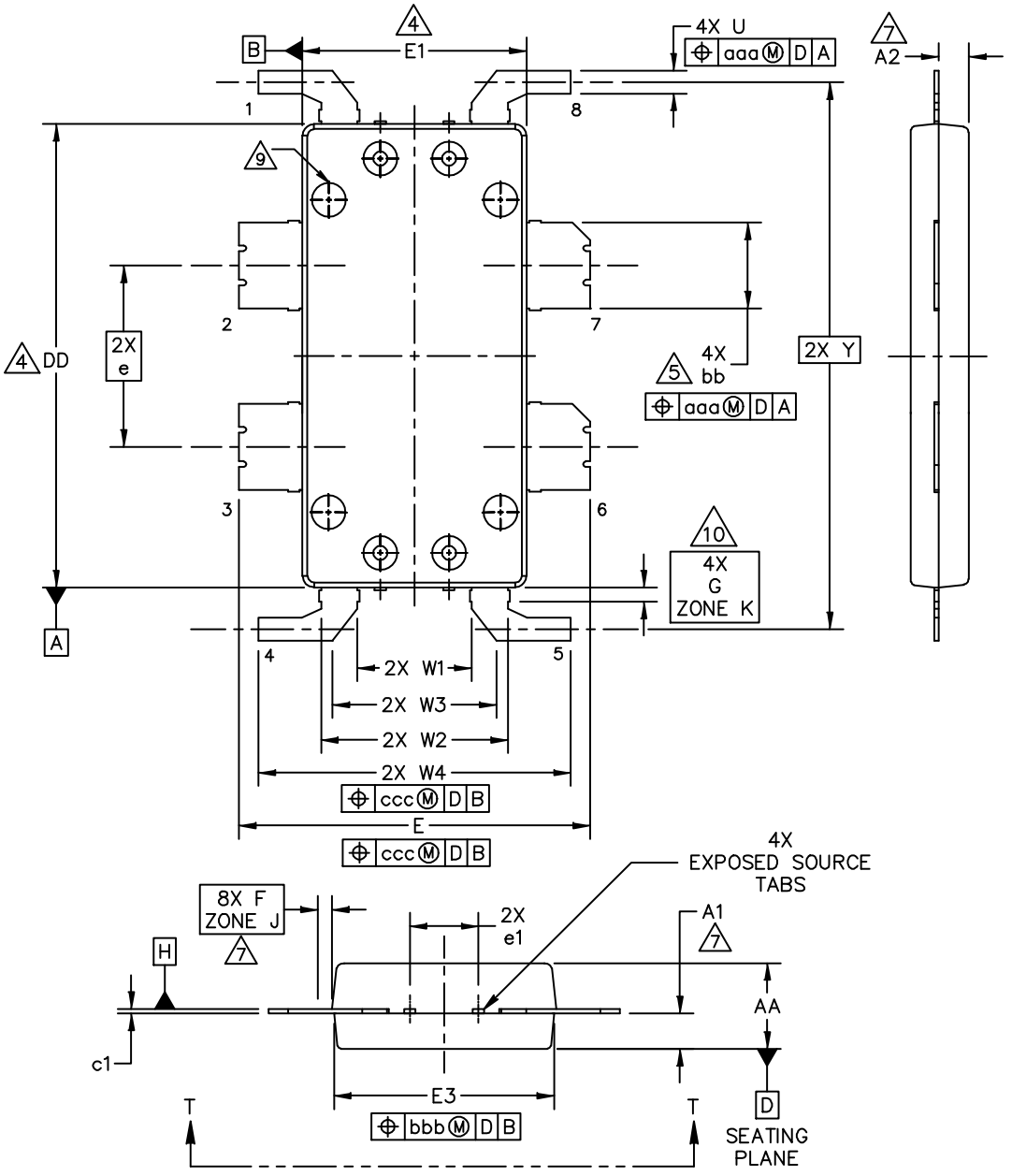

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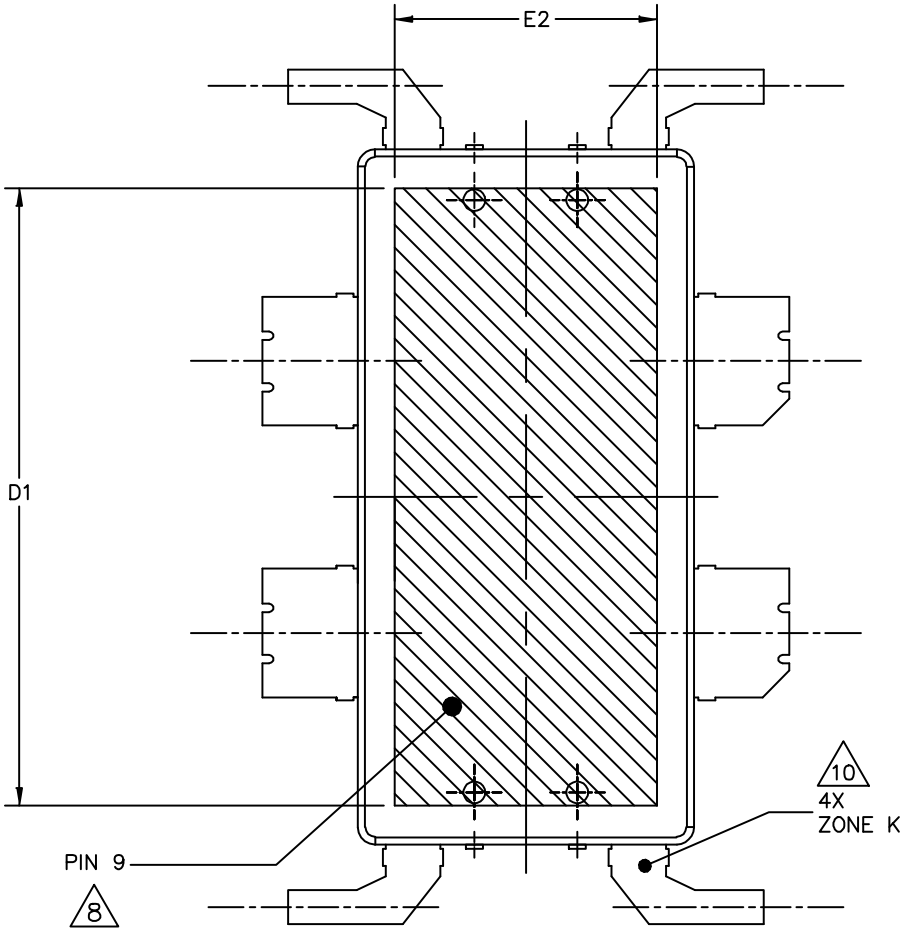

BOTTOM VIEW
VIEW T−T

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NOTES:
1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

3. DATUM PLANE H IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS DD AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS DD AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

5. DIMENSION bb DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

7. DIMENSIONS A1 AND A2 APPLIES WITHIN ZONE J ONLY. A1 APPLIES TO PINS 2, 3, 6 AND 7. A2 APPLIES TO PINS 1, 4, 5 AND 8.

8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. THE DIMENSIONS D1 AND E2 REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF HEAT SLUG.

9. DIMPLED HOLE REPRESENTS INPUT SIDE.

10. ZONE K REPRESENTS NON-SOLDERABLE REGION WHERE MOLD FLASH AND RESIN BLEED ARE PERMITTED ON BOTH SIDES OF THE LEADS.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
AA	.148	.152	3.76	3.86	W2	.321	.331	8.15	8.41
A1	.059	.065	1.50	1.65	W3	.281	.291	7.14	7.39
A2	.056	.068	1.42	1.73	W4	.538	.554	13.67	14.07
DD	.808	.812	20.52	20.62	U	.037	.043	0.94	1.09
D1	.720	----	18.29	----	Y	.956 BSC		24.28 BSC	
E	.610	.618	15.49	15.70	bb	.147	.153	3.73	3.89
E1	.390	.394	9.91	10.01	c1	.007	.011	0.18	0.28
E2	.306	----	7.77	----	e	.317 BSC		8.05 BSC	
E3	.383	.387	9.73	9.83	e1	.116	.124	2.95	3.15
F	.025 BSC		0.64 BSC		aaa	.004		0.10	
G	.030 BSC		0.76 BSC		bbb	.006		0.15	
W1	.195	.205	4.95	5.21	ccc	.010		0.25	

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Product Documentation, Software and Tools

Refer to the following resources to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Software

- .s2p File

Development Tools

- Printed Circuit Boards

Revision History

The following table summarizes revisions to this document.

Revision	Date	Description
0	14 August 2023	• Initial release of data sheet
1	21 December 2023	• Table 5, Moisture Sensitivity Level: package peak temperature updated to reflect actual test data, p. 2

Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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