G3R60MT07J
750 V 60 mΩ SiC MOSFET

GeneSiC™ SEMICONDUCTOR

Silicon Carbide MOSFET
N-Channel Enhancement Mode

|		
V_{DS}	=	750 V
$R_{DS(ON)(Typ.)}$	=	60 mΩ
$I_{D(T_C = 100°C)}$	=	31 A

Features

- G3R™ Technology with +15 V Gate Drive
- Softer $R_{DS(ON)}$ v/s Temperature Dependency
- LoRing™ - Electromagnetically Optimized Design
- Smaller $R_{G(INT)}$ and Lower Q_G
- Low Device Capacitances (C_{OSS}, C_{RSS})
- Superior Cost-Performance Index
- Robust Body Diode with Low V_F and Low Q_{RR}
- 100% Avalanche (UIL) Tested

Package

Case (D)
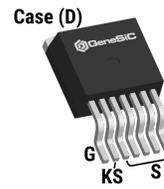
TO-263-7
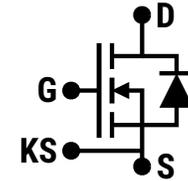
D = Drain
G = Gate
S = Source
KS = Kelvin Source

RoHS

REACH

Advantages

- Compatible with Commercial Gate Drivers
- Low Conduction Losses at all Temperatures
- Reduced Ringing
- Faster and More Efficient Switching
- Lesser Switching Spikes and Lower Losses
- Better Power Density and System Efficiency
- Ease of Paralleling without Thermal Runaway
- Superior Robustness and System Reliability

Applications

- Solar (PV) Inverters
- Server & Telecom Power Supplies
- Uninterruptible Power Supplies (UPS)
- EV / HEV Charging
- DC-DC Converters
- Switched Mode Power Supplies (SMPS)
- Energy Storage and Battery Charging
- Class D Amplifiers

Absolute Maximum Ratings (At T_C = 25°C Unless Otherwise Stated)

Parameter	Symbol	Conditions	Values	Unit	Note
Drain-Source Voltage	$V_{DS(max)}$	V_{GS} = 0 V, I_D = 100 µA	750	V	
Gate-Source Voltage (Dynamic)	$V_{GS(max)}$		-10 / +20	V	
Gate-Source Voltage (Static)	$V_{GS(op)}$	Recommended Operation	-5 / +15	V	
Continuous Forward Current	I_D	T_C = 25°C, V_{GS} = -5 / +15 V	44	A	Fig. 15
		T_C = 100°C, V_{GS} = -5 / +15 V	31		
		T_C = 135°C, V_{GS} = -5 / +15 V	23		
Pulsed Drain Current	$I_{D(pulse)}$	t_P ≤ 3µs, D ≤ 1%, V_{GS} = 15 V, Note 1	100	A	Fig. 14
Power Dissipation	P_D	T_C = 25°C	182	W	Fig. 16
Non-Repetitive Avalanche Energy	E_{AS}	L = 7.5 mH, I_{AS} = 7.5 A	210	mJ	
Operating and Storage Temperature	T_j , T_{stg}		-55 to 175	°C	

Thermal/Package Characteristics

Parameter	Symbol	Conditions	Values			Unit	Note
			Min.	Typ.	Max.		
Thermal Resistance, Junction - Case	R_{thJC}			0.69	0.82	°C/W	Fig. 13
Weight	W_T			1.45		g	

Note 1: Pulse Width t_P Limited by $T_{j(max)}$

Electrical Characteristics (At T_C = 25°C Unless Otherwise Stated)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
Drain-Source Breakdown Voltage	V_{DSS}	V_{GS} = 0 V, I_D = 100 µA	750			V	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 750 V, V_{GS} = 0 V		1		µA	
Gate Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V			100	nA	
		V_{DS} = 0 V, V_{GS} = -10 V			-100		
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 8.0 mA	1.8	2.50		V	Fig. 9
		V_{DS} = V_{GS}, I_D = 8.0 mA, T_j = 175°C		2.00			
Transconductance	g_{fs}	V_{DS} = 10 V, I_D = 15 A		7.8		S	Fig. 4
		V_{DS} = 10 V, I_D = 15 A, T_j = 175°C		8.6			
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS} = 15 V, I_D = 15 A		60	78	mΩ	Fig. 5-8
		V_{GS} = 15 V, I_D = 15 A, T_j = 175°C		72			
Input Capacitance	C_{iss}			953			
Output Capacitance	C_{oss}			90		pF	Fig. 11
Reverse Transfer Capacitance	C_{rss}			7.9			
C_{oss} Stored Energy	E_{oss}	V_{DS} = 450 V, V_{GS} = 0 V		10		µJ	Fig. 12
C_{oss} Stored Charge	Q_{oss}	f = 1 MHz, V_{AC} = 25mV		59		nC	
Effective Output Capacitance (Energy Related)	$C_{o(er)}$			98		pF	Note 2
Effective Output Capacitance (Time Related)	$C_{o(tr)}$			131			
Gate-Source Charge	Q_{gs}	V_{DS} = 450 V, V_{GS} = -5 / +15 V		13		nC	Fig. 10
Gate-Drain Charge	Q_{gd}	I_D = 15 A		16			
Total Gate Charge	Q_g	Per IEC607478-4		47			
Internal Gate Resistance	$R_{G(int)}$	f = 1 MHz, V_{AC} = 25 mV		1.0		Ω	
Turn-On Switching Energy (Body Diode)	E_{On}	T_j = 25°C, V_{GS} = -5/+15V, $R_{G(ext)}$ = 3 Ω, L = 60.0 µH, I_D = 15 A, V_{DD} = 450 V		30		µJ	Fig. 22,26
Turn-Off Switching Energy (Body Diode)	E_{Off}			4			
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 450 V, V_{GS} = -5/+15V $R_{G(ext)}$ = 3 Ω, L = 60.0 µH, I_D = 15 A Timing relative to V_{DS}, Inductive load		12		ns	Fig. 24
Rise Time	t_r			6			
Turn-Off Delay Time	$t_{d(off)}$			7			
Fall Time	t_f			4			

*The chip technology was characterized up to 200 V/ns. The measured dV/dt was limited by measurement test setup and package.

Note 2: $C_{o(er)}$, a lumped capacitance that gives same stored energy as C_{OSS} while V_{DS} is rising from 0 to 450V.
$C_{o(tr)}$, a lumped capacitance that gives same charging times as C_{OSS} while V_{DS} is rising from 0 to 450V.

Reverse Diode Characteristics

Parameter	Symbol	Conditions	Values			Unit	Note
			Min.	Typ.	Max.		
Diode Forward Voltage	V_{SD}	V_{GS} = -5 V, I_{SD} = 7 A		4.4		V	Fig. 17-18
		V_{GS} = -5 V, I_{SD} = 7 A, T_j = 175°C		3.9			
Continuous Diode Forward Current	I_S	V_{GS} = -5 V, T_c = 100°C	16			A	
Diode Pulse Current	$I_{S(pulse)}$	V_{GS} = -5 V, Note 1		64		A	
Reverse Recovery Time	t_{rr}	V_{GS} = -5 V, I_{SD} = 15 A, V_R = 450 V dif/dt = 800 A/μs, T_j = 25°C		24		ns	
Reverse Recovery Charge	Q_{rr}			102		nC	
Peak Reverse Recovery Current	I_{rrm}			6		A	
Reverse Recovery Time	t_{rr}	V_{GS} = -5 V, I_{SD} = 15 A, V_R = 450 V dif/dt = 800 A/μs, T_j = 175°C		26		ns	
Reverse Recovery Charge	Q_{rr}			155		nC	
Peak Reverse Recovery Current	I_{rrm}			9		A	

Figure 1: Output Characteristics (T$_j$ = 25°C)
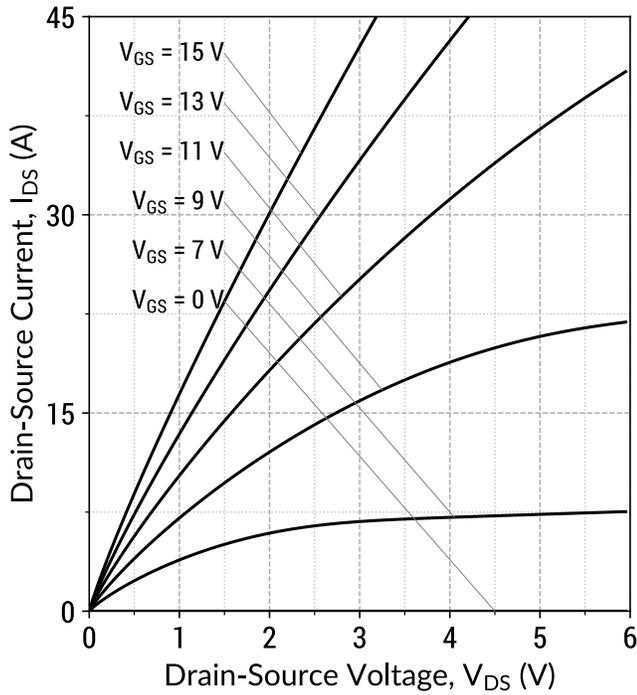
$I_D = f(V_{DS}, V_{GS})$; t$_P$ = 250 μs

Figure 2: Output Characteristics (T$_j$ = 175°C)
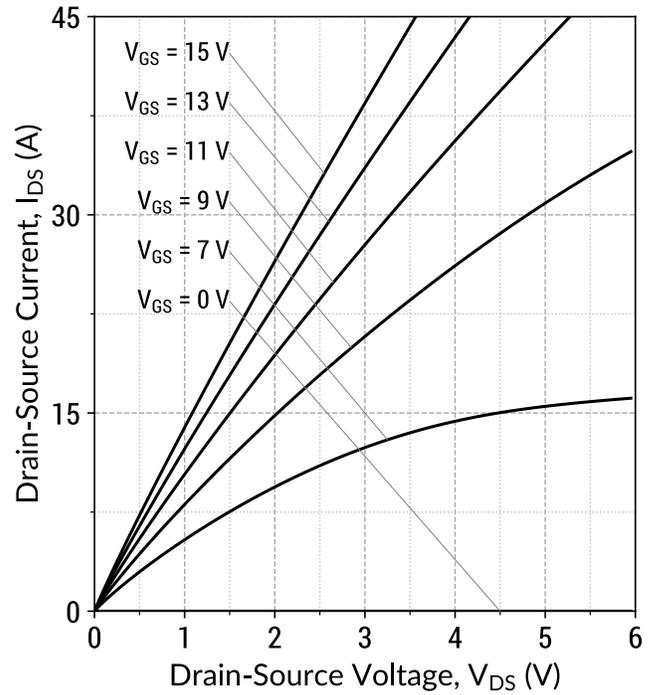
$I_D = f(V_{DS}, V_{GS})$; t$_P$ = 250 μs

Figure 3: Output Characteristics (V$_{GS}$ = 15 V)
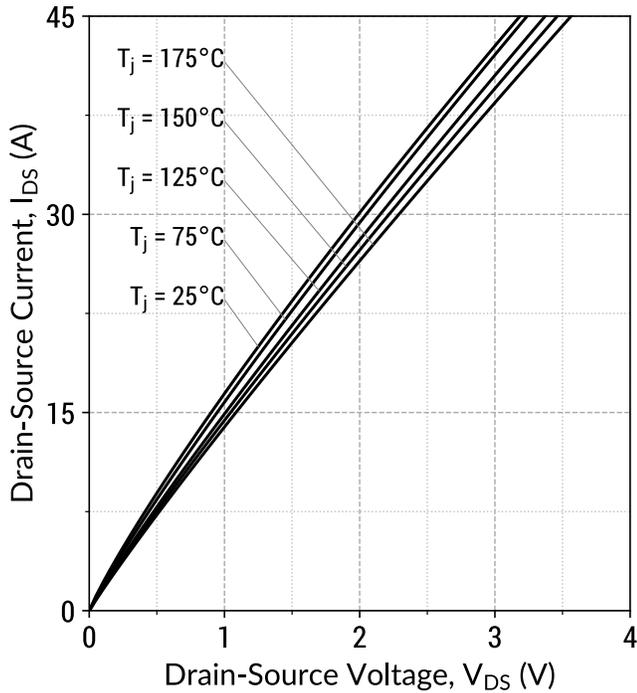
$I_D = f(V_{DS}, T_j)$; t$_P$ = 250 μs

Figure 4: Transfer Characteristics (V$_{DS}$ = 10 V)
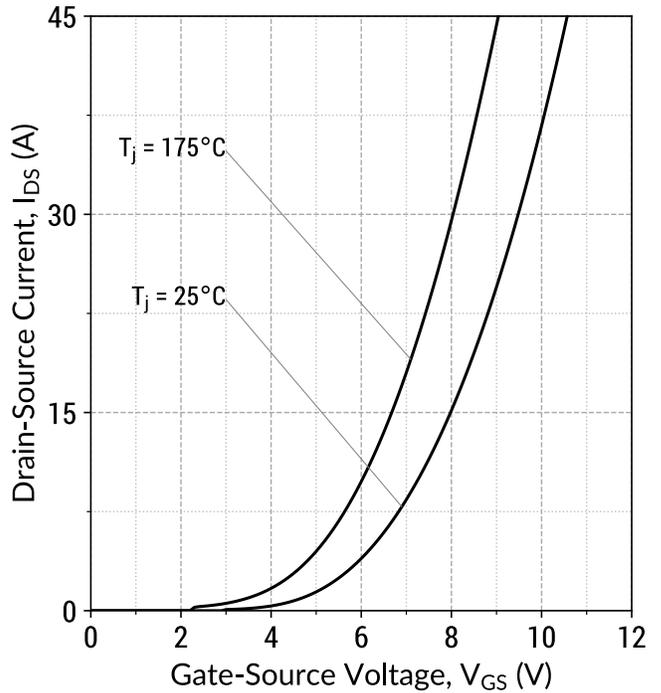
$I_D = f(V_{GS}, T_j)$; t$_P$ = 100 μs

Figure 5: On-State Resistance v/s Temperature
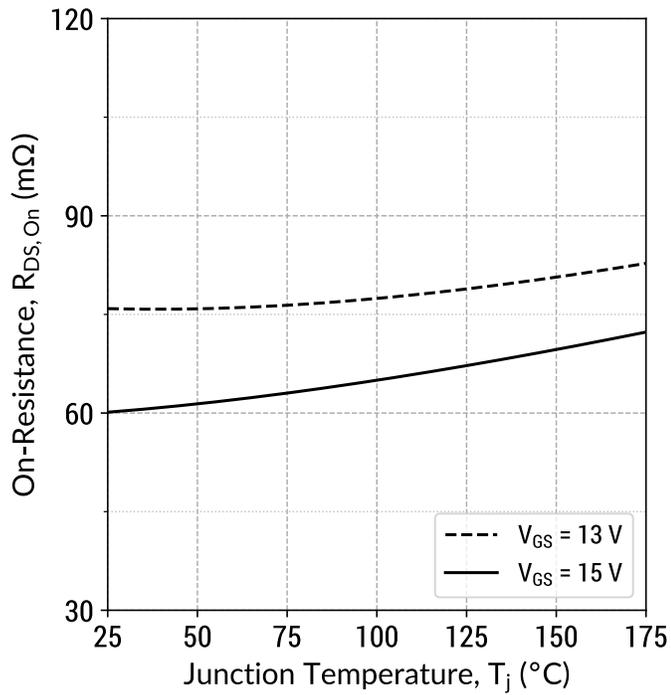
$R_{DS(ON)} = f(T_j, V_{GS}); t_P = 250\ \mu s; I_D = 15\ A$

Figure 6: On-State Resistance v/s Drain Current
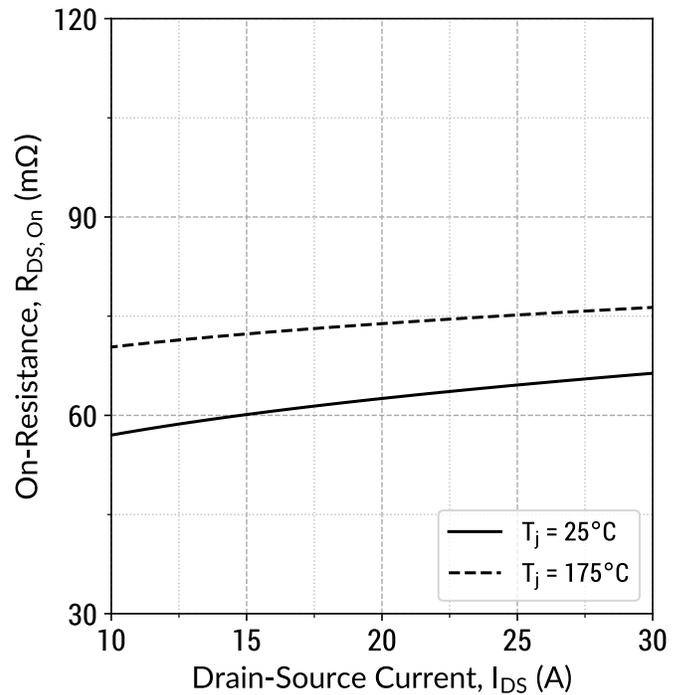
$R_{DS(ON)} = f(T_j, I_D); t_P = 250\ \mu s; V_{GS} = 15\ V$

## Figure 7: Normalized On-State Resistance v/s Temperature
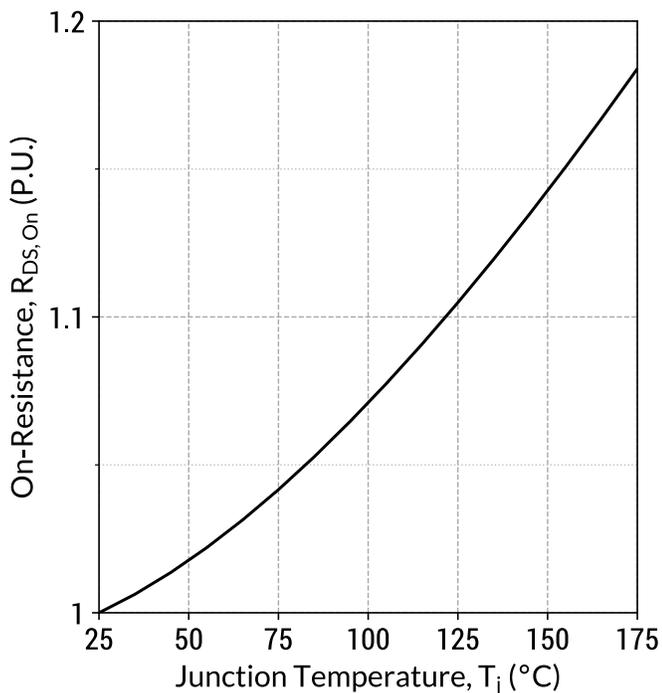
$R_{DS(ON)} = f(T_j); t_P = 250\ \mu s; I_D = 15\ A; V_{GS} = 15\ V$

Figure 8: On-State Resistance v/s Gate Voltage
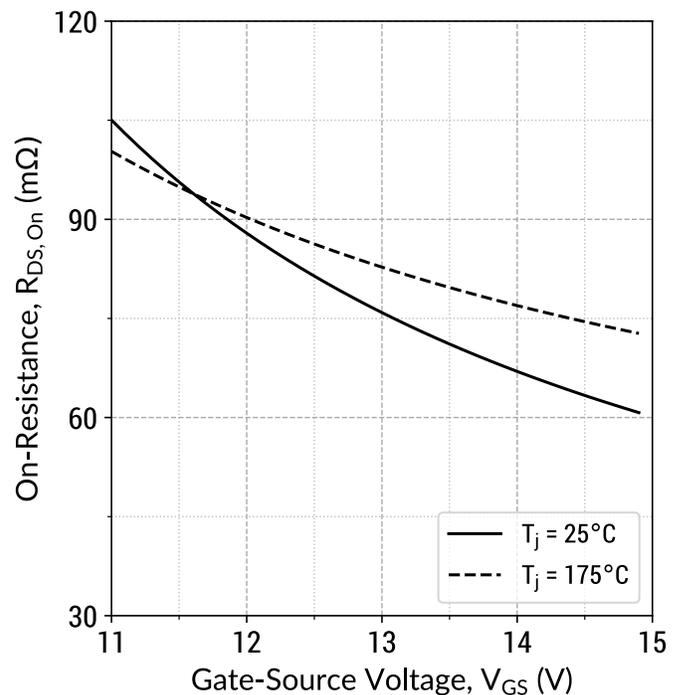
$R_{DS(ON)} = f(T_j, V_{GS}); t_P = 250\ \mu s; I_D = 15\ A$

Figure 9: Threshold Voltage Characteristics
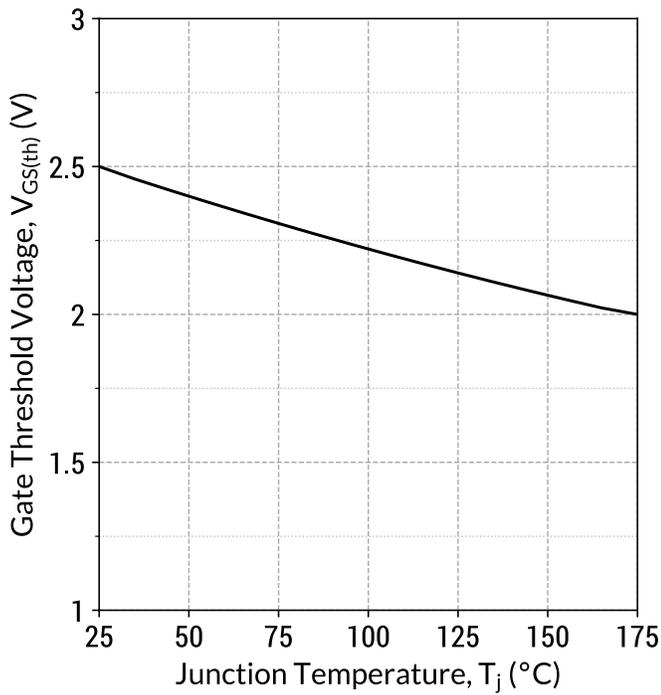
$V_{GS(th)} = f(T_j)$; $V_{DS} = V_{GS}$; $I_D = 8.0$ mA

Figure 10: Gate Charge Characteristics
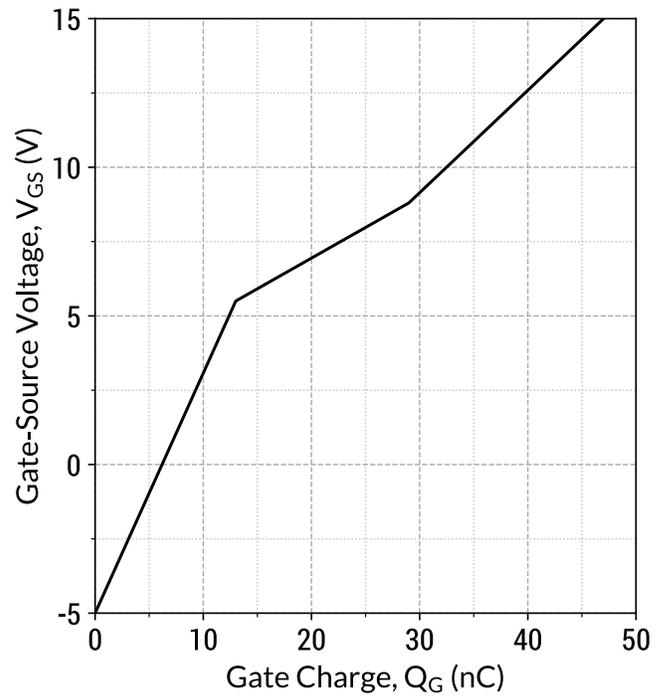
$I_D = 15$ A; $V_{DS} = 450$ V; $T_c = 25°C$

Figure 11: Capacitance v/s Drain-Source Voltage
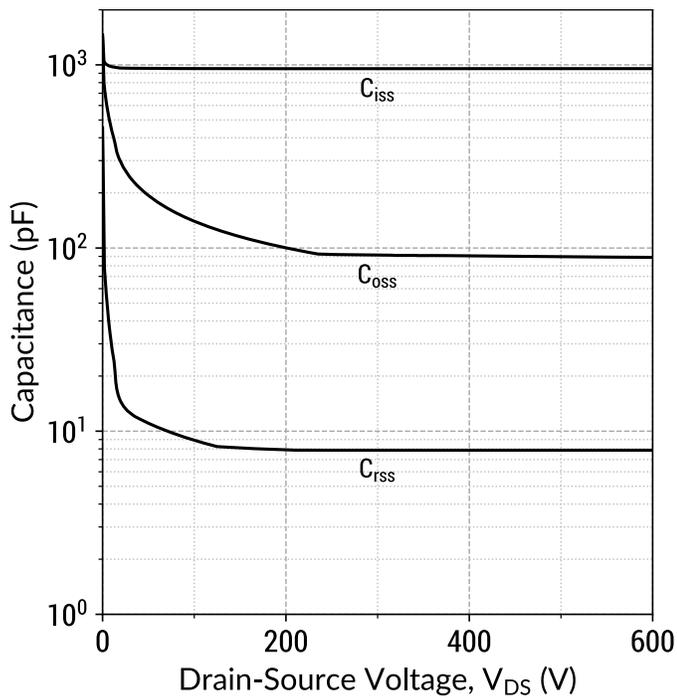

$f = 1$ MHz; $V_{AC} = 25$mV

Figure 12: Output Capacitor Stored Energy
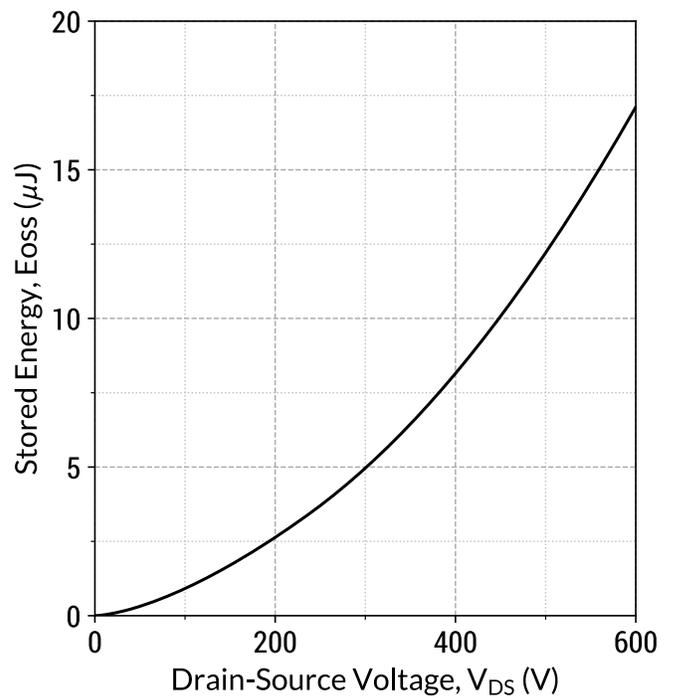
$E_{oss} = f(V_{DS})$

Figure 13: Transient Thermal Impedance

D = 0.5
D = 0.2
D = 0.1
D = 0.05
D = 0.02
D = Single Pulse
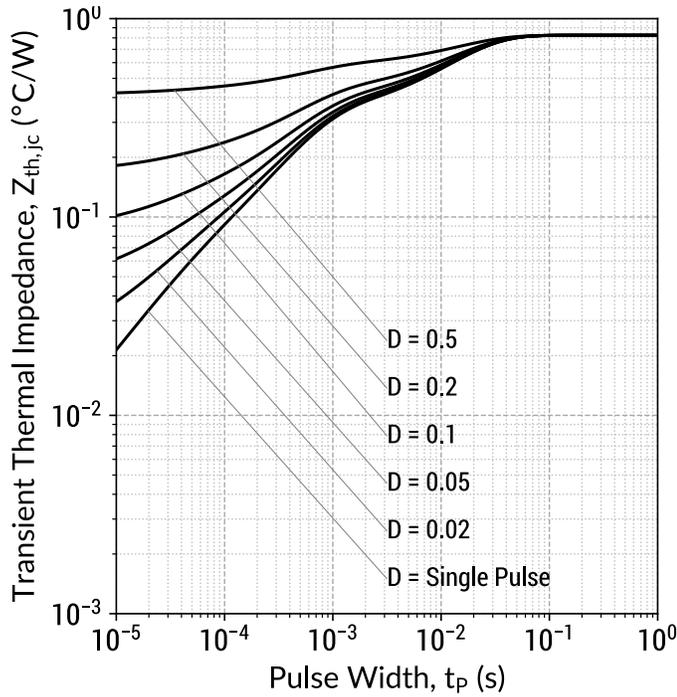
$Z_{th,jc} = f(t_P, D); D = t_P/T$

Figure 14: Safe Operating Area (T_c = 25°C)

100 ms
10 ms
100 µs
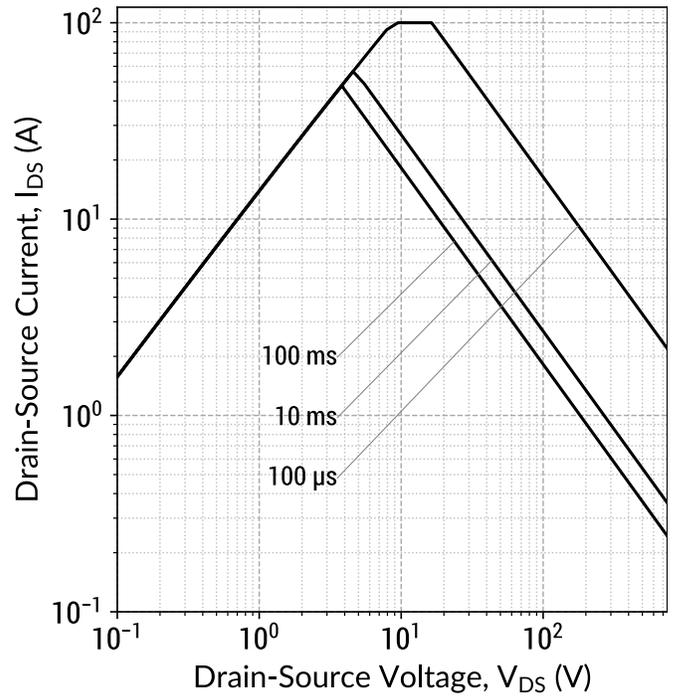
$I_D = f(V_{DS}, t_P); T_j \leq 175°C; D = 0$

Figure 15: Current De-rating Curve
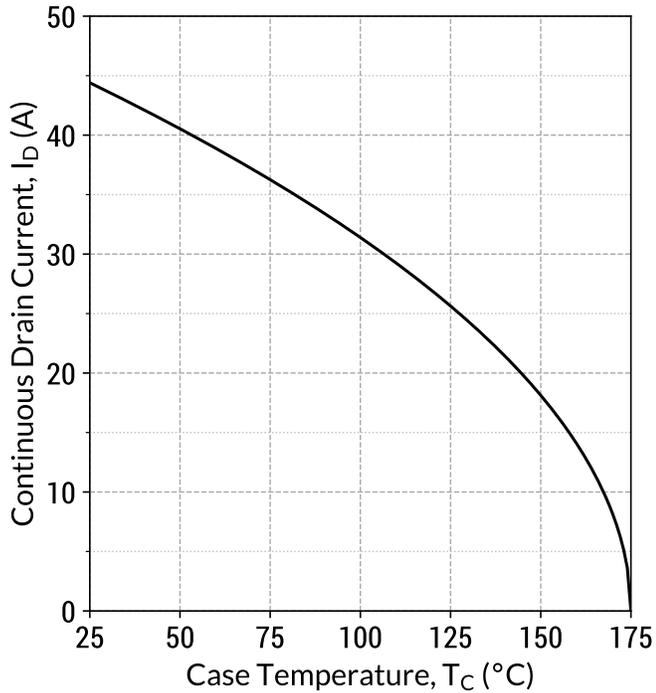

$I_D = f(T_C); T_j \leq 175°C$

Figure 16: Power De-rating Curve
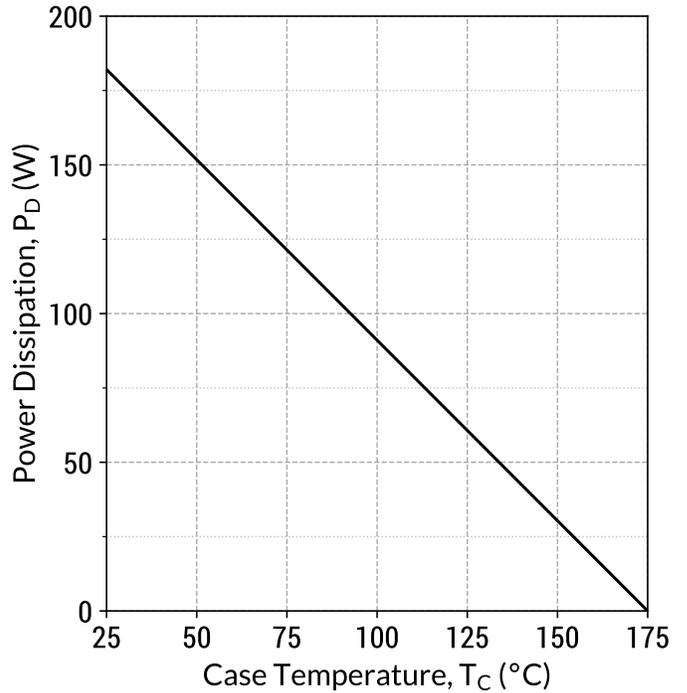
$P_D = f(T_C); T_j \leq 175°C$

Figure 17: Body Diode Characteristics (T$_j$ = 25°C)

V_{GS} = -5 V
V_{GS} = -4 V
V_{GS} = -3 V
V_{GS} = -2 V
V_{GS} = -1 V
V_{GS} = 0 V

Drain-Source Current, I$_{DS}$ (A)
Drain-Source Voltage, V$_{DS}$ (V)
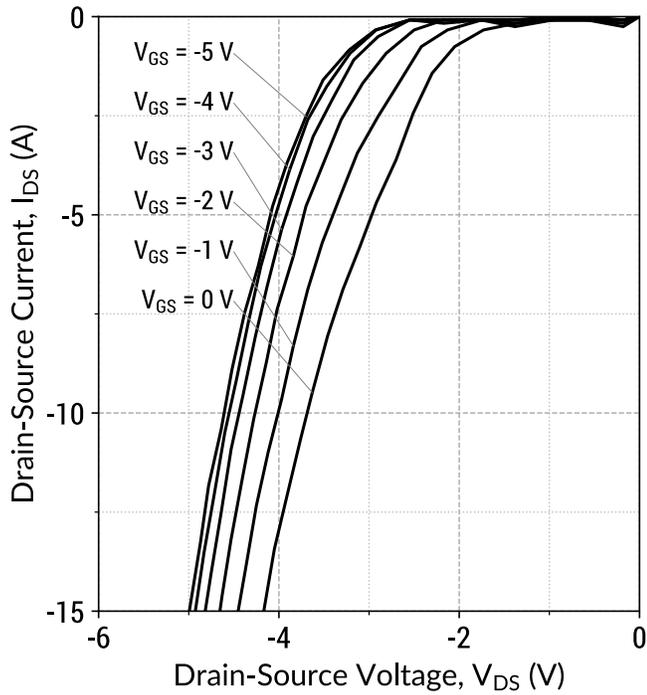
I_D = f(V$_{DS}$, V$_{GS}$); t$_P$ = 250 μs

Figure 18: Body Diode Characteristics (T$_j$ = 175°C)

V_{GS} = -5 V
V_{GS} = -4 V
V_{GS} = -3 V
V_{GS} = -2 V
V_{GS} = -1 V
V_{GS} = 0 V

Drain-Source Current, I$_{DS}$ (A)
Drain-Source Voltage, V$_{DS}$ (V)
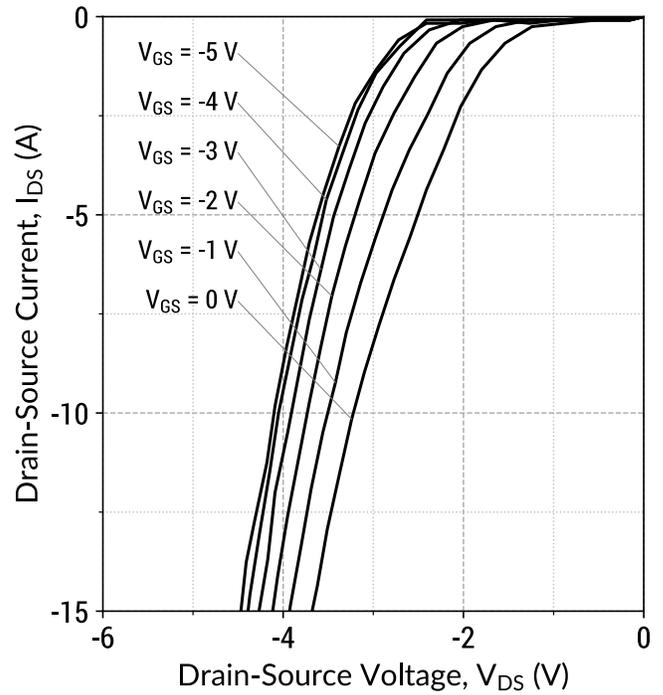
I_D = f(V$_{DS}$, V$_{GS}$); t$_P$ = 250 μs

Figure 19: Third Quadrant Characteristics (T$_j$ = 25°C)

V_{GS} = 15 V
V_{GS} = 0 V

Drain-Source Current, I$_{DS}$ (A)
Drain-Source Voltage, V$_{DS}$ (V)
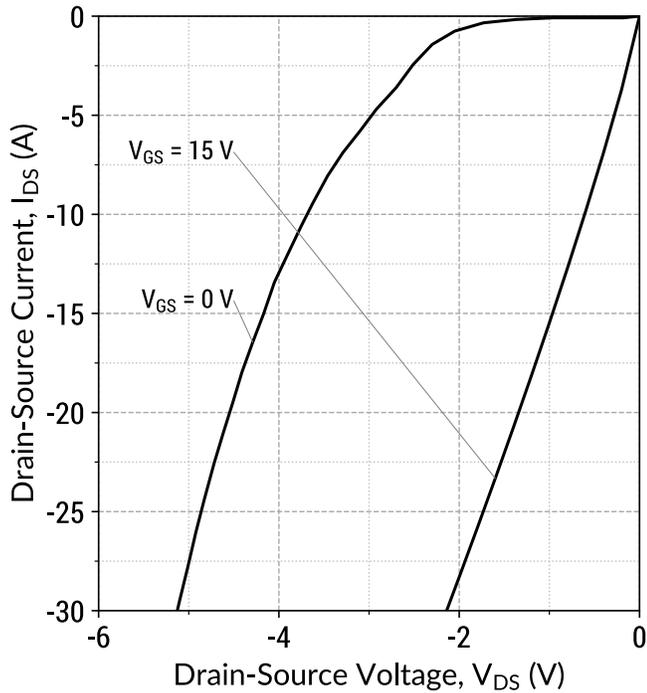
I_D = f(V$_{DS}$, V$_{GS}$); t$_P$ = 250 μs

Figure 20: Third Quadrant Characteristics (T$_j$ = 175°C)

V_{GS} = 15 V
V_{GS} = 0 V

Drain-Source Current, I$_{DS}$ (A)
Drain-Source Voltage, V$_{DS}$ (V)

I_D = f(V$_{DS}$, V$_{GS}$); t$_P$ = 250 μs

GeneSiC™
SEMICONDUCTOR
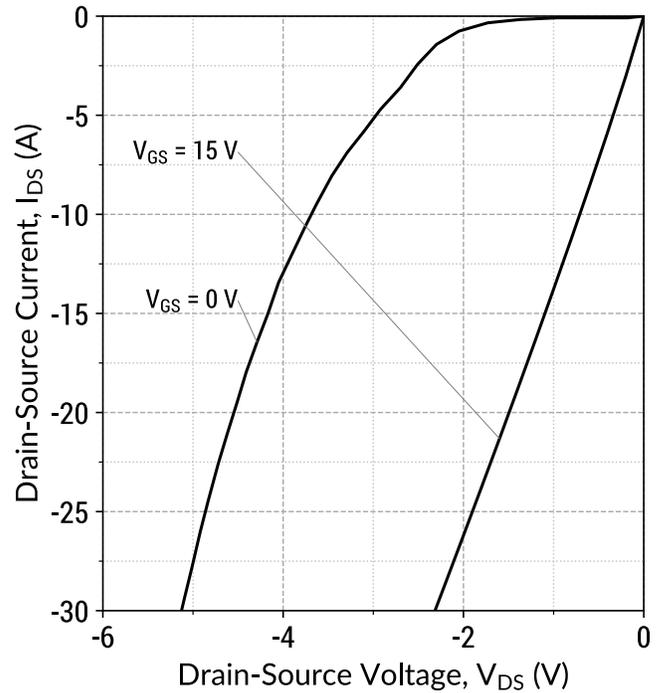
Figure 21: Inductive Switching Energy v/s Drain Current $(V_{DD} = 350V)$
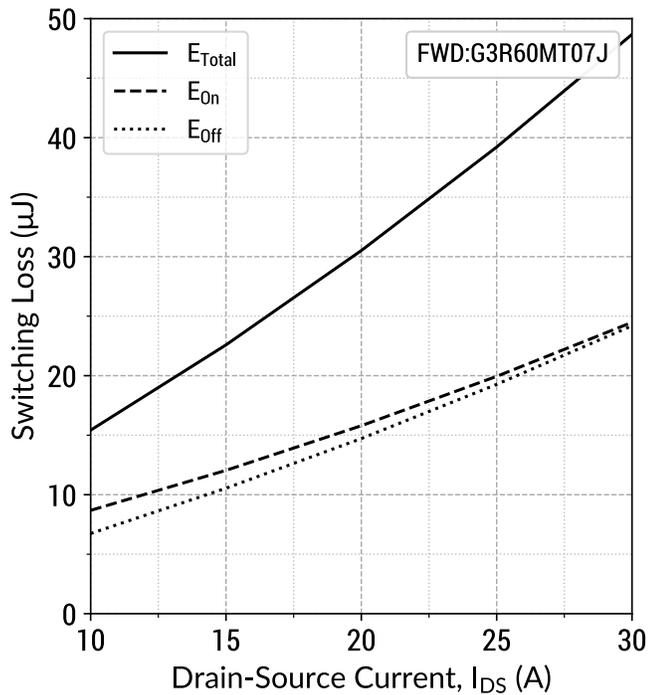
$T_j = 25°C; V_{GS} = -5/+15V; R_{G(ext)} = 3\ \Omega; L = 60.0\mu H$

Figure 22: Inductive Switching Energy v/s Drain Current $(V_{DD} = 450V)$
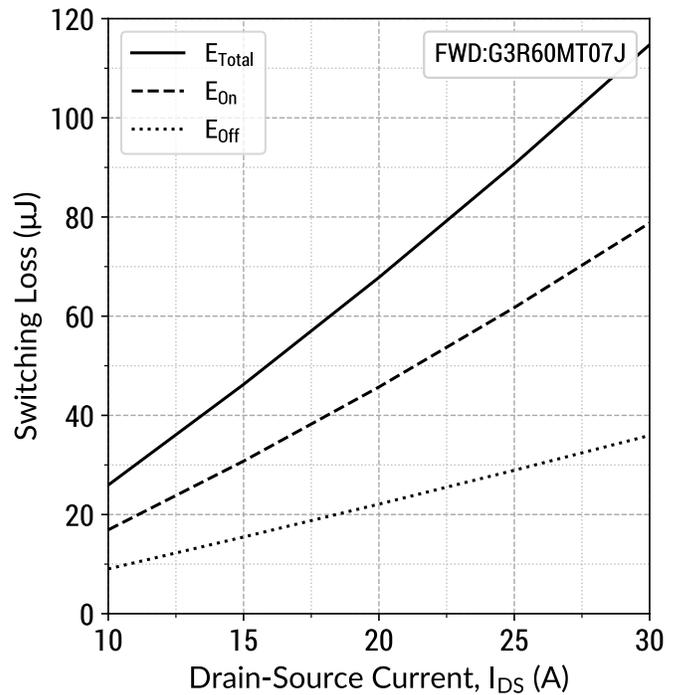

$T_j = 25°C; V_{GS} = -5/+15V; R_{G(ext)} = 3\ \Omega; L = 60.0\mu H$

Figure 23: Inductive Switching Energy v/s $R_{G(ext)}$ $(V_{DD} = 450V)$
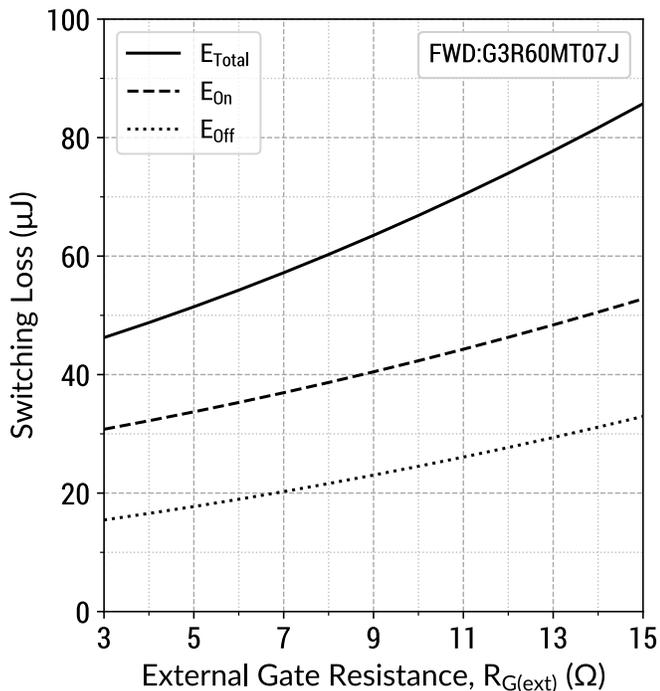
$T_j = 25°C; V_{GS} = -5/+15V; I_{DS} = 15\ A; L = 60.0\mu H$

**Figure 24: Switching Time v/s $R_{G(ext)}$** $(V_{DD} = 450V)$
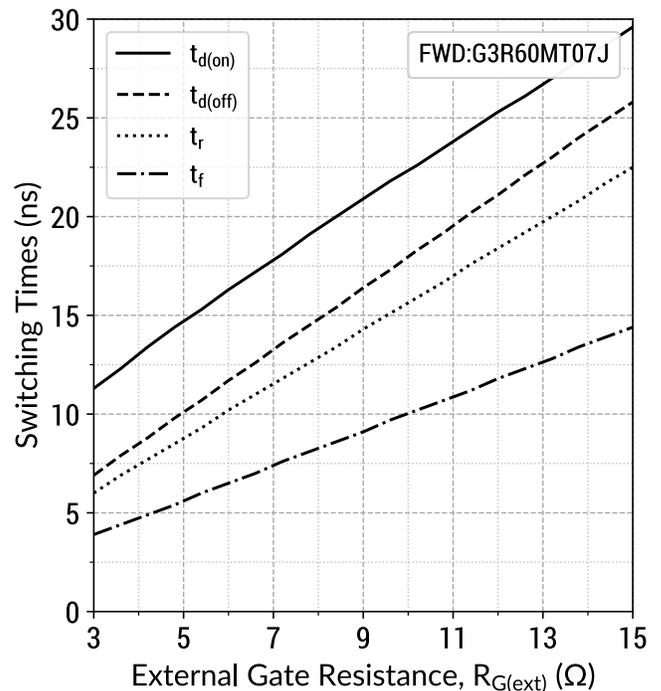
$T_j = 25°C; V_{GS} = -5/+15V; I_{DS} = 15\ A; L = 60.0\mu H$

Figure 25: Inductive Switching Energy v/s Temperature
(V_{DD} = 450V)
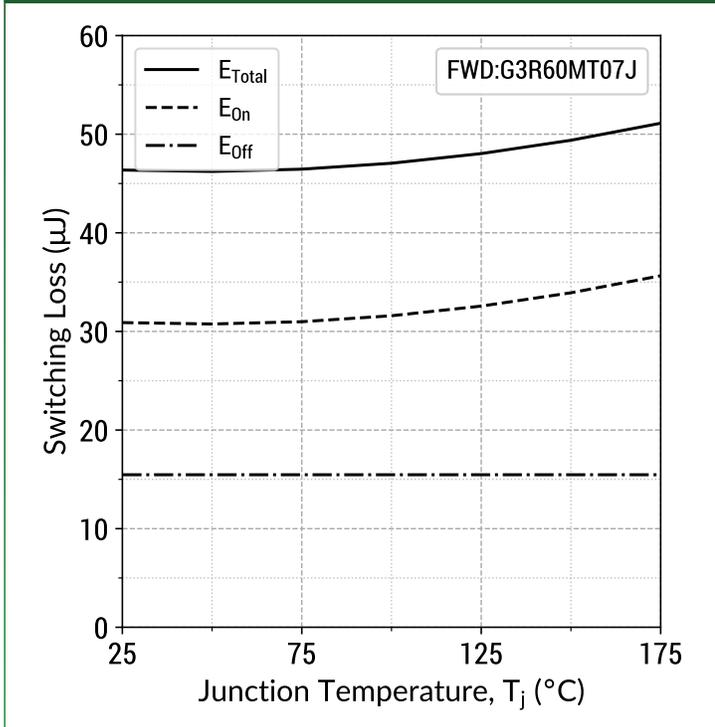
T_j = 25°C; V_{GS} = -5/+15V; $R_{G(ext)}$ = 3 Ω; I_{DS} = 15 A; L = 60.0µH

Figure 26: dV/dt v/s $R_{G(ext)}$
(V_{DD} = 450V)

T_j = 25°C; V_{GS} = -5/+15V; I_{DS} = 15 A; L = 60.0µH

Gate Charge Circuit

V_{DS}

V_{GS}

D.U.T

R_{Load}

$I_{G(cont)}$

I_D

V_{DD}

Gate Charge Waveform

Gate Voltage (V_{GS})

Q_{GS}

Q_{GD}
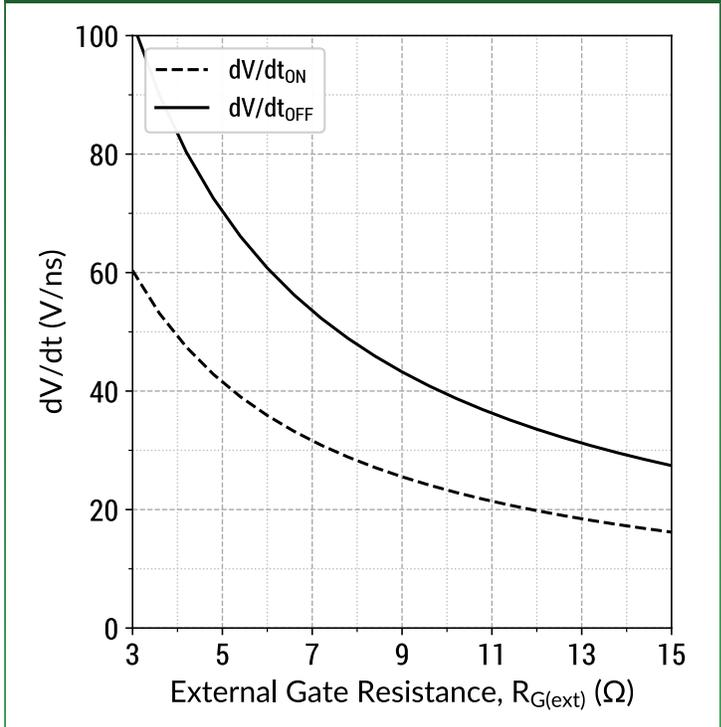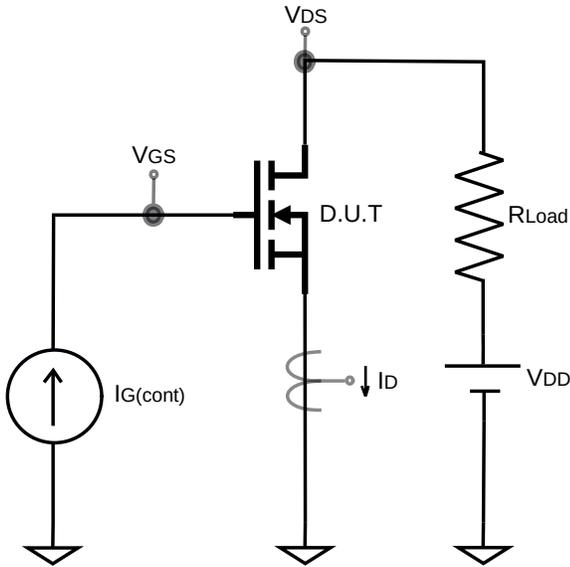
Gate Charge (Q_G)
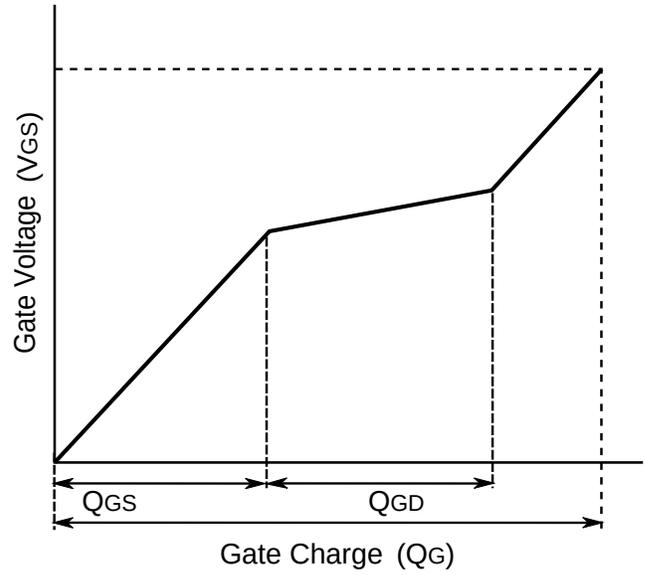
Switching Time Circuit

Same device as the D.U.T.

-5 v

L_{Load}

V_{DS}

R_G

V_{GS}

D.U.T.

V_{DD}

I_D
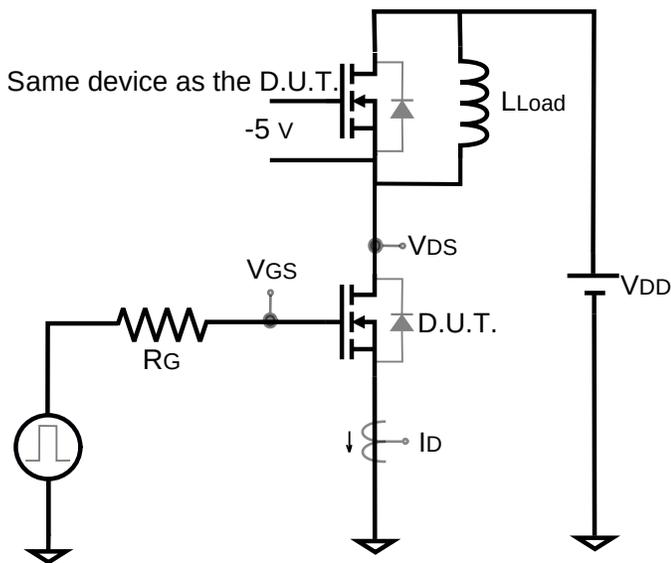
Switching Time Waveform

V_{GS} 10%

90%

V_{DS}

10%

10%

90%

90%

$t_{d(on)}$

t_r

t_{on}

$t_{d(off)}$

t_f

t_{off}
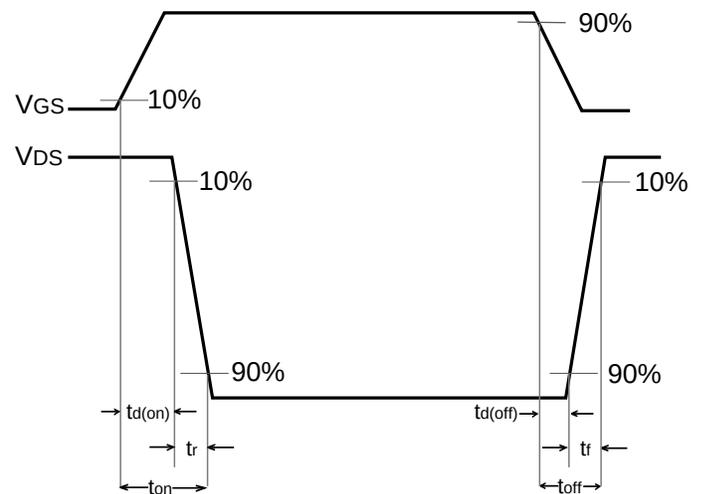
Switching Energy Circuit

Same device as the D.U.T.

-5 V

L_{Load}

V_{GS}

R_G

V_{DS}

D.U.T.

V_{DD}

I_D
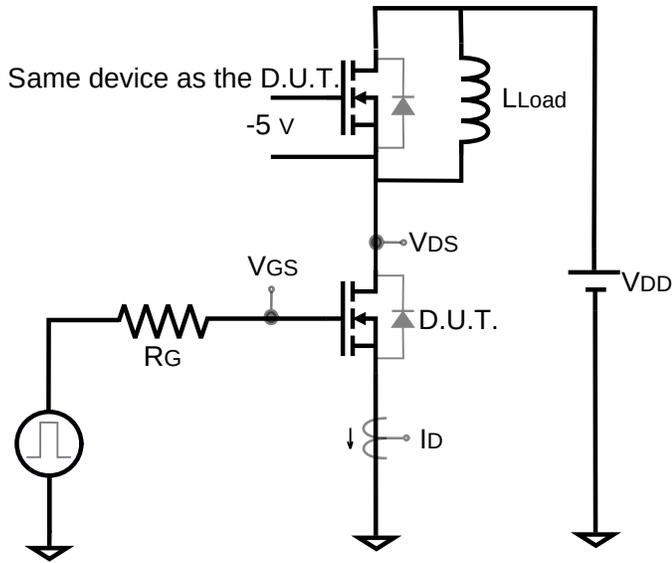
Switching Energy Waveform

$E_{ON} = \int I_D \times V_{DS} \times dt$

$E_{OFF} = \int I_D \times V_{DS} \times dt$

I_{rr}

V_{DS}

I_{DS}
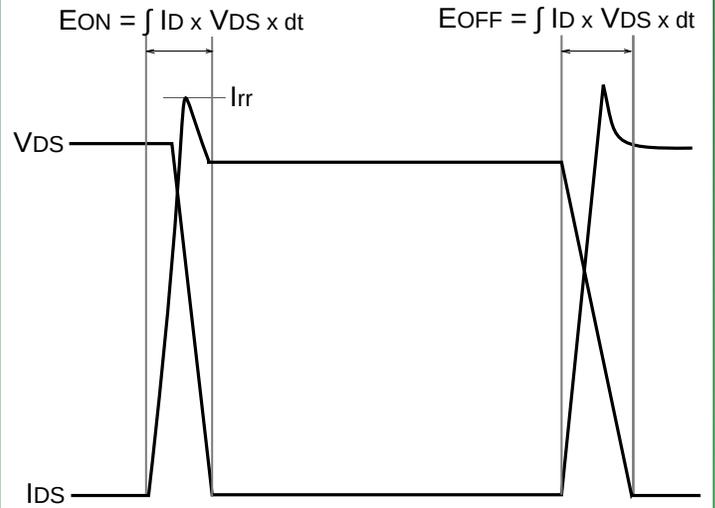
Reverse Recovery Circuit

D.U.T.

-5 V

L_{Load}

I_F

V_{GS}

R_G

Same device as the D.U.T.

V_{DD}
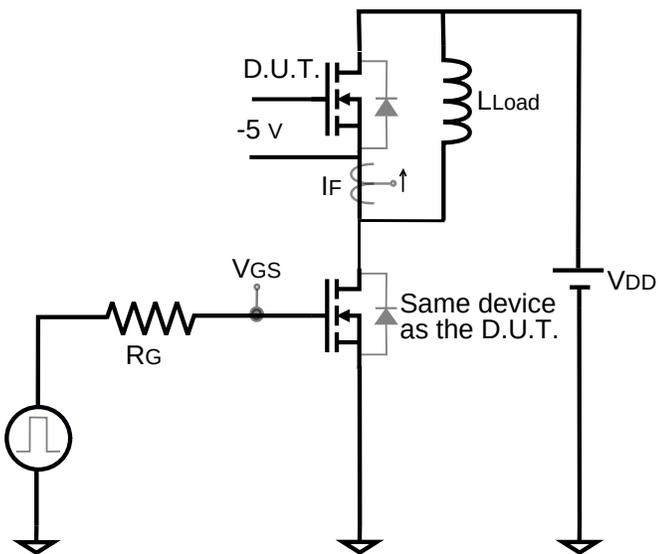
Reverse Recovery Waveform

I_F

0 Level

t_{rr}

90%

dI_{rr}/dt in 10% to 90% range

I_{rr}

10%

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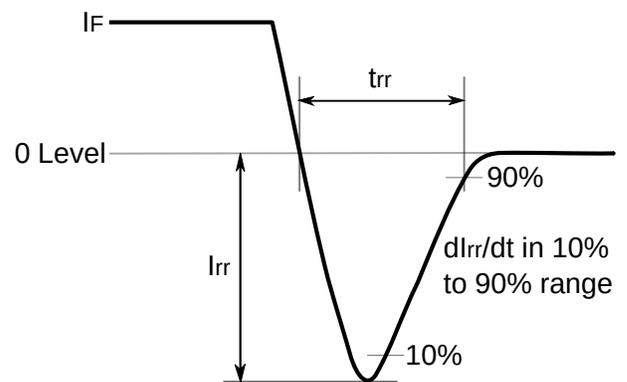
Package Dimensions

TO-263-7 Package Outline
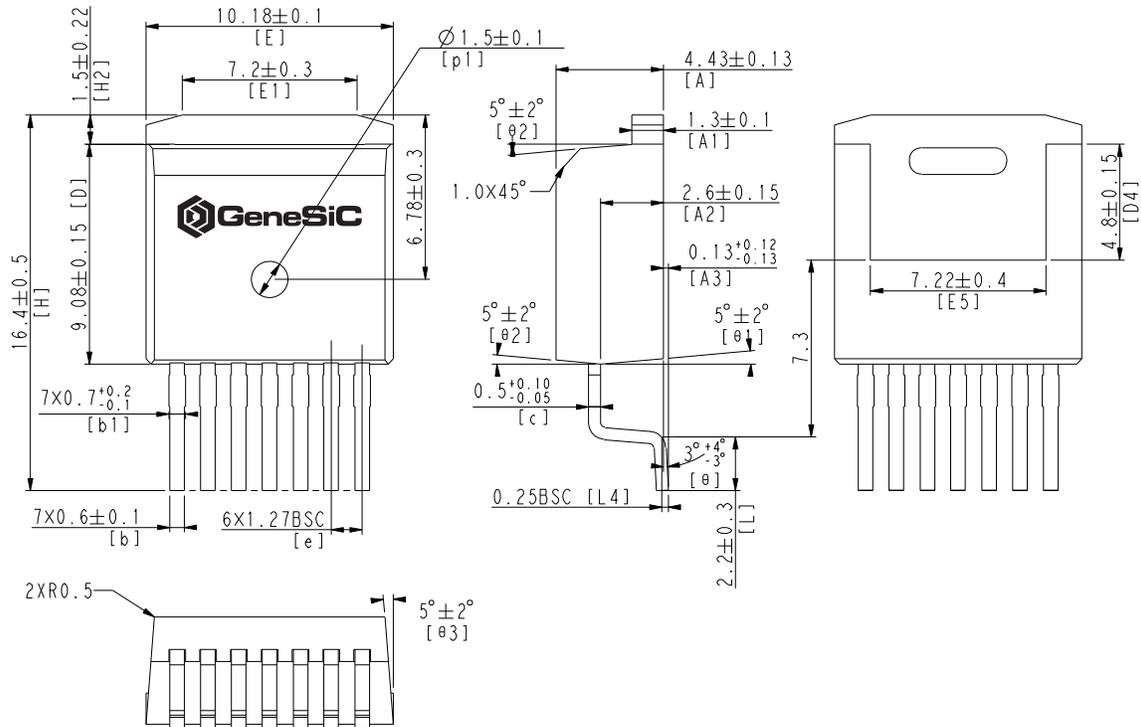
Recommended Solder Pad Layout
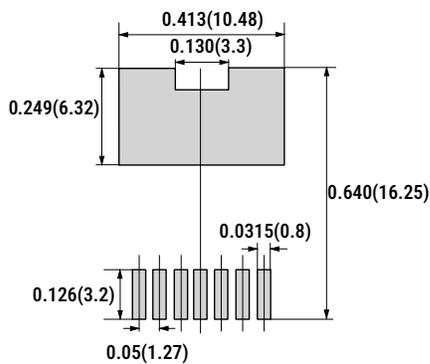
Package View
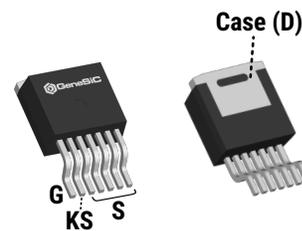
NOTE

1. CONTROLLED DIMENSION IS INCH. DIMENSION IN BRACKET IS MILLIMETER.
2. DIMENSIONS DO NOT INCLUDE END FLASH, MOLD FLASH, MATERIAL PROTRUSIONS.
3. THE SOURCE AND KELVIN-SOURCE PINS ARE NOT INTERCHANGABLE. THEIR EXCHANGE MIGHT LEAD TO MALFUNCTION.

Compliance

RoHS Compliance

The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS 2), as adopted by EU member states on January 2, 2013 and amended on March 31, 2015 by EU Directive 2015/863. RoHS Declarations for this product can be obtained from your GeneSiC representative.

REACH Compliance

REACH substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future, please contact a GeneSiC representative to insure you get the most up-to-date REACH SVHC Declaration. REACH banned substance information (REACH Article 67) is also available upon request.

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Unless otherwise expressly indicated, GeneSiC products are not designed, tested or authorized for use in life-saving, medical, aircraft navigation, communication, air traffic control and weapons systems, nor in applications where their failure may result in death, personal injury and/or property damage.

Related Links

- SPICE Models: https://www.genesicsemi.com/sic-mosfet/G3R60MT07J/G3R60MT07J_SPICE.zip
- PLECS Models: https://www.genesicsemi.com/sic-mosfet/G3R60MT07J/G3R60MT07J_PLECS.zip
- CAD Models: https://www.genesicsemi.com/sic-mosfet/G3R60MT07J/G3R60MT07J_3D.zip
- Gate Driver Reference: https://www.genesicsemi.com/technical-support
- Evaluation Boards: https://www.genesicsemi.com/technical-support
- Reliability: https://www.genesicsemi.com/reliability
- Compliance: https://www.genesicsemi.com/compliance
- Quality Manual: https://www.genesicsemi.com/quality

Revision History

- Rev 21/May: Initial Release

www.genesicsemi.com/sic-mosfet/

Rev 21/May
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