PLCHIP-P10-51220

32-bit PLC on a Chip Integrated Circuit with up to 256KB Flash, Ethernet, LCD, Digital I/O, Analog I/O, PWM

Rev. 4 - 01/27/2021

DATA SHEET

Divelbiss CORPORATION

Datasheet Contents

WARNING!!

The PLC on a Chip, must not be used alone in applications which could be hazardous to personnel in the event of failure of this device. Precautions must be taken by the user to provide mechanical and/or electrical safeguards external to this device. This device is NOT APPROVED for domestic or human medical use. All PLC on a Chip Specifications and Requirements subject to change without notice.

1. General Description

The P-Series PLC on a Chip™ (PLCHIP-P10-51220) is a 32 bit microcontroller for embedded applications with full PLC functionality. The P-Series combines powerful peripherals with industry standard I/O for a complete package that provides the advanced features required while providing an easy-to-use ladder diagram programming and structured text interface; EZ LADDER Toolkit.

The PLCHIP-P10-51220 provides many features of the PLCHIP-P13-51220 in a smaller footprint (package). Features include up to 256K of Program Flash Storage, 32K of RAM, up to 106 general purpose digital I/O, up to 3 I2C ports, up to 2 SPI Ports, up to 2 CAN Network Ports, up to 4 Serial Ports, up to 8 Analog Inputs, up to 1 Analog Output, up to 3 Pulse Width Modulation Outputs, 1 Ethernet Port, , Internal Real Time Clock, SD Card Interface, up to 4 counter/timer inputs, up to 1 quadrature counter input, LCD Display Support,and Keypad Support.

The P-Series PLC on a Chip™ is programmed exclusively using EZ LADDER Toolkit.

2. Features and Benefits

- **Memory:**
  - Up to 256K Flash memory for Ladder Program storage.
  - Up to 32K RAM memory program execution and variables.
  - Up to 3500 bytes EEPROM memory for Set Point Storage and Retentive Variable Storage.
- **Serial Interfaces:**
  - Up to three I^2C Ports. 1Mbit/s Data Rate
  - Up to four TTL Serial Ports. One Supports full handshaking while 3 support RX/TX. Supports Modbus Master & Slave.
  - TTL Ethernet Port, Supports Modbus over TCP
  - Up to two Controller Area Network (CAN) Ports. Supports Divelbiss OptiCAN, SAE J1939
  - Up to two SPI Ports.
- **HMI Support:**
  - Supports HD44780 Controller Compatible LCD Displays with up to 4 rows and up to 40 columns.
  - Supports a Keypad matrix of 5 columns by 4 rows for numbers 0-9, decimal, function keys
- **Digital Interfaces:**
  - SD/MMC Memory Card Interface
  - Up to four inputs that may be utilized as counters or timers.
  - Up to three inputs when configured properly will interface to a quadrature encoder.
  - Up to 106 General Purpose I/O (GPIO) that may be individually configured as inputs or outputs.
  - Up to Three Pulse Width Modulated Outputs
  - Real Time Clock (requires external clock and power source).

- **Analog Interfaces:**
  - Up to 8 Channels, 12 bit Analog to Digital Converter (ADC).
  - Up to 1 Channel, 10 bit Digital to Analog Converter (DAC).

3. Ordering Information

PLC on a Chip™ P-10 Series Integrated Circuits may be ordered by Part number. Pricing varies based on part number and quantity.

Part Number	Description
PLCHIP-P10-51220	PLC on a Chip P-Series, 144 Pin Low Profile, Quad Flat Package (LQFP144), 256 Flash, 32K RAM, 106 GPIO, 3 PWM Channels, 8 ADC Channels, 1 DAC Channel, 4 Timer/Counter Channels, Quadrature Encoder Input, LCD / Keypad Support, Ethernet, 4 Serial Ports, 2 CAN Ports, SD/MMC Card Support. **Shipped in Trays of 60.**
PLCHIP-P10-51220X1	PLC on a Chip P-Series, P10 (PLCHIP-P10-512210). **Shipped as Single piece.**
PLCHIP-P10-51220X5	PLC on a Chip P-Series, P10 (PLCHIP-P10-512210). **Shipped as 5 Pack.**
PLCHIP-P10-51220X10	PLC on a Chip P-Series, P10 (PLCHIP-P10-512210). **Shipped as 10 Pack.**

4. Pin Summary

The PLC on a Chip™ P-Series provides great flexibility in features by allowing pins to be assigned multiple functions. While each Pin may only be configured to be a single function, many pins provide multiple configuration options for functionality. These options are listed as Function 1 through Function 4 for each pin in TABLE 1.

TABLE 1 - Pin Summary

Pin #	Function 1	Function 2	Function 3	Function 4
1	RES11	---	---	---
2	GPIO99	---	---	---
3	RES7	---	---	---
4	RES8	---	---	---
5	RES6	---	---	---
6	GPIO160	---	---	---
7	RES9	---	---	---
8	GPIO26	AI3	AO0	---
9	GPIO100	---	---	---
10	GPIO25	AI2	---	---
11	GPIO24	AI1	---	---

TABLE 1 - Pin Summary				
Pin #	**Function 1**	**Function 2**	**Function 3**	**Function 4**
12	GPIO101	---	---	---
13	GPIO23	AI0	---	---
14	VDD_AN	---	---	---
15	VSS_AN	---	---	---
16	GPIO102	---	---	---
17	VREF_AN	---	---	---
18	VDD1	---	---	---
19	GPIO103	---	---	---
20	$\overline{\text{RSTOUT}}$	---	---	---
21	GPIO161	---	---	---
22	VSS1	---	---	---
23	RTCX1	---	---	---
24	$\overline{\text{~RESET}}$	---	---	---
25	RTCX2	---	---	---
26	RES2	---	---	---
27	VBAT	---	---	---
28	GPIO63	AI5	---	---
29	GPIO12	AI6	---	---
30	GPIO62	AI4	---	---
31	XTAL1	---	---	---
32	GPIO13	AI7	---	---
33	XTAL2	---	---	---
34	GPIO28	I2C_SCL0	---	---
35	GPIO27	I2C_SDA0	---	---
36	GPIO31	---	---	---
37	NO CONNECT	---	---	---
38	GPIO122	PWM2	---	---
39	GPIO121	PWM1	---	---
40	GPIO120	PWM0	---	
41	VDD2	---	---	---
42	GPIO29	---	---	---
43	GPIO30	---	---	---
44	VSS2	---	---	---
45	GPIO119	---	---	
46	GPIO50	TMR_CAP1.0	---	---
47	GPIO51	TMR_CAP1.1	---	---
48	GPIO14	---	---	---
49	GPIO52	QEI_PHA	---	---
50	GPIO53	---	---	---
51	GPIO54	TMR_MAT1	---	---

TABLE 1 - Pin Summary				
Pin #	**Function 1**	**Function 2**	**Function 3**	**Function 4**
52	GPIO128	LCD_D0	---	---
53	GPIO55	QEI_PHB	---	---
54	GPIO56	QEI_IDX	---	---
55	GPIO129	LCD_D1	---	---
56	GPIO57	---	---	---
57	GPIO58	TMR_CAP0.0	---	---
58	GPIO130	LCD_D2	---	---
59	VSS3	---	---	---
60	VDD3	---	---	---
61	GPIO59	TMR_CAP0.1	---	---
62	VDD4	---	---	---
63	GPIO60	TMR_MAT0	---	---
64	GPIO61	MCI_CARD_PRESENT	---	---
65	VSS4	---	---	---
66	GPIO0	CAN_RX0	I2C_SDA1	---
67	GPIO1	CAN_TX0	I2C_SCL1	---
68	GPIO131	LCD_D3	---	---
69	GPIO10	I2C_SDA2	---	---
70	GPIO11	12C_SCL2	---	---
71	GPIO77	MCI_DATA3	---	---
72	GPIO132	LCD_D4	---	---
73	GPIO76	MCI_DATA2	---	---
74	GPIO133	LCD_D5	---	---
75	GPIO75	MCI_DATA1	---	---
76	LED_KERNEL	Pull to 3.3V	---	---
77	VDD5	---	---	---
78	GPIO134	LCD_D6	---	---
79	VSS5	---	---	---
80	GPIO22	MCI_DATA0	---	---
81	GPIO162	---	---	---
82	GPIO21	MCI_PWR	---	---
83	GPIO20	MCI_CMD	---	---
84	GPIO135	LCD_D7	---	---
85	GPIO19	MCI_CLK	---	---
86	GPIO18	SPI_MOSI0	---	---
87	GPIO17	SPI_MISO0	---	---
88	GPIO136	LCD_RS	---	---
89	GPIO15	SPI_SCK0	---	---
90	GPIO16	$\overline{\text{LOW\_VOLT\_SENSE}}$	---	---
91	GPIO137	LCD_RW	---	---

TABLE 1 - Pin Summary				
Pin #	**Function 1**	**Function 2**	**Function 3**	**Function 4**
92	GPIO73	RXD2	---	---
93	GPIO72	TXD2	---	---
94	GPIO138	LCD_E	---	---
95	GPIO71	RTS1	---	---
96	GPIO70	RI1	---	---
97	GPIO69	DTR1	---	---
98	GPIO163	RXD4	---	---
99	GPIO68	DSR1	---	---
100	GPIO67	DCD1	---	---
101	GPIO139	KEYPAD_COL1	---	---
102	VDD6	---	---	---
103	VSS6	---	---	---
104	GPIO140	KEYPAD_COL2	---	---
105	GPIO66	CTS1	---	---
106	GPIO65	RXD1	---	---
107	GPIO64	TXD1	---	---
108	GPIO141	KEYPAD_COL3	---	---
109	GPIO9	SPI_MOSI1	---	---
110	GPIO142	KEYPAD_COL4	---	---
111	GPIO8	SPI_MISO1	---	---
112	GPIO7	SPI_SCK1	---	---
113	GPIO6	TMR_MAT2	---	---
114	VDD7	---	---	---
115	GPIO5	CAN_TX1	---	---
116	GPIO4	CAN_RX1	---	---
117	VSS7	---	---	---
118	GPIO156	TXD3	---	---
119	VSS8	---	---	---
120	GPIO143	KEYPAD_COL5	---	---
121	VDD8	---	---	---
122	GPIO157	RXD3	---	---
123	GPIO49	ETHER_MDIO	---	---
124	GPIO153	KEYPAD_ROW2	---	---
125	GPIO48	ETHER_MDC	---	---
126	GPIO47	ETHER_REFCLK	---	---
127	GPIO152	KEYPAD_ROW1	---	---
128	GPIO46	ETHER_RXER	---	---
129	GPIO42	ETHER_RXD1	---	---
130	GPIO158	KEYPAD_ROW3	---	---

TABLE 1 - Pin Summary				
Pin #	**Function 1**	**Function 2**	**Function 3**	**Function 4**
131	GPIO41	ETHER_RXD0	---	---
132	GPIO40	ETHER_CRS	---	---
133	GPIO36	$\overline{\text{ETHER\_TXEN}}$	---	---
134	GPIO159	KEYPAD_ROW4	---	---
135	GPIO33	ETHER_TXD1	---	---
136	GPIO32	ETHER_TXD0	---	---
137	GPIO96	---	---	---
138	VDD9	---	---	---
139	VSS9	---	---	---
140	GPIO97	---	---	---
141	TXD0	---	---	---
142	RXD0	---	---	---
143	GPIO164	TXD4	---	---
144	GPIO98	---	---	---

5. Pin Details

TABLE 2 lists details for each pins individual supported functions. Required pins and related pins are also listed.

TABLE 2 - Pin Details	
Pin #	**Description**
1	**Not Connected** Do Not Connect this pin.
2	**GPIO99** General Purpose Digital I/O. May be configured as General Purpose Input 99 (GPI99) or General Purpose Output 99 (GPO99).
3	**Not Connected** Do Not Connect this pin.
4	**Not Connected** Do Not Connect this pin.
5	**Not Connected** Do Not Connect this pin.

TABLE 2 - Pin Details	
Pin #	**Description**
6	**GPIO160** General Purpose Digital I/O. May be configured as General Purpose Input 160 (GPI160) or General Purpose Output 160 (GPO160).
7	**Not Connected** Do Not Connect this pin.
8	**GPIO26** General Purpose Digital I/O. May be configured as General Purpose Input 26 (GPI26) or General Purpose Output 26 (GPO26). **AI3** Analog Input 3. Not to exceed 3.3VDC. Resolution: 12 bit. The following pins are required for Analog Input functionality: 14, 15, 17. Related Analog Input Pins: 8, 10, 11, 13, 28, 29, 30, 32 **AO0** Analog Output 0. 3.3VDC Maximum Output. Resolution 10 bit. The following pins are required for Analog Output functionality: 14, 15.
9	**GPIO100** General Purpose Digital I/O. May be configured as General Purpose Input 100 (GPI100) or General Purpose Output 100 (GPO100).
10	**GPIO25** General Purpose Digital I/O. May be configured as General Purpose Input 25 (GPI25) or General Purpose Output 25 (GPO25). **AI2** Analog Input 2. Not to exceed 3.3VDC. Resolution: 12 bit. The following pins are required for Analog Input functionality: 14, 15, 17. Related Analog Input Pins: 8, 10, 11, 13, 28, 29, 30, 32
11	**GPIO24** General Purpose Digital I/O. May be configured as General Purpose Input 24 (GPI24) or General Purpose Output 24 (GPO24). **AI1** Analog Input 1. Not to exceed 3.3VDC. Resolution: 12 bit. The following pins are required for Analog Input functionality: 14, 15, 17. Related Analog Input Pins: 8, 10, 11, 13, 28, 29, 30, 32
12	**GPIO101** General Purpose Digital I/O. May be configured as General Purpose Input 101 (GPI101) or General Purpose Output 101 (GPO101).
13	**GPIO23** General Purpose Digital I/O. May be configured as General Purpose Input 23 (GPI23) or General Purpose Output 23 (GPO23). **AI0** Analog Input 0. Not to exceed 3.3VDC. Resolution: 12 bit. The following pins are required for Analog Input functionality: 14, 15, 17. Related Analog Input Pins: 8, 10, 11, 13, 28, 29, 30, 32

TABLE 2 - Pin Details	
Pin #	**Description**
14	**VDD_AN** +V Power Supply for on-board analog circuitry. Connect to 3.3VDC supply. This pin can be connected to the same 3.3VDC logic supply for the PLC on a Chip™ or a separate supply as required for noise and error. This pin is used to power the on-board ADC and DAC components. The recommended bypass capacitor must be installed near this pin (this pin to the VSS_AN pin). If the ADC and DAC are not used, this pin should be connected to 3.3VDC. The following pins are required for Analog Input functionality: 14, 15, 17. Related Analog Input Pins: 8, 10, 11, 13, 28, 29, 30, 32
15	**VSS_AN** Analog Ground. 0V Power Supply / Reference for the on-board ADC and DAC components. This should be the same potential as VSS (GND) but isolated as required to minimize noise and error. The following pins are required for Analog Input functionality: 14, 15, 17. Related Analog Input Pins: 8, 10, 11, 13, 28, 29, 30, 32
16	**GPIO102** General Purpose Digital I/O. May be configured as General Purpose Input 102 (GPI102) or General Purpose Output 102 (GPO102).
17	**VREF_AN** On-board ADC Positive Reference Voltage. This should be the same voltage as VDD. It should be isolated as required to minimize noise and error. The voltage level on this pin is used as a reference for the ADC and DAC. If the ADC and DAC are not used, this pin should be connected to 3.3VDC. The recommended bypass capacitor must be installed near this pin (this pin to the VSS_AN pin). The following pins are required for Analog Input functionality: 14, 15, 17. Related Analog Input Pins: 8, 10, 11, 13, 28, 29, 30, 32
18	**VDD1** Connect to 3.3VDC Supply. The recommended bypass capacitor must be installed near this pin (this pin to GND / 3.3V COMMON).
19	**GPIO103** General Purpose Digital I/O. May be configured as General Purpose Input 103 (GPI103) or General Purpose Output 103 (GPO103).
20	**$\overline{\text{RSTOUT}}$** Reset Output. This pin is used to connect to other smart integrated circuits and provides the status of the PLC on a Chip™. When LOW, the PLC on a Chip™ is in the reset state.
21	**GPIO161** General Purpose Digital I/O. May be configured as General Purpose Input 161 (GPI161) or General Purpose Output 161 (GPO161).
22	**VSS1** Connect to GND / 3.3V COMMON.
23	**RTXC1** Real Time Cloock Power Oscillator Circuit Input. Ultra-low power. 32KHz oscillator required. The following pins are required for Real Time Clock (RTC) functionality: 23, 25, 27. See Section 6.19 - Real Time Clock for detials.

TABLE 2 - Pin Details	
Pin #	**Description**
24	**RESET** Reset Input Pin. A Low on this pin places the PLC on a ChipTM in the reset state, causing all I/O and peripherals to return to their default states. This pin includes a 20 ns input glitch filter. This pin should be connected to an extenal power-on reset device.
25	**RTXC2** Real Time Cloock Power Oscillator Circuit Output. The following pins are required for Real Time Clock (RTC) functionality: 23, 25, 27. See Section 6.19 - Real Time Clock for detials.
26	**Not Connected** Do Not Connect this pin.
27	**VBAT** Real Time Cloock Power Supply (3.3V nominal). Voltage on this pin supplies power to the Real Time Clock and provides a source of power to maintain RTC functionality when PLC on a Chip™ is not powered. If no RTC function is enabled (no battery), this pin should be connected to 3.3V. The following pins are required for Real Time Clock (RTC) functionality: 23, 25, 27.
28	**GPIO63** General Purpose Digital I/O. May be configured as General Purpose Input 63 (GPI63) or General Purpose Output 63 (GPO63). **AI5** Analog Input 5. Not to exceed 3.3VDC. Resolution: 12 bit. The following pins are required for Analog Input functionality: 14, 15, 17. Related Analog Input Pins: 8, 10, 11, 13, 28, 29, 30, 32
29	**GPIO12** General Purpose Digital I/O. May be configured as General Purpose Input 12 (GPI12) or General Purpose Output 12 (GPO12). **AI6** Analog Input 6. Not to exceed 3.3VDC. Resolution: 12 bit. The following pins are required for Analog Input functionality: 14, 15, 17. Related Analog Input Pins: 8, 10, 11, 13, 28, 29, 30, 32
30	**GPIO62** General Purpose Digital I/O. May be configured as General Purpose Input 62 (GPI62) or General Purpose Output 62 (GPO62). **AI4** Analog Input 4. Not to exceed 3.3VDC. Resolution: 12 bit. The following pins are required for Analog Input functionality: 14, 15, 17. Related Analog Input Pins: 8, 10, 11, 13, 28, 29, 30, 32
31	**XTAL1** Oscillator and internal clock generator circuit input. 12MHz oscillator required. See Section 6.3 - Oscillator for detials.
32	**GPIO13** General Purpose Digital I/O. May be configured as General Purpose Input 13 (GPI13) or General Purpose Output 13 (GPO13). **AI7** Analog Input 7. Not to exceed 3.3VDC. Resolution: 12 bit. The following pins are required for Analog Input functionality: 14, 15, 17. Related Analog Input Pins: 8, 10, 11, 13, 28, 29, 30, 32

TABLE 2 - Pin Details	
Pin #	**Description**
33	**XTAL2** On-board Oscillator Amplifier output. See Section 6.3 - Oscillator for detials.
34	**GPIO28** General Purpose Digital I/O. May be configured as General Purpose Input 28 (GPI28) or General Purpose Output 28 (GPO28). **Pin is Open Drain. When used as GPIO, a pull-up resistor is required for proper operation.** **I2C_SCL0** I^2C Port 0 Clock Line. This line is used to communicate to I^2C devices. Pull-up resistors (1.4K Ohm) are required for proper operation. The following pins are required for Port 0 I^2C functionality: 34, 35.
35	**GPIO27** General Purpose Digital I/O. May be configured as General Purpose Input 27 (GPI27) or General Purpose Output 27 (GPO27). **Pin is Open Drain. When used as GPIO, a pull-up resistor is required for proper operation.** **I2C_SDA0** I^2C Port 0 Data Line. This line is used to communicate to I^2C devices. Pull-up resistors (1.4K Ohm) are required for proper operation. The following pins are required for Port 0 I^2C functionality: 34, 35.
36	**GPIO31** General Purpose Digital I/O. May be configured as General Purpose Input 31 (GPI31) or General Purpose Output 31 (GPO31).
37	**Not Connected** Do Not Connect this pin.
38	**GPIO122** General Purpose Digital I/O. May be configured as General Purpose Input 122 (GPI122) or General Purpose Output 122 (GPO122). **PWM2** Pulse Width Modulation Output 2 (PWM2).
39	**GPIO121** General Purpose Digital I/O. May be configured as General Purpose Input 121 (GPI121) or General Purpose Output 121 (GPO121). **PWM1** Pulse Width Modulation Output 1 (PWM1).
40	**GPIO120** General Purpose Digital I/O. May be configured as General Purpose Input 120 (GPI120) or General Purpose Output 120 (GPO120). **PWM0** Pulse Width Modulation Output 0 (PWM0).
41	**VDD2** Connect to 3.3VDC Supply. The recommended bypass capacitor must be installed near this pin (this pin to GND / 3.3V COMMON).

TABLE 2 - Pin Details	
Pin #	**Description**
42	**GPIO29** General Purpose Digital I/O. May be configured as General Purpose Input 29 (GPI29) or General Purpose Output 29 (GPO29). Note: GPIO29 and GPIO30 must both be input or output as a pair. One cannot be input while the other is an output.
43	**GPIO30** General Purpose Digital I/O. May be configured as General Purpose Input 30 (GPI30) or General Purpose Output 30 (GPO30). Note: GPIO29 and GPIO30 must both be input or output as a pair. One cannot be input while the other is an output.
44	**VSS2** Connect to GND / 3.3V COMMON.
45	**GPIO119** General Purpose Digital I/O. May be configured as General Purpose Input 119 (GPI119) or General Purpose Output 119 (GPO119).
46	**GPIO50** General Purpose Digital I/O. May be configured as General Purpose Input 50 (GPI50) or General Purpose Output 50 (GPO50). **TMR_CAP1.0** Capture input for Timer Module 1, Channel 0. Timer Module 1 supports two input pins: Channel 0 and Channel 1. Only one channel may be used as a timer capture pin in any Timer Module. This setting must match the configuration in EZ LADDER Toolkit. Based on the software configuration, either pin (when selected) will operate as a counter or will caculate the time/frequency of pulses. The following pins are related for Timer Module 1 functionality: 46, 47, 51.
47	**GPIO51** General Purpose Digital I/O. May be configured as General Purpose Input 51 (GPI51) or General Purpose Output 51 (GPO51). **TMR_CAP1.1** Capture input for Timer Module 1, Channel 1. Timer Module 1 supports two input pins: Channel 0 and Channel 1. Only one channel may be used as a timer capture pin in any Timer Module. This setting must match the configuration in EZ LADDER Toolkit. Based on the software configuration, either pin (when selected) will operate as a counter or will caculate the time/frequency of pulses. The following pins are related for Timer Module 1 functionality: 46, 47, 51.
48	**GPIO14** General Purpose Digital I/O. May be configured as General Purpose Input 14 (GPI14) or General Purpose Output 14 (GPO14).
49	**GPIO52** General Purpose Digital I/O. May be configured as General Purpose Input 52 (GPI52) or General Purpose Output 52 (GPO52). **QEI_PHA** Qudrature Encoder Encoder Phase A (A Channel) input. The P10-Series supports an on-board quadrature encoder that provides inputs for Phase A, Phase B and Index. The following pins are required for on-board Quadrature Encoder Interface functionality: 49, 53, 54.

TABLE 2 - Pin Details	
Pin #	**Description**
50	**GPIO53** General Purpose Digital I/O. May be configured as General Purpose Input 53 (GPI53) or General Purpose Output 53 (GPO53).
51	**GPIO54** General Purpose Digital I/O. May be configured as General Purpose Input 54 (GPI54) or General Purpose Output 54 (GPO54). **TMR_MAT1** NOTE 1 Timer/Capture Channel 1 Match output. This output is HIGH based on Timer/Capture Channel 1's configuration and when the captured or timed value equals a predetermined set point. The following pins are related for Timer Module 1 functionality: 46, 47, 51.
52	**GPIO128** General Purpose Digital I/O. May be configured as General Purpose Input 128 (GPI128) or General Purpose Output 128 (GPO128). **LCD_D0** Data 0 Line for LCD Display Port. Supports up to 4 Line, 20 Character Liquid Crystal Display (LCD). See LCD under *Section 5: Functional Descriptions*. The following pins are required for LCD functionality: 52, 55, 58, 68, 72, 74, 78, 84, 88, 91, 94.
53	**GPIO55** General Purpose Digital I/O. May be configured as General Purpose Input 55 (GPI55) or General Purpose Output 55 (GPO55). **QEI_PHB** Qudrature Encoder Encoder Phase B (B Channel) input. The P10-Series supports an on-board quadrature encoder that provides inputs for Phase A, Phase B and Index. The following pins are required for on-board Quadrature Encoder Interface functionality: 49, 53, 54.
54	**GPIO56** General Purpose Digital I/O. May be configured as General Purpose Input 56 (GPI56) or General Purpose Output 56 (GPO56). **QEI_IDX** Qudrature Encoder Encoder Phase Index input. The P10-Series supports an on-board quadrature encoder that provides inputs for Phase A, Phase B and Index. The index input must be pulled high or low based on desired functionality if the connected encoder does not support the index channel. The following pins are required for on-board Quadrature Encoder Interface functionality: 49, 53, 54.
55	**GPIO129** General Purpose Digital I/O. May be configured as General Purpose Input 129 (GPI129) or General Purpose Output 129 (GPO129). **LCD_D1** Data 1 Line for LCD Display Port. Supports up to 4 Line, 20 Character Liquid Crystal Display (LCD). See LCD under *Section 5: Functional Descriptions*. The following pins are required for LCD functionality: 52, 55, 58, 68, 72, 74, 78, 84, 88, 91, 94.
56	**GPIO57** General Purpose Digital I/O. May be configured as General Purpose Input 57 (GPI57) or General Purpose Output 57 (GPO57).

TABLE 2 - Pin Details

Pin #	Description
57	**GPIO58** General Purpose Digital I/O. May be configured as General Purpose Input 58 (GPI58) or General Purpose Output 58 (GPO58). **TMR_CAP0.0** Capture input for Timer Module 0, Channel 0. Timer Module 0 supports two input pins: Channel 0 and Channel 1. Only one channel may be used as a timer capture pin in any Timer Module. This setting must match the configuration in EZ LADDER Toolkit. Based on the software configuration, either pin (when selected) will operate as a counter or will caculate the time/frequency of pulses. The following pins are related for Timer Module 0 functionality: 57, 61, 63.
58	**GPIO130** General Purpose Digital I/O. May be configured as General Purpose Input 130 (GPI130) or General Purpose Output 130 (GPO130). **LCD_D2** Data 2 Line for LCD Display Port. Supports up to 4 Line, 20 Character Liquid Crystal Display (LCD). See LCD under *Section 5: Functional Descriptions*. The following pins are required for LCD functionality: 52, 55, 58, 68, 72, 74, 78, 84, 88, 91, 94.
59	**VSS3** Connect to GND / 3.3V COMMON.
60	**VDD3** Connect to 3.3VDC Supply. The recommended bypass capacitor must be installed near this pin (this pin to GND / 3.3V COMMON).
61	**GPIO59** General Purpose Digital I/O. May be configured as General Purpose Input 59 (GPI59) or General Purpose Output 59 (GPO59). **TMR_CAP0.1** Capture input for Timer Module 0, Channel 1. Timer Module 0 supports two input pins: Channel 0 and Channel 1. Only one channel may be used as a timer capture pin in any Timer Module. This setting must match the configuration in EZ LADDER Toolkit. Based on the software configuration, either pin (when selected) will operate as a counter or will caculate the time/frequency of pulses. The following pins are related for Timer Module 0 functionality: 57, 61, 63.
62	**VDD4** Connect to 3.3VDC Supply. The recommended bypass capacitor must be installed near this pin (this pin to GND / 3.3V COMMON).
63	**GPIO60** General Purpose Digital I/O. May be configured as General Purpose Input 60 (GPI60) or General Purpose Output 60 (GPO60). **TMR_MAT0** NOTE 1 Timer/Capture Channel 0 Match output. This output is HIGH based on Timer/Capture Channel 0's configuration and when the captured or timed value equals a predetermined set point. The following pins are related for Timer Module 0 functionality: 57, 61, 63.

TABLE 2 - Pin Details	
Pin #	**Description**
64	**GPIO61** General Purpose Digital I/O. May be configured as General Purpose Input 61 (GPI61) or General Purpose Output 61 (GPO61). **MCI_CARD_PRESENT** Detects when SD Card is installed in SD Socket. Only required if SD Card socket supports a card present function. The following pins are required for SD Card functionality: 64, 71, 73, 75, 80, 82, 83, 85.
65	**VSS4** Connect to GND / 3.3V COMMON.
66	**GPIO0** General Purpose Digital I/O. May be configured as General Purpose Input 0 (GPI0) or General Purpose Output 0 (GPO0). **CAN_RX0** Receive Line for CAN Port 0. Supports OptiCAN, SAE 1939. The following pins are required for CAN Port 0 functionality: 66, 67. **I2C_SDA1** I^2C Port 1 Data Line. This line is used to communicate to I^2C devices. Pull-up resistors (1.4K Ohm) are required for proper operation. The following pins are required for Port 1 I^2C functionality: 66, 67.
67	**GPIO1** General Purpose Digital I/O. May be configured as General Purpose Input 1 (GPI1) or General Purpose Output 1 (GPO1). **CAN_TX0** Transmit Line for CAN Port 0. Supports OptiCAN, SAE 1939. The following pins are required for CAN Port 0 functionality: 66, 67. **I2C_SCL1** I^2C Port 1 Clock Line. This line is used to communicate to I^2C devices. Pull-up resistors (1.4K Ohm) are required for proper operation. The following pins are required for Port 1 I^2C functionality: 66, 67.
68	**GPIO131** General Purpose Digital I/O. May be configured as General Purpose Input 131 (GPI131) or General Purpose Output 131 (GPO131). **LCD_D3** Data 3 Line for LCD Display Port. Supports up to 4 Line, 20 Character Liquid Crystal Display (LCD). See LCD under *Section 5: Functional Descriptions*. The following pins are required for LCD functionality: 52, 55, 58, 68, 72, 74, 78, 84, 88, 91, 94.
69	**GPIO10** General Purpose Digital I/O. May be configured as General Purpose Input 10 (GPI10) or General Purpose Output 10 (GPO10). **I2C_SDA2** I^2C Port 2 Data Line. This line is used to communicate to I^2C devices. Pull-up resistors (1.4K Ohm) are required for proper operation. The following pins are required for Port 2 I^2C functionality: 69, 70

TABLE 2 - Pin Details	
Pin #	**Description**
70	**GPIO11** General Purpose Digital I/O. May be configured as General Purpose Input 11 (GPI11) or General Purpose Output 11 (GPO11). **I2C_SCL2** I^2C Port 2 Clock Line. This line is used to communicate to I^2C devices. Pull-up resistors (1.4K Ohm) are required for proper operation. The following pins are required for Port 2 I^2C functionality: 69, 70
71	**GPIO77** General Purpose Digital I/O. May be configured as General Purpose Input 77 (GPI77) or General Purpose Output 77 (GPO77). **MCI_DATA3** Data Line 3 for SD Card Interface. The following pins are required for SD Card functionality: 64, 71, 73, 75, 80, 82, 83, 85.
72	**GPIO132** General Purpose Digital I/O. May be configured as General Purpose Input 132 (GPI132) or General Purpose Output 132 (GPO132). **LCD_D4** Data 4 Line for LCD Display Port. Supports up to 4 Line, 20 Character Liquid Crystal Display (LCD). See LCD under *Section 5: Functional Descriptions*. The following pins are required for LCD functionality: 52, 55, 58, 68, 72, 74, 78, 84, 88, 91, 94.
73	**GPIO76** General Purpose Digital I/O. May be configured as General Purpose Input 76 (GPI76) or General Purpose Output 76 (GPO76). **MCI_DATA2** Data Line 2 for SD Card Interface. The following pins are required for SD Card functionality: 64, 71, 73, 75, 80, 82, 83, 85.
74	**GPIO133** General Purpose Digital I/O. May be configured as General Purpose Input 133 (GPI133) or General Purpose Output 133 (GPO133). **LCD_D5** Data 5 Line for LCD Display Port. Supports up to 4 Line, 20 Character Liquid Crystal Display (LCD). See LCD under *Section 5: Functional Descriptions*. The following pins are required for LCD functionality: 52, 55, 58, 68, 72, 74, 78, 84, 88, 91, 94.
75	**GPIO75** General Purpose Digital I/O. May be configured as General Purpose Input 75 (GPI75) or General Purpose Output 75 (GPO75). **MCI_DATA1** Data Line 1 for SD Card Interface. The following pins are required for SD Card functionality: 64, 71, 73, 75, 80, 82, 83, 85.

TABLE 2 - Pin Details

Pin #	Description
76	**LED_KERNEL** This connects to an LED and provides the current status of the PLC on a Chip™'s condition: No Kernel Installed, User Program not executing, User Program executing. This pin must be pulled to 3.3V by approximately a 4.7K ohm resistor. **If this pin is not pulled high, the PLC on a Chip will not operate.** See Section 6.20 - Watchdog LED Circuit for details.
77	**VDD5** Connect to 3.3VDC Supply. The recommended bypass capacitor must be installed near this pin (this pin to GND / 3.3V COMMON).
78	**GPIO134** General Purpose Digital I/O. May be configured as General Purpose Input 134 (GPI134) or General Purpose Output 134 (GPO134). **LCD_D6** Data 6 Line for LCD Display Port. Supports up to 4 Line, 20 Character Liquid Crystal Display (LCD). See LCD under *Section 5: Functional Descriptions*. The following pins are required for LCD functionality: 52, 55, 58, 68, 72, 74, 78, 84, 88, 91, 94.
79	**VSS5** Connect to GND / 3.3V COMMON.
80	**GPIO22** General Purpose Digital I/O. May be configured as General Purpose Input 22 (GPI22) or General Purpose Output 22 (GPO22). **MCI_DATA0** Data Line 0 for SD Card Interface. The following pins are required for SD Card functionality: 64, 71, 73, 75, 80, 82, 83, 85.
81	**GPIO162** General Purpose Digital I/O. May be configured as General Purpose Input 162 (GPI162) or General Purpose Output 162 (GPO162). **Pin is Open Drain. A pull-up resistor is required for proper operation.**
82	**GPIO21** General Purpose Digital I/O. May be configured as General Purpose Input 21 (GPI21) or General Purpose Output 21 (GPO21). **MCI_PWR** Power Supply Enable for external SD Card power supply. The following pins are required for SD Card functionality: 64, 71, 73, 75, 80, 82, 83, 85.
83	**GPIO20** General Purpose Digital I/O. May be configured as General Purpose Input 20 (GPI20) or General Purpose Output 20 (GPO20). **MCI_CMD** Command line for SD Card Interface. The following pins are required for SD Card functionality: 64, 71, 73, 75, 80, 82, 83, 85.

TABLE 2 - Pin Details

Pin #	Description
84	**GPIO135** General Purpose Digital I/O. May be configured as General Purpose Input 135 (GPI135) or General Purpose Output 135 (GPO135). **LCD_D7** Data 7 Line for LCD Display Port. Supports up to 4 Line, 20 Character Liquid Crystal Display (LCD). See LCD under *Section 5: Functional Descriptions*. The following pins are required for LCD functionality: 52, 55, 58, 68, 72, 74, 78, 84, 88, 91, 94.
85	**GPIO19** General Purpose Digital I/O. May be configured as General Purpose Input 19 (GPI19) or General Purpose Output 19 (GPO19). **MCI_CLK** Clock output line for SD Card Interface. The following pins are required for SD Card functionality: 64, 71, 73, 75, 80, 82, 83, 85.
86	**GPIO18** General Purpose Digital I/O. May be configured as General Purpose Input 18 (GPI18) or General Purpose Output 18 (GPO18). **SPI_MOSI0** Master Out - Slave In Output for SPI Port 0. The following pins are required for SPI Port 0 functionality: 86, 87, 89. Any *GPIO* to act as a Chip Select for each SPI device on the bus.
87	**GPIO17** General Purpose Digital I/O. May be configured as General Purpose Input 17 (GPI17) or General Purpose Output 17 (GPO17). **SPI_MISO0** Master In - Slave Out Input for SPI Port 0. The following pins are required for SPI Port 0 functionality: 86, 87, 89. Any *GPIO* to act as a Chip Select for each SPI device on the bus.
88	**GPIO136** General Purpose Digital I/O. May be configured as General Purpose Input 136 (GPI136) or General Purpose Output 136 (GPO136). **LCD_RS** Register Select Line for LCD Display Port. Supports up to 4 Line, 20 Character Liquid Crystal Display (LCD). See LCD under *Section 5: Functional Descriptions*. The following pins are required for LCD functionality: 52, 55, 58, 68, 72, 74, 78, 84, 88, 91, 94.
89	**GPIO15** General Purpose Digital I/O. May be configured as General Purpose Input 15 (GPI15) or General Purpose Output 15 (GPO15). **SPI_SCK0** Serial Clock Output for SPI Port 0. The following pins are required for SPI Port 0 functionality: 86, 87, 89. Any *GPIO* to act as a Chip Select for each SPI device on the bus.

TABLE 2 - Pin Details

Pin #	Description
90	**GPIO16** General Purpose Digital I/O. May be configured as General Purpose Input 16 (GPI16) or General Purpose Output 16 (GPO16). **LOW_VOLT_SENSE** Low voltage sense input. Used for Retentive Memory Storage. On falling edge, all retentive variables are written to non-volatile memory (provided sufficient power supply time for processor to complete store).
91	**GPIO137** General Purpose Digital I/O. May be configured as General Purpose Input 137 (GPI137) or General Purpose Output 137 (GPO137). **LCD_RW** Read / Write Line for LCD Display Port. Supports up to 4 Line, 20 Character Liquid Crystal Display (LCD). See LCD under *Section 5: Functional Descriptions*. The following pins are required for LCD functionality: 52, 55, 58, 68, 72, 74, 78, 84, 88, 91, 94.
92	**GPIO73** General Purpose Digital I/O. May be configured as General Purpose Input 73 (GPI73) or General Purpose Output 73 (GPO73). **RXD2** UART 2 Receive Line. UART 2 supports transmit and receive only. If handshaking is required, use UART 1. The following pins are related for UART2 functionality: 92, 93.
93	**GPIO72** General Purpose Digital I/O. May be configured as General Purpose Input 72 (GPI72) or General Purpose Output 72 (GPO72). **TXD2** UART 2 Transmit Line. UART 2 supports transmit and receive only. If handshaking is required, use UART 1. The following pins are related for UART2 functionality: 92, 93.
94	**GPIO138** General Purpose Digital I/O. May be configured as General Purpose Input 138 (GPI138) or General Purpose Output 138 (GPO138). **LCD_E** Enable Line for LCD Display Port. Supports up to 4 Line, 20 Character Liquid Crystal Display (LCD). See LCD under *Section 5: Functional Descriptions*. The following pins are required for LCD functionality: 52, 55, 58, 68, 72, 74, 78, 84, 88, 91, 94.
95	**GPIO71** General Purpose Digital I/O. May be configured as General Purpose Input 71 (GPI71) or General Purpose Output 71 (GPO71). **RTS1** UART 1 Request To Send Line. UART 1 supports full handshaking hardware functionality. The following pins are related for UART 1 functionality: 96, 96, 97, 99, 100, 105, 106, 107.

TABLE 2 - Pin Details	
Pin #	**Description**
96	**GPIO70** General Purpose Digital I/O. May be configured as General Purpose Input 70 (GPI70) or General Purpose Output 70 (GPO70). **RI1** UART 1 Ring Indicator Line. UART 1 supports full handshaking hardware functionality. The following pins are related for UART 1 functionality: 96, 96, 97, 99, 100, 105, 106, 107.
97	**GPIO69** General Purpose Digital I/O. May be configured as General Purpose Input 69 (GPI69) or General Purpose Output 69 (GPO69). **DTR1** UART 1 Data Terminal Ready Line. UART 1 supports full handshaking hardware functionality. The following pins are related for UART 1 functionality: 96, 96, 97, 99, 100, 105, 106, 107.
98	**GPIO163** General Purpose Digital I/O. May be configured as General Purpose Input 163 (GPI163) or General Purpose Output 163 (GPO163). **Pin is Open Drain. When used as GPIO, a pull-up resistor is required for proper operation.** **RXD4** UART 4 Receive Line. UART 4 supports transmit and receive only. If handshaking is required, use UART 1. The following pins are related for UART4 functionality: 98, 143
99	**GPIO68** General Purpose Digital I/O. May be configured as General Purpose Input 68 (GPI68) or General Purpose Output 68 (GPO68). **DSR1** UART 1 Data Set Ready Line. UART 1 supports full handshaking hardware functionality. The following pins are related for UART 1 functionality: 96, 96, 97, 99, 100, 105, 106, 107.
100	**GPIO67** General Purpose Digital I/O. May be configured as General Purpose Input 67 (GPI67) or General Purpose Output 67 (GPO67). **DCD1** UART 1 Data Carrier Detect Line. UART 1 supports full handshaking hardware functionality. The following pins are related for UART 1 functionality: 96, 96, 97, 99, 100, 105, 106, 107.
101	**GPIO139** General Purpose Digital I/O. May be configured as General Purpose Input 139 (GPI139) or General Purpose Output 139 (GPO139). **KEYPAD_COL1** Keypad Column 1 line. Supports a 5 column, 4 row keypad matrix. The following pins are required for KEYPAD functionality: 101, 104, 108, 110, 120, 124, 127, 130, 134
102	**VDD6** Connect to 3.3VDC Supply. The recommended bypass capacitor must be installed near this pin (this pin to GND / 3.3V COMMON).
103	**VSS6** Connect to GND / 3.3V COMMON.

TABLE 2 - Pin Details

Pin #	Description
104	**GPIO140** General Purpose Digital I/O. May be configured as General Purpose Input 140 (GPI140) or General Purpose Output 140 (GPO140). **KEYPAD_COL2** Keypad Column 2 line. Supports a 5 column, 4 row keypad matrix. The following pins are required for KEYPAD functionality: 101, 104, 108, 110, 120, 124, 127, 130, 134
105	**GPIO66** General Purpose Digital I/O. May be configured as General Purpose Input 66 (GPI66) or General Purpose Output 66 (GPO66). **CTS1** UART 1 Clear To Send Line. UART 1 supports full handshaking hardware functionality. The following pins are related for UART 1 functionality: 96, 96, 97, 99, 100, 105, 106, 107.
106	**GPIO65** General Purpose Digital I/O. May be configured as General Purpose Input 65 (GPI65) or General Purpose Output 65 (GPO65). **RXD1** UART 1 Receive Line. UART 1 supports full handshaking hardware functionality. The following pins are related for UART 1 functionality: 96, 96, 97, 99, 100, 105, 106, 107.
107	**GPIO64** General Purpose Digital I/O. May be configured as General Purpose Input 64 (GPI64) or General Purpose Output 64 (GPO64). **TXD1** UART 1 Transmit Line. UART 1 supports full handshaking hardware functionality. The following pins are related for UART 1 functionality: 96, 96, 97, 99, 100, 105, 106, 107.
108	**GPIO141** General Purpose Digital I/O. May be configured as General Purpose Input 141 (GPI141) or General Purpose Output 141 (GPO141). **KEYPAD_COL3** Keypad Column 3 line. Supports a 5 column, 4 row keypad matrix. The following pins are required for KEYPAD functionality: 101, 104, 108, 110, 120, 124, 127, 130, 134
109	**GPIO9** General Purpose Digital I/O. May be configured as General Purpose Input 9 (GPI9) or General Purpose Output 9 (GPO9). **SPI_MOSI1** Master Out - Slave In Output for SPI Port 1. The following pins are required for SPI Port 1 functionality: 109, 111, 112. Any *GPIO* to act as a Chip Select for each SPI device on the bus.
110	**GPIO142** General Purpose Digital I/O. May be configured as General Purpose Input 142 (GPI142) or General Purpose Output 142 (GPO142). **KEYPAD_COL4** Keypad Column 4 line. Supports a 5 column, 4 row keypad matrix. The following pins are required for KEYPAD functionality: 101, 104, 108, 110, 120, 124, 127, 130, 134

TABLE 2 - Pin Details	
Pin #	**Description**
111	**GPIO8** General Purpose Digital I/O. May be configured as General Purpose Input 8 (GPI8) or General Purpose Output 8 (GPO8). **SPI_MISO1** Master In - Slave Out Input for SPI Port 1. The following pins are required for SPI Port 1 functionality: 109, 111, 112. Any *GPIO* to act as a Chip Select for each SPI device on the bus.
112	**GPIO7** General Purpose Digital I/O. May be configured as General Purpose Input 7 (GPI7) or General Purpose Output 7 (GPO7). **SPI_SCK1** Serial Clock Output for SPI Port 1. The following pins are required for SPI Port 1 functionality: 109, 111, 112. Any *GPIO* to act as a Chip Select for each SPI device on the bus.
113	**GPIO6** General Purpose Digital I/O. May be configured as General Purpose Input 6 (GPI6) or General Purpose Output 6 (GPO6).
114	**VDD7** Connect to 3.3VDC Supply. The recommended bypass capacitor must be installed near this pin (this pin to GND / 3.3V COMMON).
115	**GPIO5** General Purpose Digital I/O. May be configured as General Purpose Input 5 (GPI5) or General Purpose Output 5 (GPO5). **CAN_TX1** Transmit Line for CAN Port 1. Supports OptiCAN, SAE 1939. The following pins are required for CAN Port 1 functionality: 115, 116
116	**GPIO4** General Purpose Digital I/O. May be configured as General Purpose Input 4 (GPI4) or General Purpose Output 4 (GPO4). **CAN_RX1** Receive Line for CAN Port 1. Supports OptiCAN, SAE 1939. The following pins are required for CAN Port 1 functionality: 115, 116
117	**VSS7** Connect to GND / 3.3V COMMON.
118	**GPIO156** General Purpose Digital I/O. May be configured as General Purpose Input 156 (GPI156) or General Purpose Output 156 (GPO156). **TXD3** UART 3 Transmit Line. UART 3 supports transmit and receive only. If handshaking is required, use UART 1. The following pins are related for UART3 functionality: 118, 122.
119	**VSS8** Connect to GND / 3.3V COMMON.

TABLE 2 - Pin Details

Pin #	Description
120	**GPIO143** General Purpose Digital I/O. May be configured as General Purpose Input 143 (GPI143) or General Purpose Output 143 (GPO143). **KEYPAD_COL5** Keypad Column 5 line. Supports a 5 column, 4 row keypad matrix. The following pins are required for KEYPAD functionality: 101, 104, 108, 110, 120, 124, 127, 130, 134
121	**VDD8** Connect to 3.3VDC Supply. The recommended bypass capacitor must be installed near this pin (this pin to GND / 3.3V COMMON).
122	**GPIO157** General Purpose Digital I/O. May be configured as General Purpose Input 157 (GPI157) or General Purpose Output 157 (GPO157). **RXD3** UART 3 Receive Line. UART 3 supports transmit and receive only. If handshaking is required, use UART 1. The following pins are related for UART3 functionality: 118, 122.
123	**GPIO49** General Purpose Digital I/O. May be configured as General Purpose Input 49 (GPI49) or General Purpose Output 49 (GPO49). **ETHER_MDIO** Ethernet MDIO input/output. Used as Ethernet MIIm data input and output. Typically connects to MDIO port on an Ethernet Physical Integrated Circuit. The following pins are required for Ethernet functionality: 123, 125, 126, 128, 129, 131, 132, 133, 135, 136.
124	**GPIO153** General Purpose Digital I/O. May be configured as General Purpose Input 153 (GPI153) or General Purpose Output 153 (GPO153). **KEYPAD_ROW2** Keypad Row 2 line. Supports a 5 column, 4 row keypad matrix. The following pins are required for KEYPAD functionality: 101, 104, 108, 110, 120, 124, 127, 130, 134
125	**GPIO48** General Purpose Digital I/O. May be configured as General Purpose Input 48 (GPI48) or General Purpose Output 48 (GPO48). **ETHER_MDC** Ethernet MDIO/MIIM Clock output. Typically connects to MDC port on an Ethernet Physical Integrated Circuit. The following pins are required for Ethernet functionality: 123, 125, 126, 128, 129, 131, 132, 133, 135, 136.
126	**GPIO47** General Purpose Digital I/O. May be configured as General Purpose Input 47 (GPI47) or General Purpose Output 47 (GPO47). **ETHER_REFCLK** Ethernet Reference Clock. Typically connects to X1 port on an Ethernet Physical Integrated Circuit. The following pins are required for Ethernet functionality: 123, 125, 126, 128, 129, 131, 132, 133, 135, 136.

TABLE 2 - Pin Details

Pin #	Description
127	**GPIO152** General Purpose Digital I/O. May be configured as General Purpose Input 152 (GPI152) or General Purpose Output 152 (GPO152). **KEYPAD_ROW1** Keypad Row 1 line. Supports a 5 column, 4 row keypad matrix. The following pins are required for KEYPAD functionality: 101, 104, 108, 110, 120, 124, 127, 130, 134
128	**GPIO46** General Purpose Digital I/O. May be configured as General Purpose Input 46 (GPI46) or General Purpose Output 46 (GPO46). **ETHER_RXER** Ethernet Receive Error input. Typically connects to RXER port on an Ethernet Physical Integrated Circuit. The following pins are required for Ethernet functionality: 123, 125, 126, 128, 129, 131, 132, 133, 135, 136.
129	**GPIO42** General Purpose Digital I/O. May be configured as General Purpose Input 42 (GPI42) or General Purpose Output 42 (GPO42). **ETHER_RXD1** Ethernet Recieve Data 1 Input. Typically connects to RXD1 port on an Ethernet Physical Integrated Circuit. The following pins are required for Ethernet functionality: 123, 125, 126, 128, 129, 131, 132, 133, 135, 136.
130	**GPIO158** General Purpose Digital I/O. May be configured as General Purpose Input 158 (GPI158) or General Purpose Output 158 (GPO158). **KEYPAD_ROW3** Keypad Row 3 line. Supports a 5 column, 4 row keypad matrix. The following pins are required for KEYPAD functionality: 101, 104, 108, 110, 120, 124, 127, 130, 134
131	**GPIO41** General Purpose Digital I/O. May be configured as General Purpose Input 41 (GPI41) or General Purpose Output 41 (GPO41). **ETHER_RXD0** Ethernet Recieve Data 0 Input. Typically connects to RXD0 port on an Ethernet Physical Integrated Circuit. The following pins are required for Ethernet functionality: 123, 125, 126, 128, 129, 131, 132, 133, 135, 136.
132	**GPIO40** General Purpose Digital I/O. May be configured as General Purpose Input 40 (GPI40) or General Purpose Output 40 (GPO40). **ETHER_CRS** Ethernet Carrier Sense Input. Typically connects to CRS port on an Ethernet Physical Integrated Circuit. The following pins are required for Ethernet functionality: 123, 125, 126, 128, 129, 131, 132, 133, 135, 136.

TABLE 2 - Pin Details

Pin #	Description
133	**GPIO36** General Purpose Digital I/O. May be configured as General Purpose Input 36 (GPI36) or General Purpose Output 36 (GPO36). **ETHER_TXEN** Ethernet Transmit Data Enable. Typically connects to TXEN port on an Ethernet Physical Integrated Circuit. The following pins are required for Ethernet functionality: 123, 125, 126, 128, 129, 131, 132, 133, 135, 136.
134	**GPIO159** General Purpose Digital I/O. May be configured as General Purpose Input 159 (GPI159) or General Purpose Output 159 (GPO159). **KEYPAD_ROW4** Keypad Row 4 line. Supports a 5 column, 4 row keypad matrix. The following pins are required for KEYPAD functionality: 101, 104, 108, 110, 120, 124, 127, 130, 134
135	**GPIO33** General Purpose Digital I/O. May be configured as General Purpose Input 33 (GPI33) or General Purpose Output 33 (GPO33). **ETHER_TXD1** Ethernet Transmit Data 1 Output. Typically connects to TXD1 port on an Ethernet Physical Integrated Circuit. The following pins are required for Ethernet functionality: 123, 125, 126, 128, 129, 131, 132, 133, 135, 136.
136	**GPIO32** General Purpose Digital I/O. May be configured as General Purpose Input 32 (GPI32) or General Purpose Output 32 (GPO32). **ETHER_TXD0** Ethernet Transmit Data 0 Output. Typically connects to TXD0 port on an Ethernet Physical Integrated Circuit. The following pins are required for Ethernet functionality: 123, 125, 126, 128, 129, 131, 132, 133, 135, 136.
137	**GPIO96** General Purpose Digital I/O. May be configured as General Purpose Input 96 (GPI96) or General Purpose Output 96 (GPO96).
138	**VDD9** Connect to 3.3VDC Supply. The recommended bypass capacitor must be installed near this pin (this pin to GND / 3.3V COMMON).
139	**VSS9** Connect to GND / 3.3V COMMON.
140	**GPIO97** General Purpose Digital I/O. May be configured as General Purpose Input 97 (GPI97) or General Purpose Output 97 (GPO97).
141	**TXDO** UART 0 (Program Port) Transmit Line. Used as EZ LADDER Programming Port only. UART 0 supports transmit and receive only. The following pins are related for UART0 functionality: 141, 142

TABLE 2 - Pin Details	
Pin #	**Description**
142	**RXDO** UART 0 (Program Port) Receive Line. Used as EZ LADDER Programming Port only. UART 0 supports transmit and receive only. The following pins are related for UART0 functionality: 141, 142
143	**GPIO164** General Purpose Digital I/O. May be configured as General Purpose Input 164 (GPI164) or General Purpose Output 164 (GPO164). **TXD4** UART 4 Transmit Line. UART 4 supports transmit and receive only. If handshaking is required, use UART 1. The following pins are related for UART4 functionality: 98, 143
144	**GPIO98** General Purpose Digital I/O. May be configured as General Purpose Input 98 (GPI98) or General Purpose Output 98 (GPO98).
NOTE 1: This functionality is not available at this time, but may be implemented with future EZ LADDER Toolkit releases.	

6. Functional Descriptions & Circuit Examples

NOTICE

Divelbiss reserves the right to discontinue or make changes to it's products without notice. As the circuits are provided for reference only, customers assume the responsibility for the appropriate application of Divelbiss components. It is the customer's responsibility to ensure that adequate design and operating safeguards are addressed to eliminate any hazards inherent to their application.

To aid in implementing the PLCHIP-P10-51220, this section is organized by circuit function and provides details for electrical requirements, connections recommendations, example circuit diagrams and layout considerations.

This datasheet provides hardware information and support only. For programming, including functions and supported features, please refer to the P-Series EZ LADDER Toolkit User Manual.

For electrical noise immunity, it is recommended the PLCHIP-P10-51220 be implemented on a printed circuit board with at least a 4-layers (one inner ground and one inner power plane).

6.1 VDD Power Pins

The P-Series PLC on a Chip™ power supply is 3.3VDC. The power is connected to the following pins [Description (Pin #)]:

Function	Pin #	Function	Pin#	Function	Pin#

VDD 1	18	VDD 4	62	VDD 7	114
VDD 2	41	VDD 5	77	VDD 8	121
VDD 3	60	VDD 6	102	VDD 9	138

Bypass Capacitors should be placed as near VDD pins as possible.

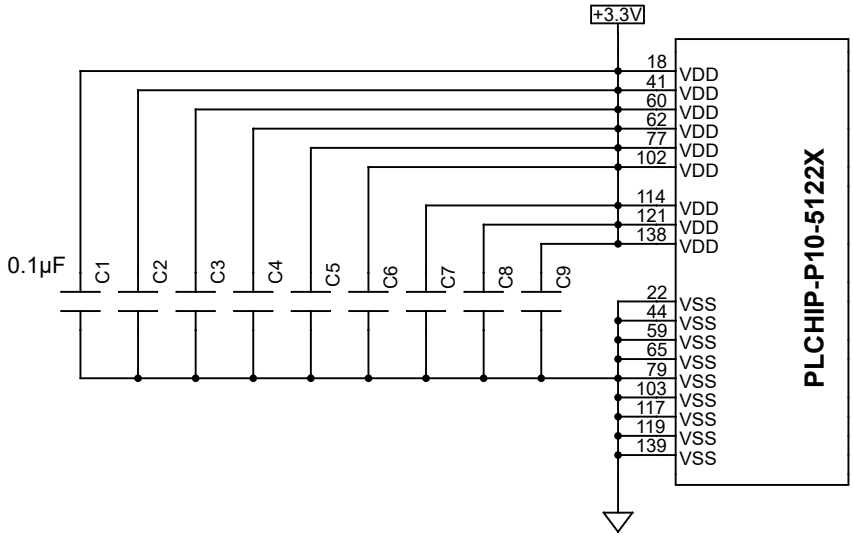


Diagram 6.1A - Example Power Connections & Bypass Capacitors Schematic

A .1µF bypass capacitor should be connected from each VDD*x* pin to the ground / common connected to the PLC on a Chip™'s VSS pins. These bypass capacitors should be physically located near each of the VDD*x* pins as possible. Diagram 6.1A is a sample schematic of the required PLCHIP-P10-51220 power and bypass filtering. Refer to Diagram 6.3B for a sample layout of the P-10 Chip, power pins, oscillator and Ethernet.

6.2 VSS Power Pins (GND)

The P-Series PLC on a Chip™ must be connected to the digital ground (3.3V Common) for proper operation. The ground is connected to the following pins [Description (Pin #)]:

Function	Pin #	Function	Pin#	Function	Pin#
VSS 1	22	VSS 4	65	VSS 7	117
VSS 2	44	VSS 5	79	VSS 8	119
VSS 3	59	VSS 6	103	VSS 9	139

Diagram 6.1A is a sample schematic of the required PLCHIP-P10-51220 power and bypass filtering. Refer to Diagram 6.3B for a sample layout of the P-10 Chip, power pins, oscillator and Ethernet.

6.3 Oscillator Input

The PLCHIP-P10-51220 requires an external oscillator input as a source to internal clock generator circuits. This oscillator provides the basis for all internal on-chip clocking and timing functions. The

following pins are required to connect the oscillator to the P-Series PLC on a Chip™: 31 and 33.

A Crystal is recommended as the external oscillator. The following specifications must be adhered to when selecting a crystal.

Frequency:	12 MHz
Crystal Load Capacitance:	20 pF (approximate)
Maximum Crystal Series Resistance:	< 60 Ω
External Load Capacitors C_{X1}, C_{X2}:	22 pF (approximate)

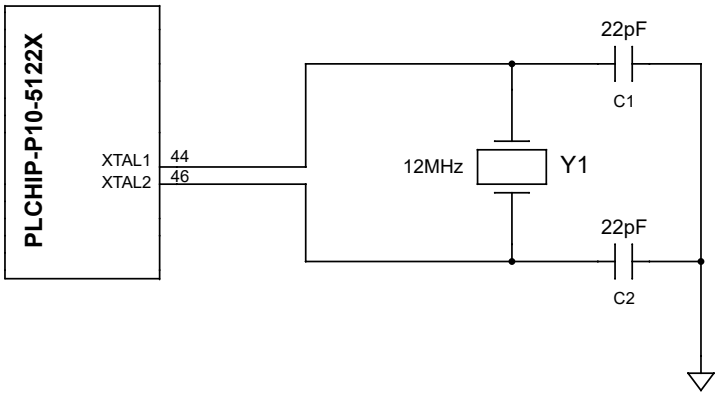


Diagram 6.3A - Example Oscillator Circuit Schematic

Diagram 6.3A is a sample schematic of the recommended oscillator circuit. Refer to Diagram 6.3B for a sample layout of the P-10 Chip, power pins, oscillator and Ethernet.

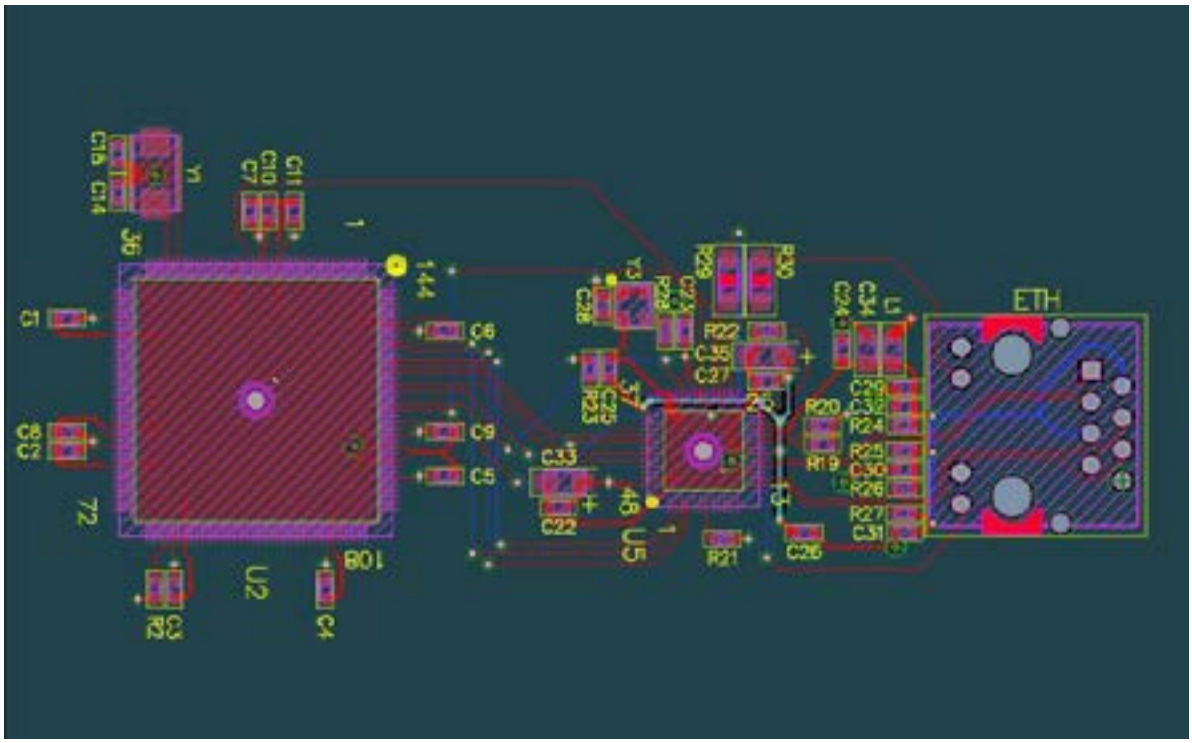


Diagram 6.3B - Sample P-10, Power, Oscillator and Ethernet Layout with 4 Layer PCB

6.4 General Purpose I/O (GPIO)

A versatile feature of the P-Series PLC on a Chip™ is it's large number of configurable Input/Output Points (I/O. These are referred to as General Purpose I/O or GPIO for short. Each GPIO point can be used as either an digital input or a digital output. All GPIO are TTL level designed to operate at 3.3VDC and most are 5VDC tolerant. Additional circuitry is required external to the PLC on a Chip™ for interfacing to real world field devices (input or output).

GPIO functionality is configured using the EZ LADDER Toolkit (programming software). In EZ LADDER Toolkit, each GPIO can be configured independently as an input or an output (provided it is not already in-use as part of another feature/function).

GPIO as Inputs

When configuring the GPIO as digital inputs, each I/O pin is **active low**, requiring a low TTL signal for the input to be considered true. When using GPIO as digital inputs, if debounce circuitry is required (as in for interfaces to push-buttons or other mechanical devices that may not have a clean transistion), it must be added in the interface circuitry. While no hardware debounce is included in the basic (kernel) operation of the P-Series PLC on a Chip™, software debounce can be added in the actual ladder diagram using inputs (GPIO) with timers if required.

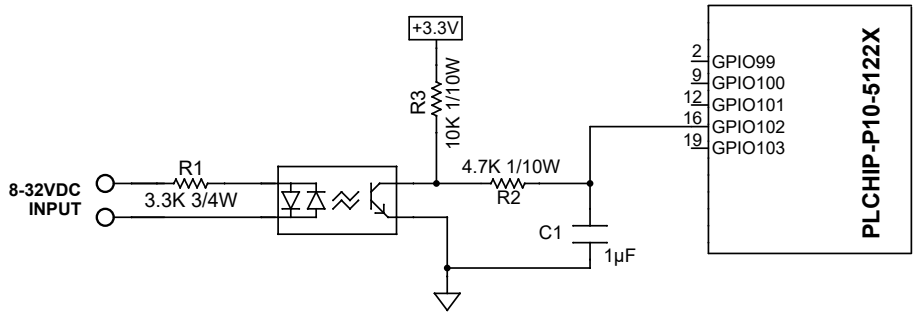


Diagram 6.4A - Example Circuit using GPIO as a Digital Input

Diagram 6.4A is a sample schematic of using a GPIO as a digital input. The example includes the use of an opto-coupler for noise immunity and built in debounce.

GPIO as Outputs

When configuring the GPIO as digital outputs, each I/O pin is **active high**, meaning when the Output is true in the ladder diagram, the actual pin is at a high TTL Level (3.3VDC).

When the PLC on a Chip™ powers up, all GPIO will revert to a default level, enabling internal pull-up resistors. The duration of this time is from power on until the ladder diagram begins executing code. During this time, the pull-ups can cause the outputs can glitch to a true state. If GPIO is used to drive real world outputs such as solenoids, contactors and more, a pull-down resistor is recommended on the GPIO pin. This pull-down resistor will eliminate this power-on glitch.

Please note that while most all pins have a defined GPIO address, many of the pins share functionality with other features such as analog inputs, UARTs, CAN ports and more. Each pin can only function as a single feature; therefore, other features should be implemented and configured (UARTS, analog inputs, Ethernet, etc.) prior to assigning GPIO.

Diagram 6.4B is a sample schematic of using a GPIO as a digital output. The example includes the use of an a relay with a de-glitch pull-down resistor.

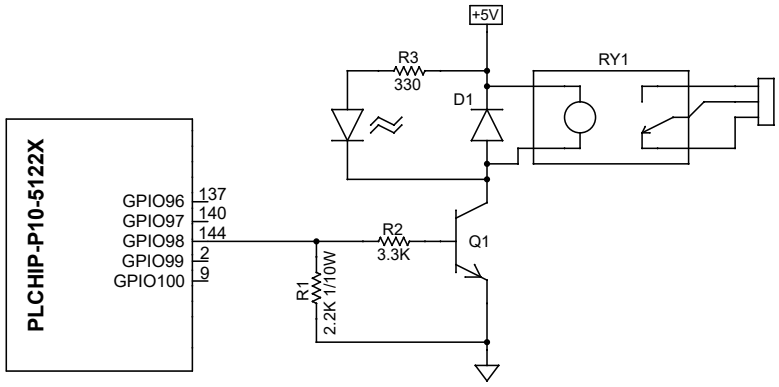


Diagram 6.4B - Example Circuit using GPIO as a Digital Output

6.5 Pulse Width Modulation (PWM) Outputs

Three of the General Purpose I/O (GPIO) are designed to be operated as Pulse Width Modulation (PWM) Outputs. These outputs are TTL level (3.3VDC) and require additional circuitry to interface to real world devices (loads). Pulse Width Modulation output channels 0 to 2 are located on pins **40**, **39**, **38** respectively.

These PWM pins may also be used as General Purpose I/O (GPIO). They do not share any additional functionality other than GPIO.

A Load when connected to a PWM output is controlled essentially by turning a switch between supply and load on and off at a fast pace. The longer the switch is on compared to the off periods, the higher the power supplied to the load is.

When the PLC on a Chip™ powers up, all PWM channels will revert to a default level, enabling internal pull-up resistors. The duration of this time is from power on until the ladder diagram begins executing code. During this time, the pull-ups can cause the outputs can glitch to a true state. If GPIO is used to drive real world outputs such as solenoids, contactors and more, a pull-down resistor is recommended on the GPIO pin. This pull-down resistor will illiminate this power-on glitch.

There are two basic elements to control a PWM output: *Frequency* and *Duty Cycle*.

Frequency

The Frequency is the base frequency of the switching described earlier. The frequency must be sized according to the application. All three channels use the same base frequency. Frequency is set in the ladder diagram program in EZ LADDER Toolkit. The frequency can also be changed in the ladder diagram during normal program operation

Duty Cycle

Duty Cycle represents the proportion of 'on' time to the regular interval or 'period' of time; a low duty cycle corresponds to lower power, because the power is off for most of the time. Duty cycle is expressed in percent where 10% would be low power to the load and 100% would be the load on fully.

Diagram 6.5A is a sample schematic of using a PWM output to drive a load. The example includes the use of a de-glitch pull-down resistor.

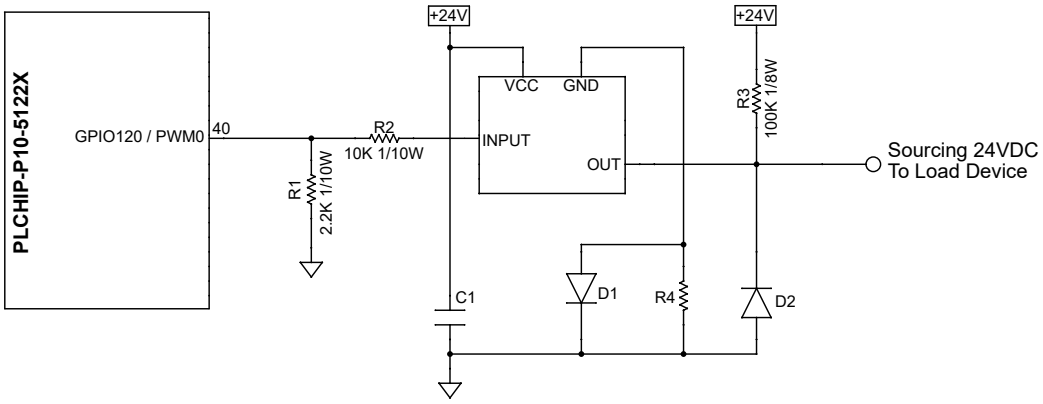


Diagram 6.5A - Example Pulse Width Modulation Output

6.6 Analog I/O

The PLCHIP-P10-51220 supports up to eight on-board analog channels. Some of these eight channels also share functionality with other features; therefore, it is recommended to map all feature pins (such as analog) prior to beginning any design.

Of the eight analog input channels, seven are designated as analog inputs (channels 0, 1, 2, 4, 5, 6, 7). One channel (3) may be configured and used as an analog input (AI3) or as an analog output (AO0). The analog inputs (Channels 0 -7) are located on pins **13**, **11**, **10**, **8**, **30**, **28**, **29** and **32** respectively. The analog output is located on pin **8**.

Additional pin connections are required to use analog I/O. The analog I/O provides pins for its own individual power source (**VDD_AN** and **VSS_AN**) and the analog reference voltage (**VREF_AN**).

VDD_AN
The VDD_AN pin (**pin 14**) is the 3.3 VDC analog supply voltage. Based on application and cost requirements, this pin may be connected to the same 3.3 VDC supply as the VDDx pins or be isolated (separate 3.3V supply) to minimize noise and error. This pin is used to power the analog inputs (ADC) and analog output (DAC). Whenever the analog inputs or analog output is not used, this pin should be connected to 3.3 VDC.

This pin does not share any functionality with other P-10 PLC on a Chip features.

VSS_AN
The VSS_AN pin (**pin 15**) is the 0 VDC power supply and reference for the analog inputs (ADC) and analog output (DAC). This should be connected to the same supply as the VSSx pins but can be isolated to minimize noise and error.

This pin does not share any functionality with other P-10 PLC on a Chip features.

VREF_AN

The VREF_AN pin (pin 17) is the analog positive reference voltage. This should the same voltage level as the supply connected to the VDD_AN (3.3 VDC). It may be connected to the same supply as VDD_AN, but it is recommended to use a precise reference voltage source to minimize noise and error. The voltage level on this pin is used as the reference for the ADC and DAC. The maximum input is 3.3 VDC. Whenever the analog inputs or analog output is not used, this pin should be connected to 3.3 VDC.

This pin does not share any functionality with other P-10 PLC on a Chip features.

AI0 - AI7 (Analog Inputs)

AI0 through AI7 are the analog input pins (13, 11, 10, 8, 30, 28, 29 and 32). Each pin can accept an input signal of 3.3VDC (supply connected to VDD_AN, VREF_AN). The resolution for all on-board analog inputs is 12 bit. Additional circuitry will be required for converting real world analog signals into a 3.3 VDC signal. Any analog input channel with an input voltage higher than 3.3 VDC will cause all analog channels to operate improperly, therefore, steps must be taken to ensure that the voltage of no channel is greater than 3.3 VDC.

Pins 13, 11, 10, 8, 30, 28, 29 and 32 share functionality and may be used as General Purpose I/O (GPIO). Additionally, Pin 8 may also be used as an analog output (AO0).

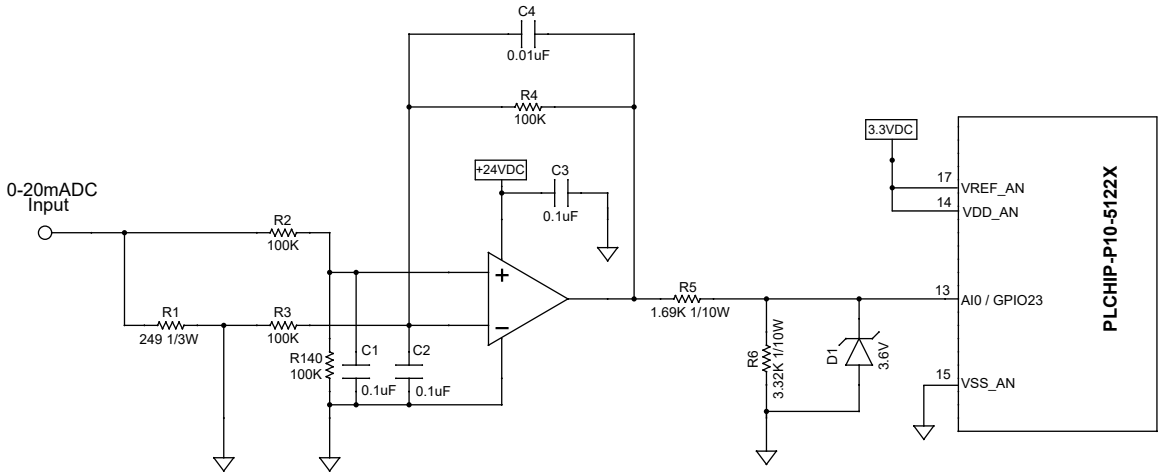


Diagram 6.6A - Example Analog Input Circuit with Scaling

Diagram 6.6A is a sample schematic of an interface circuit for a real world analog input 0-20mADC with conversion for the PLCHIP-P10-51220 analog inputs (3.3 VDC). R5 and R6 provide the voltage divider for the op-amp output and D1 is a 3.6V zener diode for limiting the input to the ADC.

AO0 (Analog Output)

AO0 is the analog output pin (8). This pin can output a variable analog signal from 0 V to 3.3 VDC (supply applied to VDD_AN, VREF_AN). The DAC output resolution is 10 bit.

Pins 8 shares functionality and may be used as General Purpose I/O (GPIO26) or as an analog input (AI3).

Diagram 6.6B is a sample schematic of an interface circuit for a real world device connected to the

DAC output.

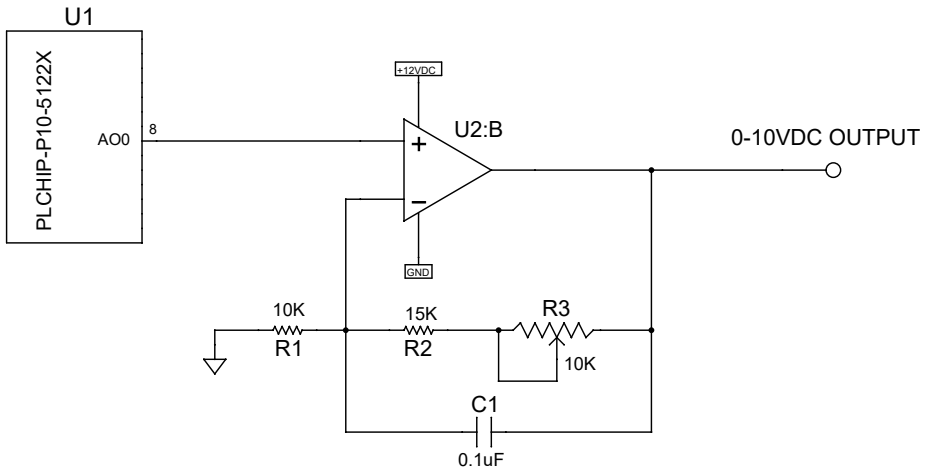


Diagram 6.6B - Example Analog Output Circuit

6.7 SD Card Interface

The PLCHIP-P10-51220 will interface to an SD Card (Secure Digital Card). An SD card is a non-volatile memory card that can be used to store information, update the PLC on a Chip™ kernel and / or ladder diagram and be the 'disk' for files of a local webserver. The SD Card is typically 'plugged-in' to the interface's socket.

To use the SD Card interface functionality, several pins must be used for the interface itself. The following pins are associated with SD Card functionality: **71**, **73**, **75**, **80**, **82**, **83**, **85**, **64.** All the pins except pin 64 are required to interface to an SD Card while pin 64 is an optional feature. These pins only currently share functionality as SD Card Interface I/O or as General Purpose I/O (GPIO).

The required pins are **MCI_CLK**, **MCI_CMD**, **MCI_PWR**, **MCI_DATA0**, **MCI_DATA1**, **MCI_DATA2** and **MCI_DATA3**.

The **MCI_CARD_PRESENT** is an optional pin (64) that is used to detect when an SD Card has been inserted into the SD Card Socket. The socket must also support this feature.

These SD Card pins may also be used as General Purpose I/O (GPIO). They do not share any additional functionality except GPIO.

Diagram 6.7A is a sample schematic of an interface for an SD card using a socket that does not support MCI_CARD_PRESENT.

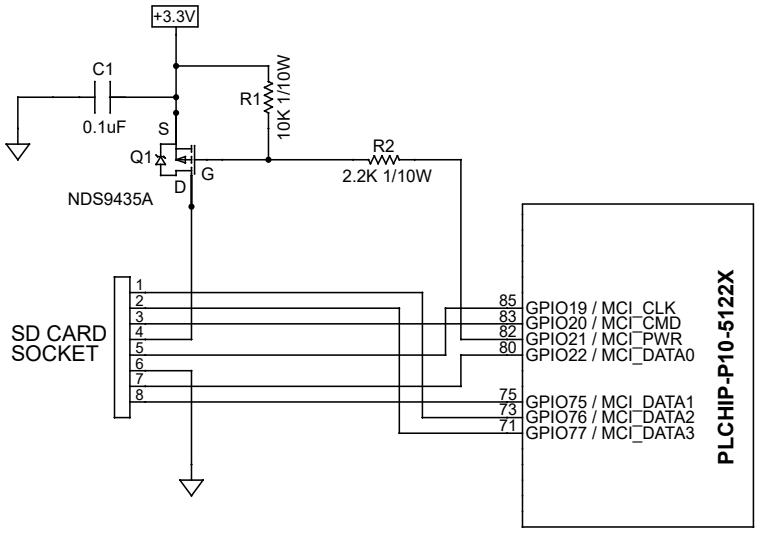


Diagram 6.7B - Example SD Card Interface Circuit

6.8 Timer / Capture Inputs

The P-Series PLC on a Chip™ provides I/O pins that may be configured to be used in timing and frequency measurement. There are two timer modules on the PLCHIP-P10-51220 : TMR_CAP0.X and TMR_CAP1.X. Each of the modules provides three I/O pins; two capture (CAP) pins and one match (MAT) pin. These pins in each module operate together to provide the full counter / timer features supported.
All Timer/Capture pins operate at 3.3V and all circuits that interface to these pins should be limited to 3.3V.

Timer / Capture Module 0
Timer module 0 consists of two capture (input) pins. These are located on pins **57** and **61** as **TMR_CAP0.0** and **TMR_CAP0.1** respectively. In addition to the capture input pins, an output pin is provided on pin **63** as **TMR_MAT0**.

While two capture pins are provided per module, only one pin per module may be used as a counter / timer input capture pin.

The TMR_MAT0 pin operates as a status output. This output is HIGH based on Timer/Capture Channel 0's configuration and when the captured or timed value equals a predetermined set point. The configuration is handled using the EZ LADDER Toolkit. The TMR_MAT0 functionality is currently not supported, but may be added in a future EZ LADDER Toolkit release.

Pin 57 shares functionality and may be used as General Purpose I/O (**GPIO58**).
Pin 61 shares functionality and may be used as General Purpose I/O (**GPIO59**)
Pin 63 shares functionality and may be used as General Purpose I/O (**GPIO60**).

Timer / Capture Module 1
Timer module 1 consists of two capture (input) pins. These are located on pins **46** and **47** as **TMR_CAP1.0** and **TMR_CAP1.1** respectively. In addition to the capture input pins, an output pin is provided on pin **51** as **TMR_MAT1**.

While two capture pins are provided per module, only one pin per module may be used as a counter / timer input capture pin.

The TMR_MAT1 pin operates as a status output. This output is HIGH based on Timer/Capture Channel 1's configuration and when the captured or timed value equals a predetermined set point. The configuration is handled using the EZ LADDER Toolkit. The TMR_MAT1 functionality is currently not supported, but may be added in a future EZ LADDER Toolkit release.

Pin 46 shares functionality and may be used as General Purpose I/O (**GPIO50**).
Pin 47 shares functionality and may be used as General Purpose I/O (**GPIO51**)
Pin 51 shares functionality and may be used as General Purpose I/O (**GPIO54**)

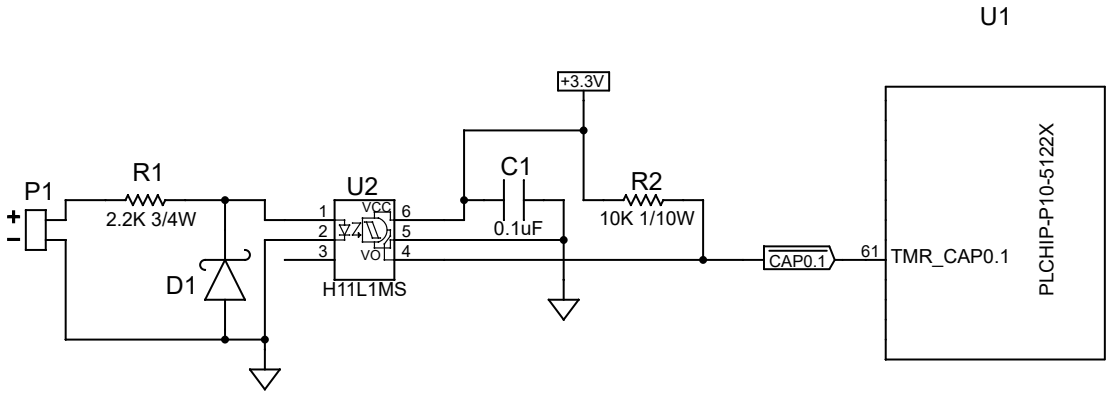


Diagram 6.8A - Example Timer / Capture Input as a Pulse Input

6.9 Retentive Memory / Loss of Power Detection

The PLCHIP-P10-51220 supports retentive memory functionality. Values of variables declared as retentive in EZ LADDER Toolkit are automatically stored into non-volatile memory when loss of power is detected and then automatically read from non-volatile memory and the variables are set to their last stored value when power is restored.

For retentive features to function properly, the ~LOW_VOLT_SENSE pin must be connected to a circuit to monitor the input voltage.

The internal EEPROM or an external FRAM device may be used as the storage device for all retentive features. The amount of retentive memory available and the details to store retentive are dependent upon the device implemented. Contact Divelbiss Corporation or refer to the P-Series EZ LADDER Toolkit for a listing of supported FRAM / I^2C devices. FRAM devices must be connected to either I^2C bus.

An input voltage monitor circuit then causes the P-10 Series PLC on a Chip to go into shut-down when the input voltage reaches a nominal value (signalling loss of power). The ~LOW_VOLT_SENSE pin is active low; therefore, a low signal on this input will cause the PLC on a Chip to go into shut-down and store all retentive variables.

The actual voltage where the hardware should go into shut-down depends upon the power supply capacitance, amount of retentive variables and the operating voltage. On a hardware unit that

will operate from 8-32VDC, a typical detection point would be about 7.5V. Enough power supply capacitance must be designed into the power supply for the 3.3V PLC on a Chip supply (+VDD) to be maintained long enough for all retentive variables to be written into the non-volatile memory.

For the FRAM devices listed above, the write time is approximately 1mS to write 100 bytes of retentive memory. The time between the Loss of Power detection (on the ~LOW_VOLT_SENSE pin) and the actual PLC on a Chip reset (~RESET pin) being active must be at least 1mS per 100 bytes of retentive memory to be written.

When using the internal EEPROM, the write time is longer and will require additional power hold time / capacitance to complete the write, again being dependent upon the number of variables being stored.

The loss of power requires pin **90**, **~LOW_VOLT_SENSE**. This pin should be connected to a circuit that will detect the loss of power early enough to allow retentive writing as described earlier.

The ~LOW_VOLT_SENSE pin may also be used as General Purpose I/O (**GPIO16**). It does not share any additional functionality except GPIO.

Diagram 6.9A is a sample schematic of a loss of power detection circuit.

Diagram 6.15A is a sample schematic of an Ramtron FRAM interfaced to the PLCHIP-P10-51220 as the storage device for retentive memory.

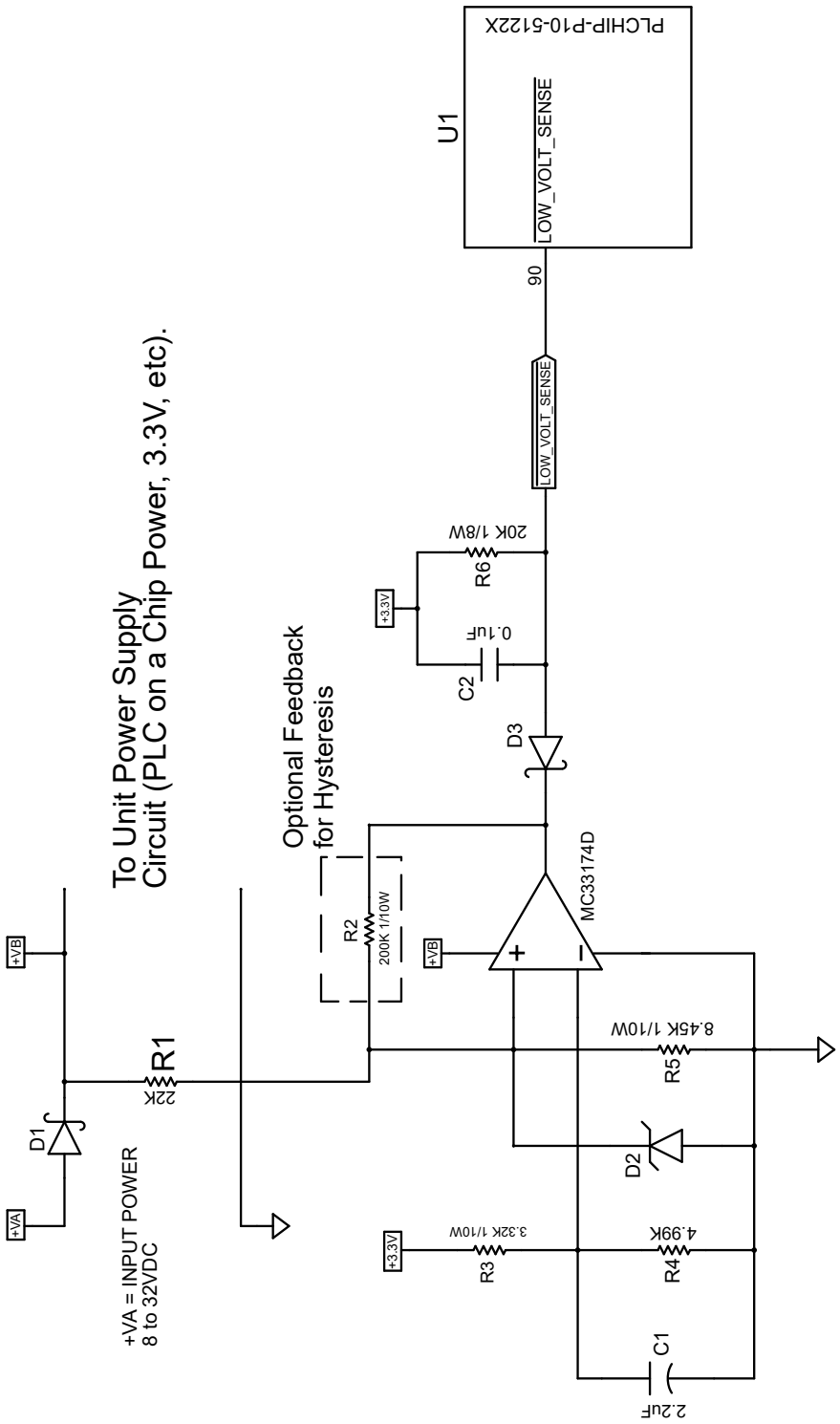


Diagram 6.9A - Example Loss of Power Detection Circuit

6.10 Programming Port

The programming port on the PLCHIP-P10-51220 is used to communicate from the chip to EZ LADDER Toolkit. This connection is used to install the PLC on a Chip kernel, download ladder diagram programs and to monitor the program's ladder execution in EZ LADDER Toolkit.

The programming port is factory set and requires the use of pins **141** and **142** which are **TXD0** and **RXDO** respectively. As the PLC on a Chip operates at a digital 3.3V level, an RS232 transceiver is required for using this port to communicate to a computer with EZ LADDER Toolkit. For communication using the programming port, a connection to digital ground (**VSS**) is required in addition to the transmit and receive pins.

These programming port pins do not share any functionality with other P-10 PLC on a Chip features.

The programming port baud rate is factory controlled and cannot be set in EZ LADDER Toolkit or the PLC on a Chip.

Diagram 6.10A is a sample schematic of an interface circuit for a communication link to a computer operating EZ LADDER Toolkit.

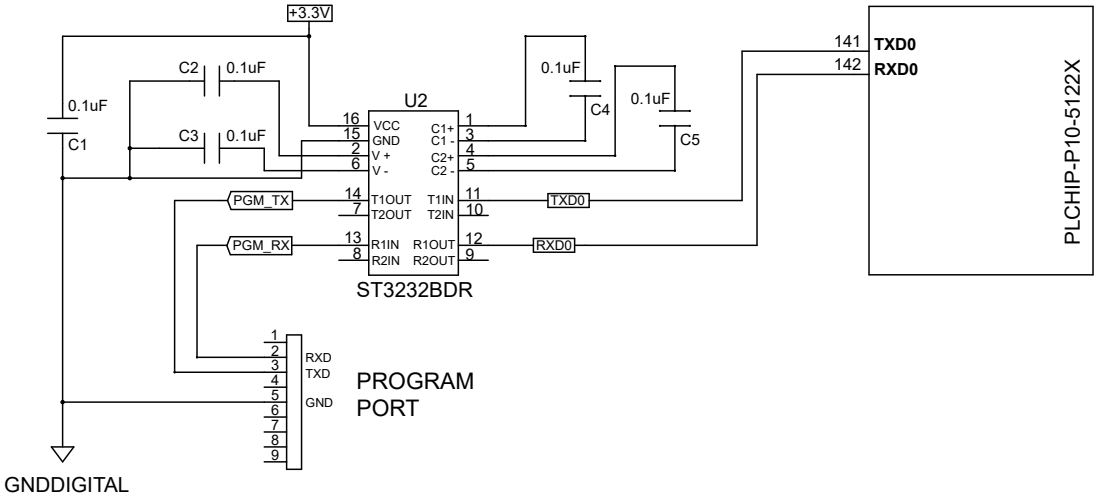


Diagram 6.10A - Example Programming Port Circuit

6.11 Ethernet Port

The PLCHIP-P10-51220 supports Ethernet communication. For ethernet functionality, external interface integrated circuits (Physical Ethernet IC) and components are required. The P-Series PLC on a Chip™ connects and interfaces directly to these exterrnal integrated circuits.

The PLCHIP-P10-51220 supports ethernet as Modbus TCP (Master or Slave). Ethernet functionality is configured in the PLC on a Chip's bootloader and kernel.

The Ethernet port requires the use of pins **136**, **135**, **133**, **132**, **131**, **129**, **128**, **126**, **125** and **123** which are **ETHER_TXD0**, **ETHER_TXD1**, **~ETHER_TXEN**, **ETHER_CRS**, **ETHER_RXD0**, **ETHER_RXD1**, **ETHER_RXER**, **ETHER_REFCLK**, **ETHER_MDC** and **ETHER_MDIO** respectively. Each of these pins is required for the ethernet port to operate correctly.

Additionally, the ~RSTOUT pin (20)should be connected to the ethernet physical chip if it supports the used of an external reset.

The Ethernet pins as with other I/O pins on the PLC on a Chip P-Series operate at a 3.3V level. All interface circuits and components should be 3.3V.

ETHERNET PIN DESCRIPTIONS

ETHER_TXD0
Ethernet Transmit Data 0 Output. Typically connects to TXD0 port on an Ethernet Physical Integrated Circuit.

This Ethernet Port pin shares functionality with General Purpose I/O, GPIO32 .

ETHER_TXD1
Ethernet Transmit Data 1 Output. Typically connects to TXD1 port on an Ethernet Physical Integrated Circuit.

This Ethernet Port pin shares functionality with General Purpose I/O, GPIO33.

ETHER_TXEN
Ethernet Transmit Data Enable. Typically connects to TXEN port on an Ethernet Physical Integrated Circuit.

This Ethernet Port pin shares functionality with General Purpose I/O, GPIO36 .

ETHER_CRS
Ethernet Carrier Sense Input. Typically connects to CRS port on an Ethernet Physical Integrated Circuit.

This Ethernet Port pin shares functionality with General Purpose I/O, GPIO40.

ETHER_RXD0
Ethernet Recieve Data 0 Input. Typically connects to RXD0 port on an Ethernet Physical Integrated Circuit.

This Ethernet Port pin shares functionality with General Purpose I/O, GPIO41.

ETHER_RXD1
Ethernet Recieve Data 1 Input. Typically connects to RXD1 port on an Ethernet Physical Integrated Circuit.

This Ethernet Port pin shares functionality with General Purpose I/O, GPIO42 .

ETHER_RXER
Ethernet Receive Error input. Typically connects to RXER port on an Ethernet Physical Integrated Circuit.

This Ethernet Port pin shares functionality with General Purpose I/O, GPIO46.

ETHER_REFCLK
Ethernet Reference Clock. Typically connects to X1 port on an Ethernet Physical Integrated Circuit.

This Ethernet Port pin shares functionality with General Purpose I/O, **GPIO47**.

ETHER_MDC
Ethernet MDIO/MIIM Clock output. Typically connects to MDC port on an Ethernet Physical Integrated Circuit.

This Ethernet Port pin shares functionality with General Purpose I/O, **GPIO48**.

ETHER_MDIO
Ethernet MDIO input/output. Used as Ethernet MIIm data input and output. Typically connects to MDIO port on an Ethernet Physical Integrated Circuit.

This Ethernet Port pin shares functionality with General Purpose I/O, **GPIO49**.

Diagram 6.11A is a sample schematic of an interface circuit for an ethernet communication port (1 port with physical).

Refer to Diagram 6.3B for a sample layout of the P-10 Chip, power pins, oscillator and Ethernet.

Multiple Ethernet Ports

The PLCHIP-P10-51220 supports the implementation of an Ethernet Physical with built-in switch. Currently there are two supported part numbers, but contact Divelbiss Corporation for any updates to the supported Ethernet devices.

The supported devices are:

Mfg: Microchip P/N: KSZ8775CLXIC
5 Port Ethernet Switch with Physical (80LQFP)

Mfg: Microchip P/N: KSZ8873RLLI
3 Port Ethernet Switch with Physical (64LQFP)

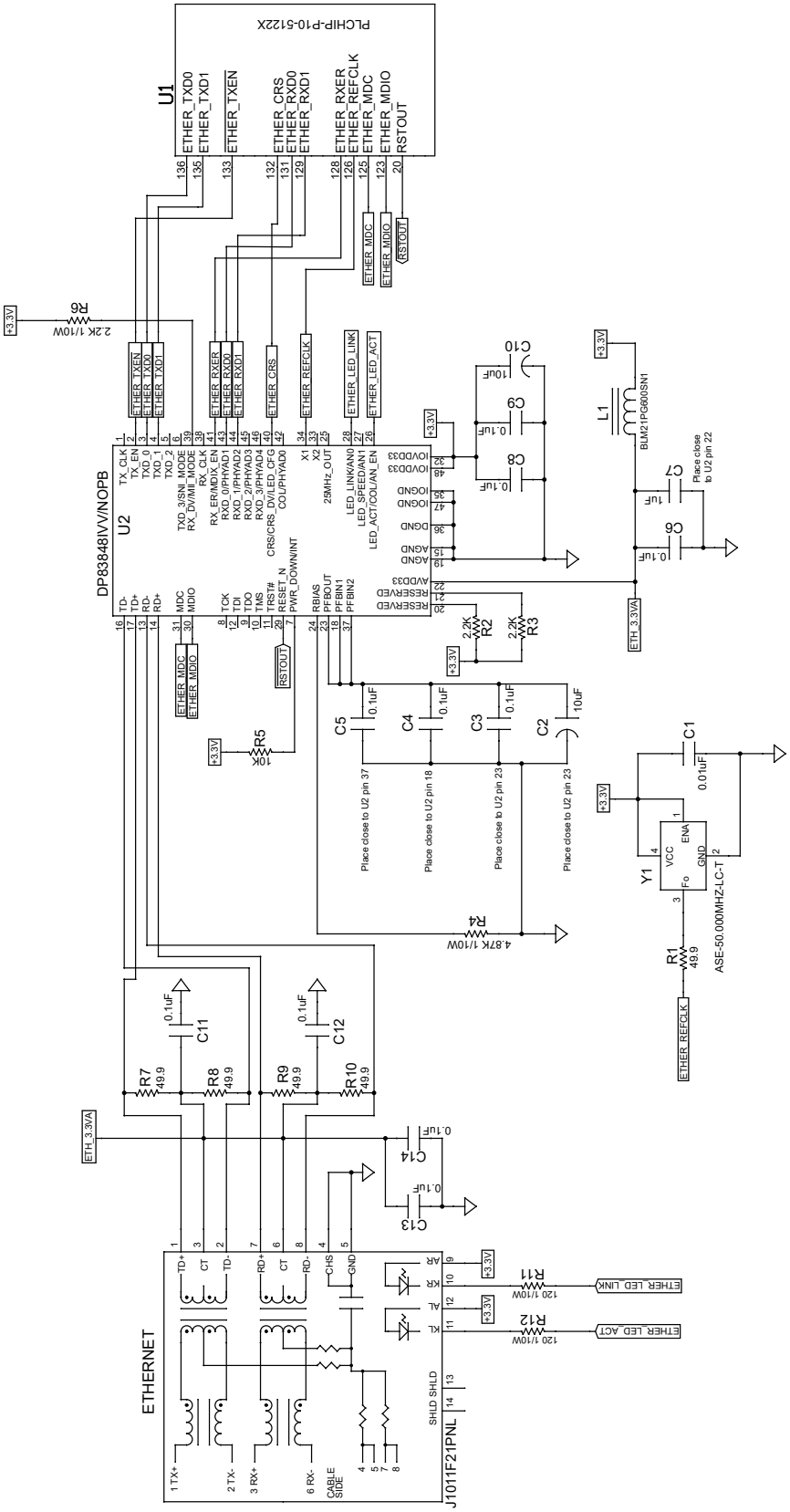


Diagram 6.11A - Example Ethernet Port Circuit

6.12 Controller Area Network (CAN) Ports

The PLCHIP-P10-51220 supports up to two Controller Area Network (CAN) Ports. These ports allow communication to other devices that support SAE-J1939 or Divelbiss OptiCAN.

CAN Port 0

CAN Port 0 requires the use of pins 66 and 67 which are CAN_RX0 and CAN_TX0 respectively. As the PLC on a Chip operates at a digital 3.3V level, a CAN transceiver is required interface these pin of the PLC on a Chip to the external CAN network.

The PLC on a Chip pins for CAN Port 0 share functionality with these other P-10 PLC on a Chip features: Pin 66 (I2C_SDA1, GPIO0), Pin 67 (I2C_SCL1, GPIO1).

CAN Port 1

CAN Port 1 requires the use of pins 116 and 115 which are CAN_RX1 and CAN_TX1 respectively. As the PLC on a Chip operates at a digital 3.3V level, a CAN transceiver is required interface these pin of the PLC on a Chip to the external CAN network.

The PLC on a Chip pins for CAN Port 1 share functionality with these other P-10 PLC on a Chip features: Pin 116 (GPIO4), Pin 115 (GPIO5).

To use the PLCHIP-P10-51220 as a device on a J1939 or OptiCAN network, all rules governing the network must be adhere to including the use of terminating resistors, cable size, type and length.

Figure 6.12A is a typical interface circuit for OptiCAN. A configurable terminating resistor is shown.

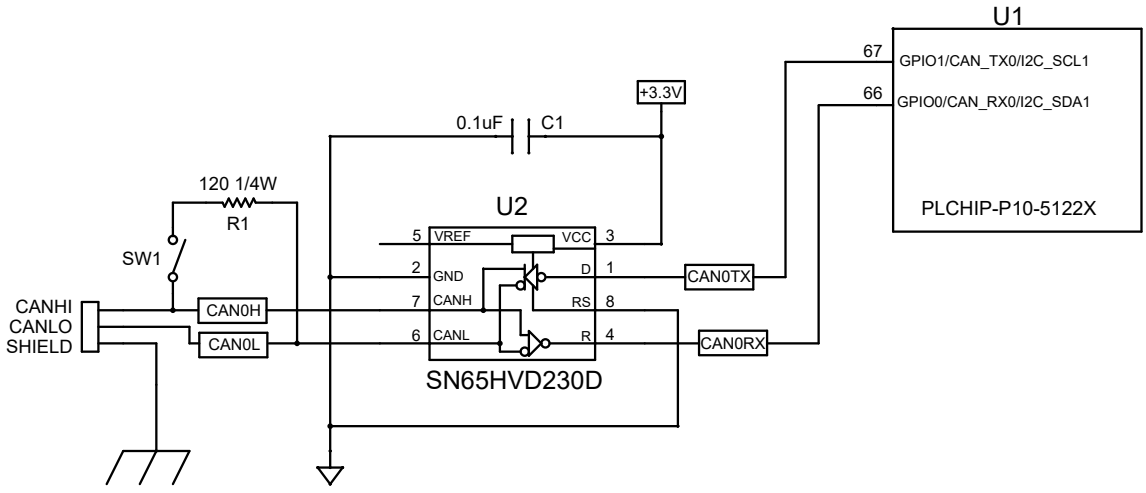


Diagram 6.12A - Example CAN Port Interface Circuit

6.13 Serial (UART) Ports

The PLCHIP-P10-51220 supports up to four TTL Serial Ports via on-board UARTs. One UART supports full hardware handshaking while the other three support transmit and receive only. These

UART ports are 3.3V TTL level; therefore they require additional interface circuitry to communicate with other device external to the PLC on a Chip.

The PLC on a Chip UARTs support Modbus Master and Modbus Slave. The maximum baud rate for all UARTs is 115,200 baud (115K).

Figure 6.13A is a typical RS232 Interface circuit.
Figure 6.13B is a typical RS422 Interface circuit.
Figure 6.13C is a typical RS485 Interface circuit.

UART 1

UART 1 supports full hardware handshaking on pins **107**, **106**, **105**, **100**, **99**, **97**, **96**, **95** as **TXD1**, **RXD1**, **CTS1**, **DCD1**, **DSR1**, **DTR1**, **RI1**, **RTS1** respectively. With full handshaking support, UART 1 is ideal for interfacing to items such as modems, radios, etc. When interfacing to these types of devices, refer to their documentation for connection requirements.

The PLC on a Chip pins for UART 1 share functionality with these other P-10 PLC on a Chip features: Pin 107 (**GPIO64**), Pin 106 (**GPIO65**), Pin 105 (**GPIO66**), Pin 100 (**GPIO67**), Pin 99 (**GPIO68**), Pin 97 (**GPIO69**), Pin 96 (**GPIO70**), Pin 95 (**GPIO71**).

UART 2

UART 2 supports transmit and receive only. These connections are on pins **93** and **92**, which are **TXD2** and **RXD2** respectively.

The PLC on a Chip pins for UART 2 share functionality with these other P-10 PLC on a Chip features: Pin 93 (**GPIO72**), Pin 92 (**GPIO73**).

UART 3

UART 3 supports transmit and receive only. These connections are on pins **118** and **122**, which are **TXD3** and **RXD3** respectively.

The PLC on a Chip pins for UART 3 share functionality with these other P-10 PLC on a Chip features: Pin 118 (**GPIO156**), Pin 122 (**GPIO157**).

UART 4

UART 4 supports transmit and receive only. These connections are on pins **143** and **98**, which are **TXD4** and **RXD4** respectively.

The PLC on a Chip pins for UART 4 share functionality with these other P-10 PLC on a Chip features: Pin 143 (**GPIO164**), Pin 98 (**GPIO163**).

Pin 98 (RXD4) is open-drain. A pull-up resistor is required if the pin is being used as GPIO.

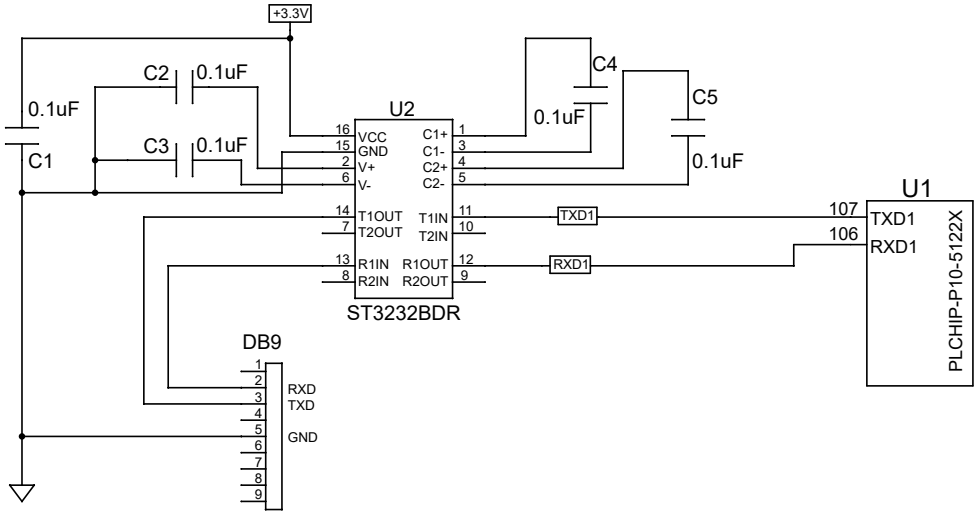


Diagram 6.13A - Example RS232 Interface Circuit

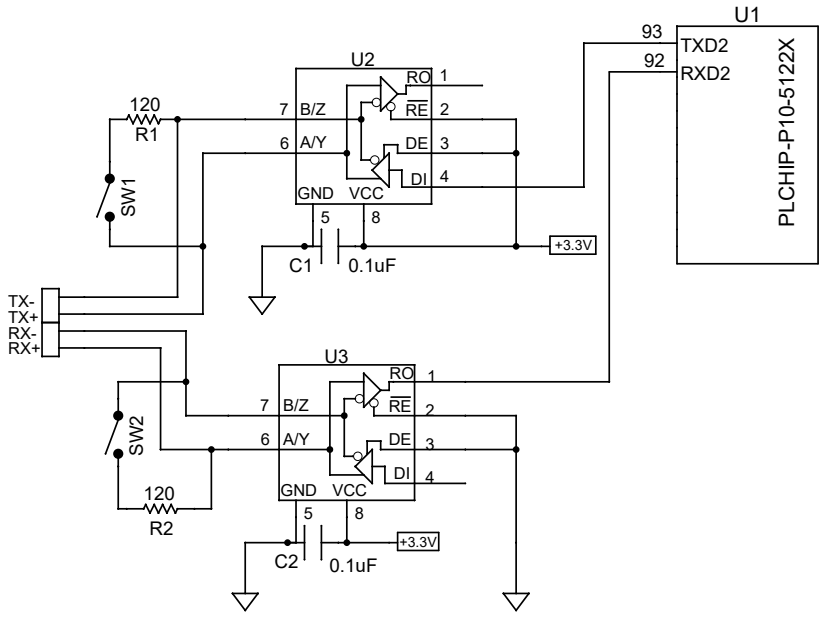


Diagram 6.13B - Example RS422 Interface Circuit

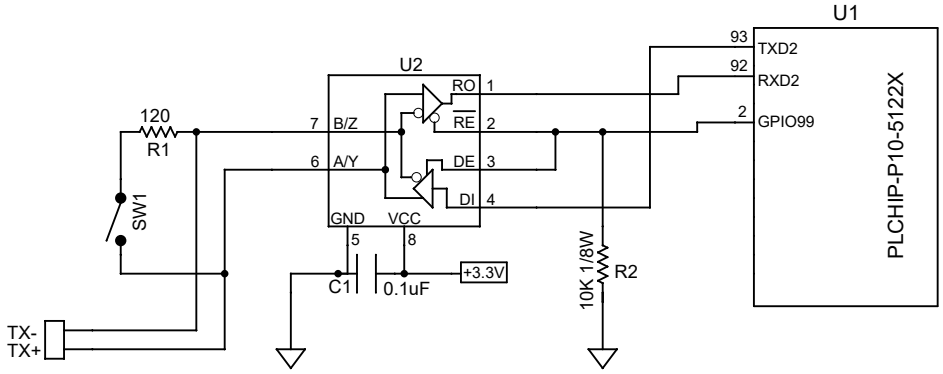


Diagram 6.13C - Example RS485 Interface Circuit

6.14 SPI Ports

The PLCHIP-P10-51220 supports up to two SPI (Serial Peripheral Interface) Ports. These SPI ports may be used to interface to a multitude of SPI devices, extending the PLC on a Chip's versatility. SPI devices must be supported in EZ LADDER Toolkit or you must write your own interface using the EZ LADDER structured text editor. As supported devices may change periodically, refer to the P-Series EZ LADDER Toolkit Manual for a list of supported devices.

Diagram 6.14A represents a sample SPI Port connection to an SPI device.

SPI Port 0

SPI port 0 consists of three individual pins that work together to allow complete functionality of the SPI bus. SPI port 0 is located on pins 89, 87 and 86 which are SPI_SCK0, SPI_MISO0 and SPI_MOSI0 respectively. Additionally, for each SPI device on the bus (port), a select line must be used. Any GPIO pin may be used as the select line for an SPI device.

SPI_SCK0
Serial Clock Output for SPI Port 0.
Pin 89 shares functionality and may be used as General Purpose I/O (GPIO15).

SPI_MISO0
Master In - Slave Out Input for SPI Port 0
Pin 87 shares functionality and may be used as General Purpose I/O (GPIO17).

SPI_MOSI0
Master Out - Slave In Output for SPI Port 0
Pin 86 shares functionality and may be used as General Purpose I/O (GPIO18).

SPI Port 1

SPI port 1 consists of three individual pins that work together to allow complete functionality of the SPI bus. SPI port 1 is located on pins 112, 111 and 109 which are SPI_SCK1, SPI_MISO1 and SPI_MOSI1 respectively. Additionally, for each SPI device on the bus (port), a select line must be used. Any GPIO pin may be used as the select line for an SPI device.

SPI_SCK1
Serial Clock Output for SPI Port 1.
Pin 112 shares functionality and may be used as General Purpose I/O (GPIO7).

SPI_MISO1
Master In - Slave Out Input for SPI Port 1
Pin 111 shares functionality and may be used as General Purpose I/O (GPIO8).

SPI_MOSI1
Master Out - Slave In Output for SPI Port 1
Pin 109 shares functionality and may be used as General Purpose I/O (GPIO9).

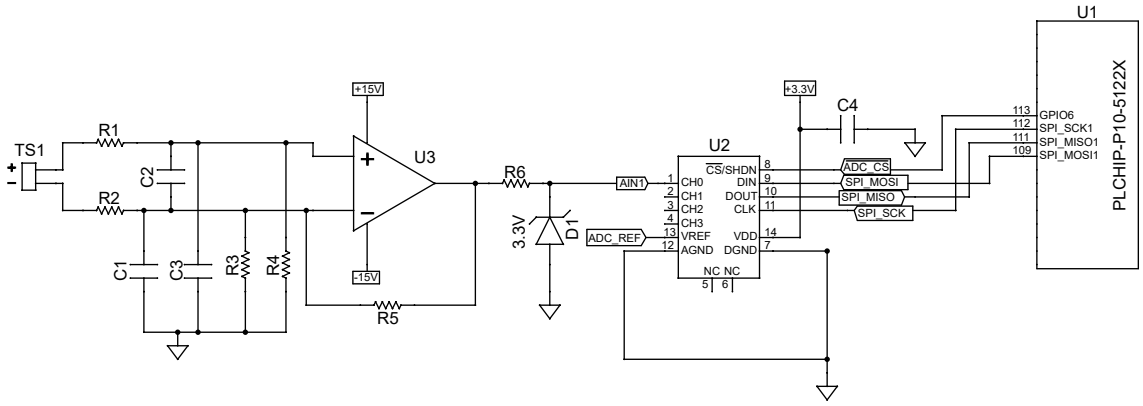


Diagram 6.14A - Example SPI Port Circuit

6.15 I²C Ports

The PLCHIP-P10-51220 supports up to three 1Mbit I²C Ports. These ports support standard I²C devices (up to 1Mbit) using Data and Clock lines. I²C port lines require an external pull-up resistor of 1.5KΩ for proper operation.

While the P-Series PLC on a Chip™ provides hardware support for I2C devices, only supported devices will be functional and available in EZ LADDER Toolkit. As supported devices may change periodically, refer to the P-Series EZ LADDER Toolkit Manual for a list of supported devices.

I²C Port 0

Port 0 requires the use of pins **35** and **34** which are **I2C_SDA0** and **I2C_SCL0** respectively. As the PLC on a Chip operates at a digital 3.3V level, a all I²C devices connected to this port should be 3.3V compliant.

The PLC on a Chip pins for I²C Port 0 share functionality with these other P-10 PLC on a Chip features: Pin 35 (**GPIO27**), Pin 34 (**GPIO28**).

I2C Port Pins 48 and 50 are open-drain. A pull-up resistor is required if the pin(s) are being used as GPIO.

Figure 6.15A is a example circuit schematic for an I²C FRAM retentive memory storage.

I²C Port 1

Port 1 requires the use of pins **66** and **67** which are **I2C_SDA1** and **I2C_SCL1** respectively. As the PLC on a Chip operates at a digital 3.3V level, a all I²C devices connected to this port should be 3.3V compliant.

The PLC on a Chip pins for I²C Port 1 share functionality with these other P-10 PLC on a Chip features: Pin 66 (**GPIO0**, **CAN_RX0**), Pin 67 (**GPIO1**, **CAN_TX0**).

I²C Port 2

Port 2 requires the use of pins **69** and **70** which are **I2C_SDA2** and **I2C_SCL2** respectively. As the PLC on a Chip operates at a digital 3.3V level, a all I²C devices connected to this port should be 3.3V compliant.

The PLC on a Chip pins for I²C Port 2 share functionality with these other P-10 PLC on a Chip features: Pin 69 (GPIO10), Pin 70 (GPIO11).

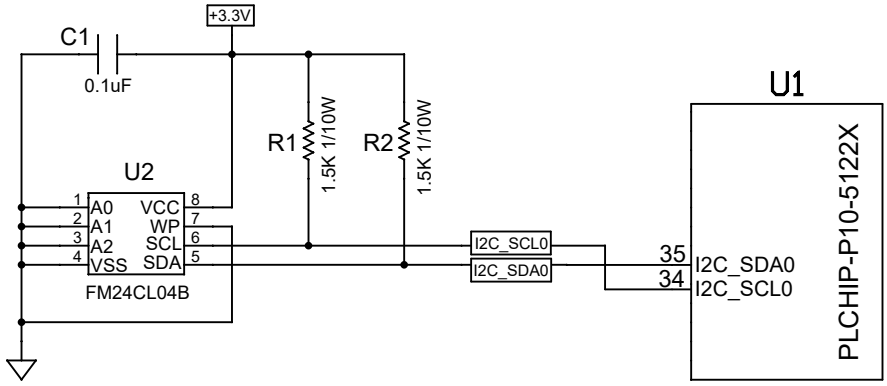


Diagram 6.15A - Example I²C FRAM storage device for Retentive Memory

6.16 Quadrature Encoder Interface

The PLCHIP-P10-51220 supports a three (3) channel quadrature input (Channel A, Channel B and Index). As with all other I/O pins, the quadrature input requires 3.3VDC input signals for proper opreration. The Quadrature Encoder Interface supports X1, X4 and Up/Down plus additional features based on software configuration. Refer to the P-Series EZ LADDER Toolkit Manual for details of supported features.

The Quadrature Encoder Interface requires the use of pins 49, 53 and 54 which are QEI_PHA, QEI_PHB and QEI_IDX respectively. Each of these pins is required for the interface port to operate correctly. Diagram 6.16A represents a sample circuit and connection to the Quadrature Encoder Interface.

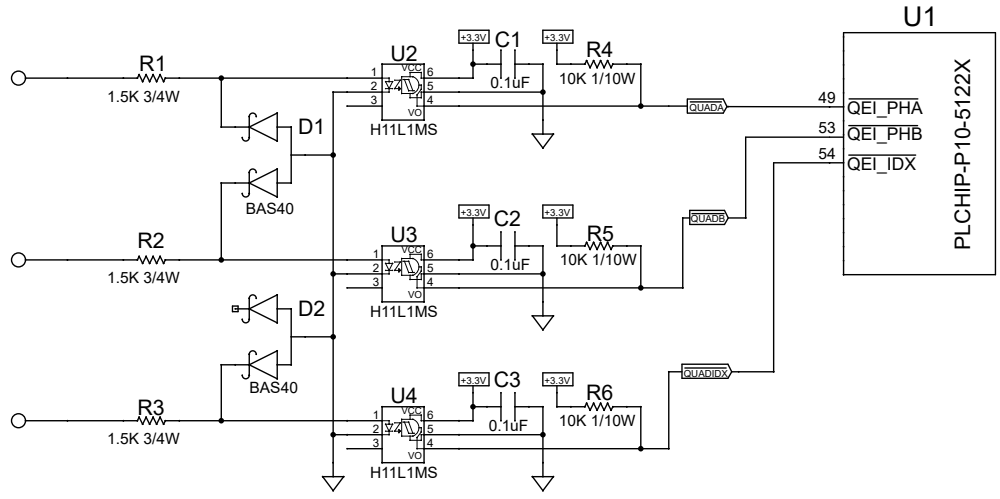


Diagram 6.16A - Example Quadrature Encoder Interface Circuit

The PLC on a Chip pins for the Quadrature Encoder Interface share functionality with these other P-10 PLC on a Chip features: Pin 49 (GPIO52), Pin 53 (GPIO55), Pin 54 (GPIO56).

6.17 Liquid Crystal Display (LCD) Interface

The PLCHIP-P10-51220 supports an LCD (Liquid Crystal Display) Interface. This LCD Interface supports the industry standard HD44780 Controller Emulation. LCD displays connected to this interface must support the HD44780 standard.

The LCD Interface supports displays from 1-4 Rows and from 8 to 42 colums.

The LCD Interface requires the use of pins 52, 55, 58, 68, 72, 74, 78, 84, 88, 91 and 94 which are LCD_D0, LCD_D1, LCD_D2, LCD_D3, LCD_D4, LCD_D5, LCD_D6, LCD_D7, LCD_RS, LCD_RW and LCD_E respectively. Each of these pins is required for the interface port to operate correctly. Diagram 6.18A represents a sample circuit and connection to the LCD Interface.

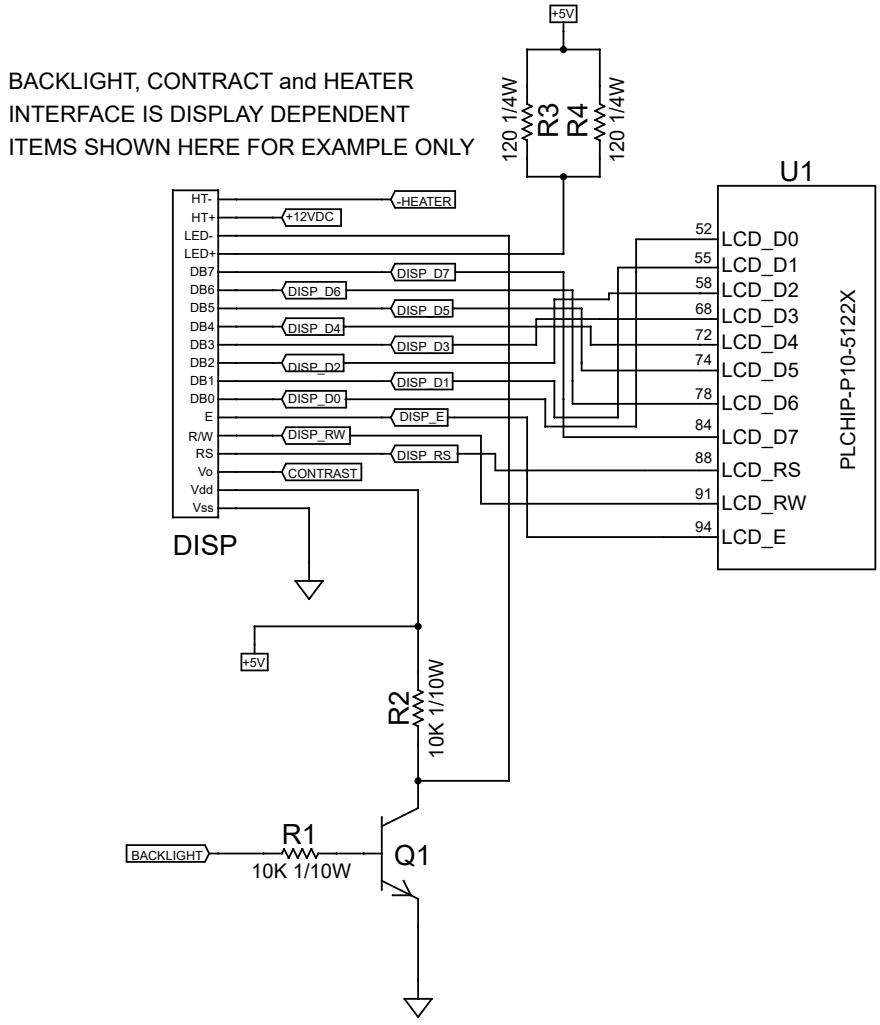


Diagram 6.17A - Example LCD Display Interface Circuit

The PLC on a Chip pins for the LCD Interface share functionality with these other P-10 PLC on a Chip features: Pin 52 (GPIO128), Pin 55 (GPIO129), Pin 58 (GPIO130), Pin 68 (GPIO131), Pin 72 (GPIO132), Pin 74 (GPIO133), Pin 78 (GPIO134), Pin 84 (GPIO135), Pin 88 (GPIO136), Pin 91 (GPIO137), Pin 94 (GPIO138).

6.18 Keypad Interface

The PLCHIP-P10-51220 supports a 4 row by 5 column keypad matrix. The PLC on a Chip™ scans the keypad matrix, detecting keys that are pressed.

The Keypad Interface requires the use of pins 101, 104, 108, 110, 120, 127, 124, 130,and 134 which are KEYPAD_COL1, KEYPAD_COL2, KEYPAD_COL3, KEYPAD_COL4, KEYPAD_COL5, KEYPAD_ROW1, KEYPAD_ROW2, KEYPAD_ROW3 and KEYPAD_ROW4 respectively. Each of these pins is required for the interface port to operate correctly.

Diagram 6.18A represents the standard 4x5 matrix keypad circuit.

The PLC on a Chip pins for the Keypad Interface share functionality with these other P-10 PLC on a Chip features: Pin 101 (GPIO139), Pin 104 (GPIO140), Pin 108 (GPIO141), Pin 110 (GPIO142), Pin 120 (GPIO143), Pin 127 (GPIO152), Pin 124 (GPIO153), Pin 130 (GPIO158) and Pin 134 (GPIO159).

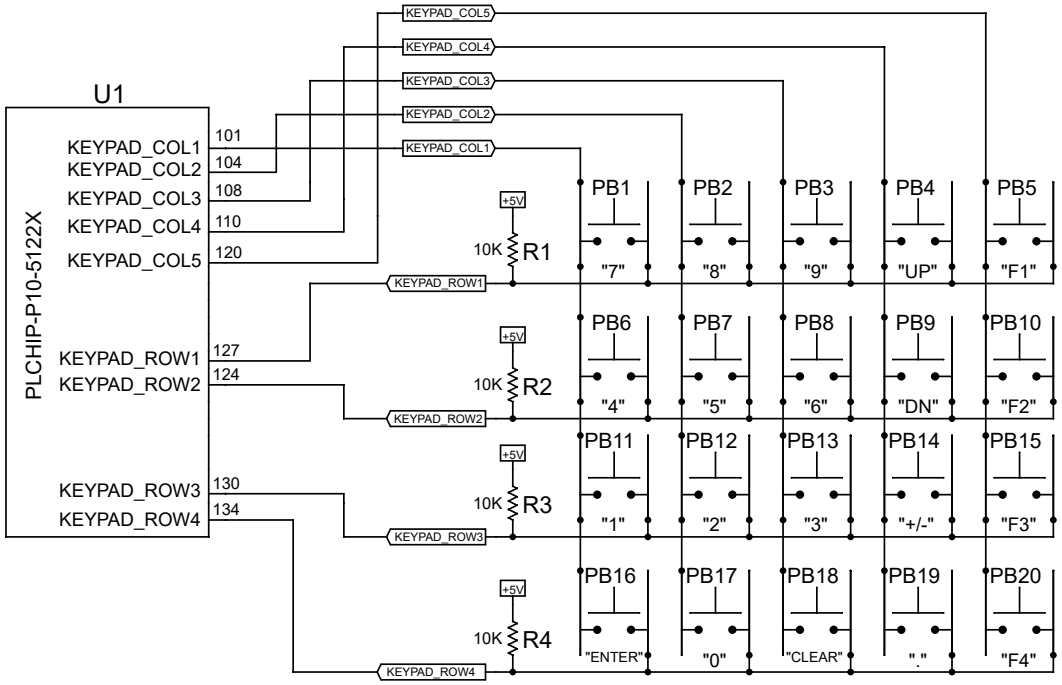


Diagram 6.18A - Example Keypad Interface Circuit

6.19 Graphics LCD Display Interface

The PLCHIP-P10-51220 supports specific LCD graphics displays. These LCD graphics displays provide the ability for PLC on a Chip products to display graphics, multiple sized text and variables.

The following graphics displays are supported:

1. Crystal Fontz part number: CFAG12864A-xxxx
2. New Haven part number: NHD-12864AZ-xxxx
   xxxx are optional items in the part number for specifying features.

The LCD graphics display uses the same PLC on a Chip pins as the standard (non-graphics) LCD display with a requirement for three additional **GPIO** pins for RESET, CS1 and CS2.

The LCD Interface requires the use of pins **52**, **55**, **58**, **68**, **72**, **74**, **78**, **84**, **88**, **91** and **94** which are **LCD_D0**, **LCD_D1**, **LCD_D2**, **LCD_D3**, **LCD_D4**, **LCD_D5**, **LCD_D6**, **LCD_D7**, **LCD_RS**, **LCD_RW** and **LCD_E** respectively. Each of these pins is required for the interface port to operate correctly. Diagram 6.19A represents a sample circuit and connection to the the graphics LCD Interface.

The graphics display requires RESET, CS1 and CS2 pins be connected to any available GPIO pins on the PLC on a Chip. Refer to Table 1, Table 2 and Section 6.4 for possible General Purpose I/O (GPIO).

The PLC on a Chip logic operates at 3.3VDC and the graphics display operates at 5VDC. For the graphics disiplay to see a logic high from the PLC on a Chip, the graphics display interface circuit requires logic level translators (in this example, MC74HCT245N).

Diagram 6.19A represents the graphics LCD display interface circuit.

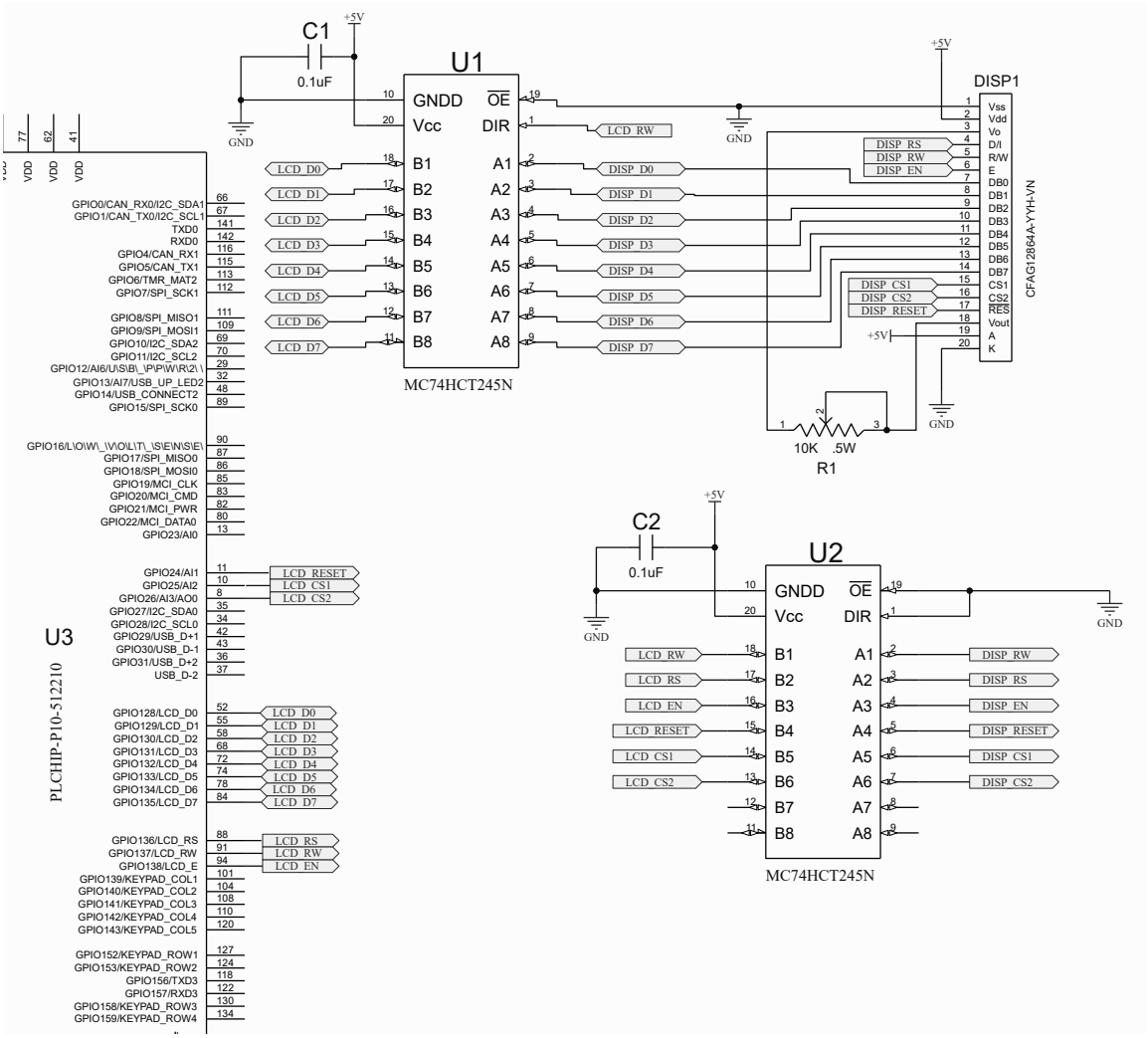


Diagram 6.19A - Example Graphics LCD Display Interface Circuit

6.20 Real Time Clock Circuit

The PLCHIP-P10-51220 supports an internal real time clock. This real time clock must have external circuitry to function. The external circuit is comprised of two capacitors, a battery and a crystal. The crystal should be 32.768KHz and the capacitors should be 22pF. The battery should be a 3V battery with a sufficient mAH rating to support the application.

The real time clock requires the use of pins **23**, **25** and **27** which are **RTCX1**, **RTCX2** and **VBAT** respectively. Each of these pins is required for the real time clock to operate correctly.

Diagram 6.20A represents the required real time clock circuit.

The PLC on a Chip pins for the for the Real Time clock do not share functionality with any other pins or features.

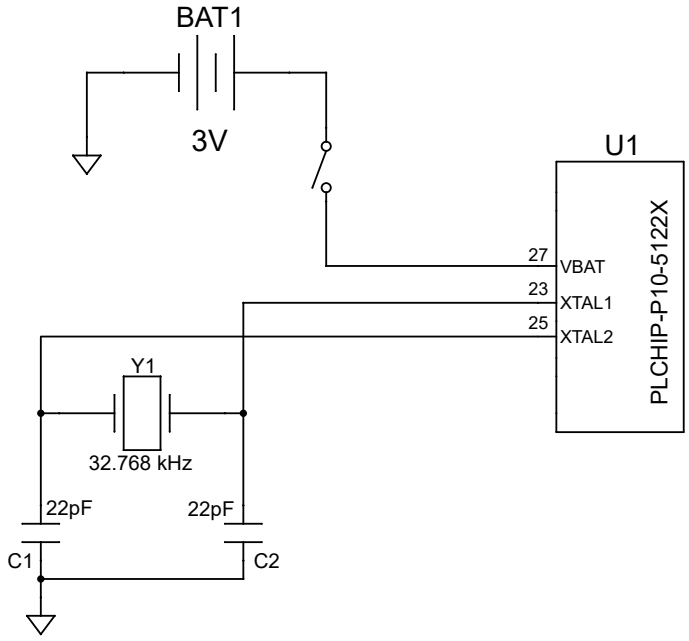


Diagram 6.20A - Example Real Time Clock Circuit

6.21 Watchdog LED Circuit

The PLCHIP-P10-51220 supports an LED indicator for status of the PLC on a Chip. The LED is connected to the **LED_KERNEL** pin (pin **76**). This pin must be pulled high for proper PLC on a Chip operation.

Diagram 6.21A represents a recommended Watchdog LED Circuit.

The PLC on a Chip pin for the for the LED KERNEL does not share functionality with any other pins or features.

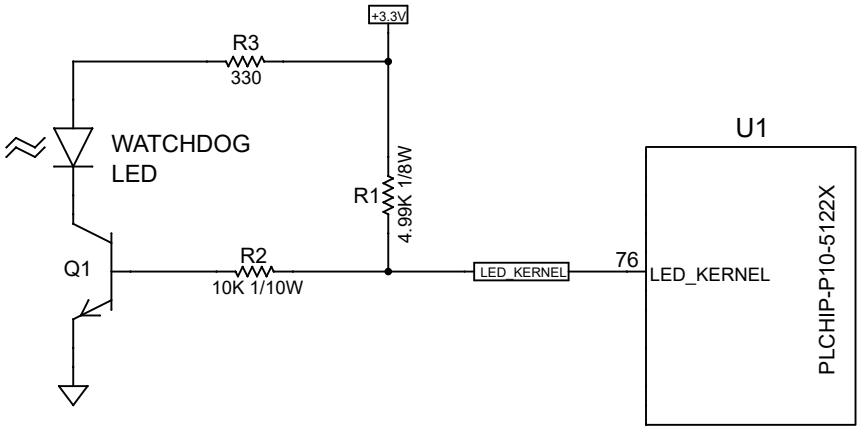


Diagram 6.21A - Example Watchdog / Kernel LED Circuit

7. Electrical Characteristics

TABLE 3 - Power Pins					
Pin #	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
14	VDD_AN	2.7	3.3	3.6	V
17	VREF_AN	2.7	3.3	VDD_AN	V
18	VDD1	2.4	3.3	3.6	V
27	VBAT	2.1	3.3	3.6	V
41	VDD2	2.4	3.3	3.6	V
60	VDD3	2.4	3.3	3.6	V
62	VDD4	2.4	3.3	3.6	V
77	VDD5	2.4	3.3	3.6	V
102	VDD6	2.4	3.3	3.6	V
114	VDD7	2.4	3.3	3.6	V
121	VDD8	2.4	3.3	3.6	V
138	VDD9	2.4	3.3	3.6	V

TABLE 4 - General Purpose I/O Pins (GPIO) as Digital Inputs					
Symbol	**Paramter**	**Min**	**Typ**	**Max**	**Unit**
V_I	Input Voltage	0	---	5.0*	V
V_{IH}	High Level Input Voltage	0.7 x VDD	---	---	V
V_{IL}	Low Level Input Voltage	---	---	0.3 x VDD	V

* GPIO input pins are designed to operate at 3.3V but are 5V tolerant.

TABLE 5 - General Purpose I/O Pins (GPIO) as Digital Outputs						
Symbol	**Paramter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
V_I	Output Voltage	---	0	---	VDD	V
V_{IH}	High Level Input Voltage	I_{OH}= -4mA	VDD - 0.4	---	---	V
V_{IL}	Low Level Input Voltage	I_{OL}= 4mA	---	---	0.4	V

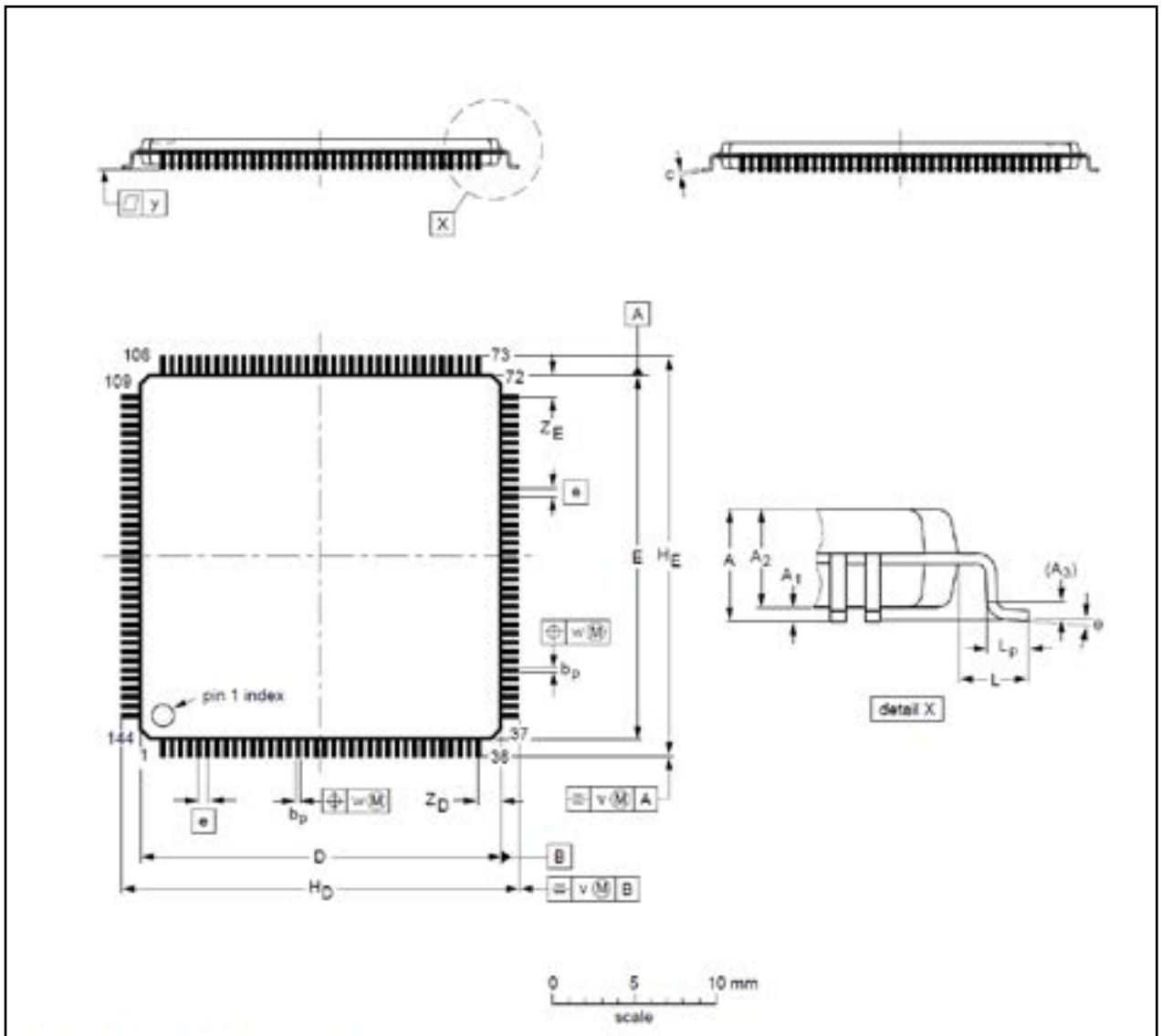
TABLE 6 - I^2C Bus Pins						
Symbol	**Paramter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
V_{IH}	High Level Input Voltage		0.7 x VDD	---	---	V
V_{IL}	Low Level Input Voltage		---	---	0.3 x VDD	V
V_{hys}	Hysteresis Voltage		---	0.05 x VDD	---	V
V_{OL}	Low Level Output Voltage		---	---	.4	V

8. Thermal Characteristics

The maximum junction temperature the the PLC on Chip™ , PLCHIP-P10-51220 is 125 ˚C with ambient from -40 ˚C to +85 ˚C.

9. Package & Soldering Details

PLCHIP-P10-51220 Packaging / Mechanical Dimensions



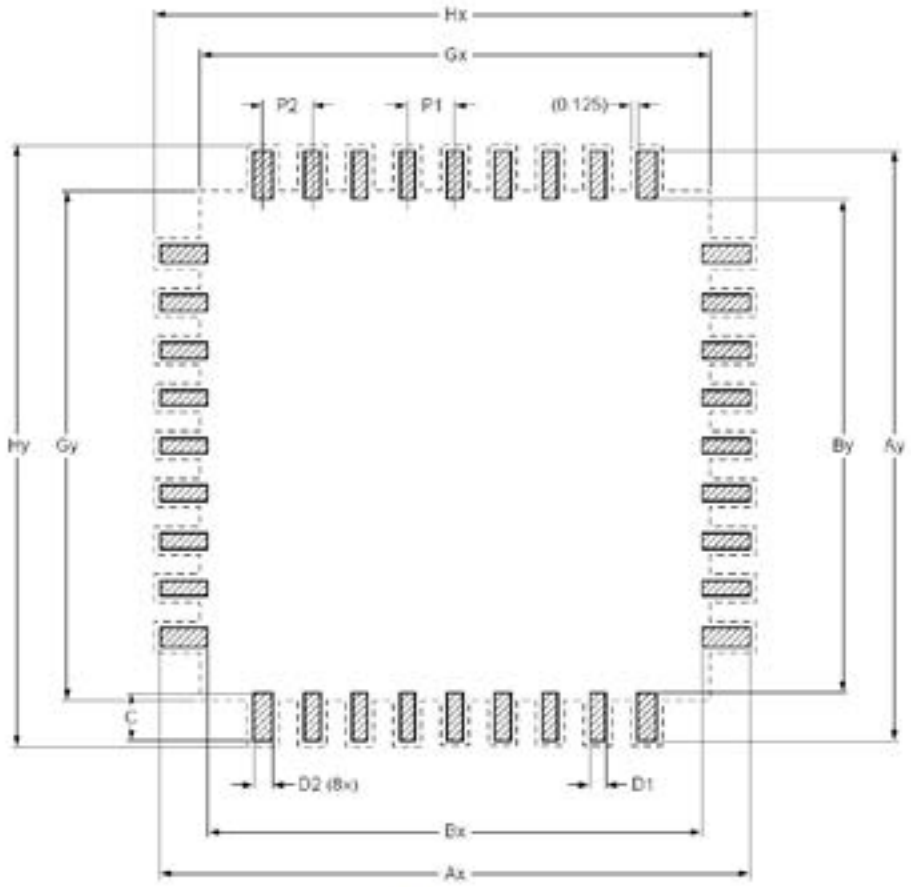
DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	20.1 19.9	20.1 19.9	0.5	22.15 21.85	22.15 21.85	1	0.75 0.45	0.2	0.08	0.08	1.4 1.1	1.4 1.1	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

PLCHIP-P10-51220 Footprint Information for Reflow Soldering



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	23.300	23.300	20.300	20.300	1.500	0.280	0.400	20.500	20.500	23.550	23.550

sot485-1_fr

10. Software Information

While this datasheet has been devoted to the hardware design of the PLC on a Chip Integrated Circuit, the chip itself does require software to operate.

10.1 EZ LADDER Tookit

EZ LADDER Toolkit is the only programming platform for PLC on a Chip targets (controllers, modules and integrated circuits). EZ LADDER provides the platform for installing the necessary target kernels to each target, developing ladder diagrams and the tools to download and debug the ladder diagram programs. Refer to the P-Series EZ LADDER Toolkit Manual for details on using EZ LADDER with P-Series PLC on a Chip targets.

10.2 Target Kernel

The first primary software needed is the PLC on a Chip Module's kernel. This software is loaded on the PLC on a Chip Module using the Bootloader feature in EZ LADDER Toolkit. This software essentially becomes the Module's operating system allowing ladder diagrams to be downloaded and ran on the PLC on a Chip Module (also identified as the target).

All PLC on a Chip targets (controllers, modules and chips) ship from the factory without a kernel installed for greater versatility for customers. It is the customer's responsibility to install the correct kernel (and version they require) on each PLC on a Chip Module (target). As new features are added, some customers may wish to 'freeze' their versions while others do not. With each customer installing the kernel for each target, they have the option of loading the latest kernel and taking advantage of new features or installing a previous kernel version.

All kernel files are automatically installed when EZ LADDER Toolkit is installed and by default are loaded in a subdirectory under where EZ LADDER Toolkit is installed named **Kernel**.

All kernel files have the .dat file extension. **The file named PLCHIP-P10-5122X.dat is the correct file for the PLC on a Chip (PLCHIP-P10-51220)**. This file and only this file should be installed on the hardware target. Refer to the P-Series EZ LADDER Toolkit Manual for details on installing kernels.

11. Revision History

03/17/2020	**Revision 1**	**Initial Datasheet Release.**
04/22/2020	**Revision 2**	**Corrected Typographical Errors**
6/17/2020	**Revision 3**	**Updated ordering information (part numbers and ship quantities).**
1/27/2021	**Revision 4**	**Added Graphics LCD Display Informaton**

PLCHIP-P10-51220 Pb-free Profile Feature and Specification

Profile Feature	Pb-Free Assembly
Average Ramp-Up Rate	3°C / second max
Preheat Temperature Minimum	150°C
Preheat Temperature Maximum	200°C
Preheat Temperature Time	60-180 seconds
Temperature - Time maintained above	217°C
Time maintained above Temperature	60-150 seconds
Peak / Classification Temperature	260°C
Time within 5°C of actual Peak Temperature	20-40 seconds
Ramp-Down Rate	6°C / second maximum
Time 25°C to Peak Temperature	8 minutes maximum

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