

Customer Advisory

ADV2407

Quartus[®] Prime Pro Edition Software Update for Agilex[™] 7 Device

Description

Altera is notifying customers of important software updates related to the Quartus[®] Prime Pro Edition Software for Agilex[™] 7 Devices F-Series and I-Series. Refer to Table 1 for the change details.

Table 1

Update Details	KDB Article Link
In the Quartus Prime Pro Edition Software version 23.2 and later, you might see a functional failure when writing to an M20K RAM after Partial Reconfiguration. This problem only affects designs using an Agilex 7 device F-Series or I-Series with either of the conditions below:	
The Compiler Optimization Mode is not set to Performance .	Why do writes to an M20K fail after a Partial Reconfiguration?
• The design has 2 or more abutting Partial Reconfiguration partitions that share the same clock.	
The issue is resolved in the Quartus Prime Pro Edition Software version 24.1 onwards.	

Recommended Actions

Customers are requested to review the changes and determine the impact on their designs. See the KDB article link above for details.

For questions or support, please contact your local Sales representative, or submit a question or request at the My Intel support page, log in via: https://www.intel.com/content/www/us/en/my-intel/fpga-sign-in.html

Products Affected

Agilex 7 FPGAs and SoC FPGAs F-Series Agilex 7 FPGAs and SoC FPGAs I-Series

The list of affected part numbers (OPNs) can be downloaded in Excel form: https://cdrdv2.intel.com/v1/dl/getContent/822715



Contact

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Customer Notifications Subscription

If you want to receive customer notifications by email, please follow the instructions in ADV 2209.

Altera references J-STD-046 guidelines for PCN.

In accordance with J-STD-046, this change is deemed acceptable to the customer if no acknowledgment is received within 30 days from the date of notification.

Document Revision History

Date	Version	Description
2024-05-09	1.0.0	Initial release

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